Interfacing
OTG243
USB Host/Function/OTG Controller
to
MCF5272 ColdFire Processor

Reference Design

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Revision History

Version Number	Release Date	Notes
1.00	September, 2002	First release

Note: This document is subject to change without notice

Contents

1. Introduction

1.1 System Overview

TransDimension's OTG243 is a low cost, high-performance, easily programmable device designed specifically for embedded *USB host*, *USB function*, and USB On-The-Go (OTG) *dual role device* (DRD) applications. It can be configured to operate as:

- A standard USB OTG DRD controller (Port 1) and a standard USB 2-port host controller (Port 2 and Port 3).
- A standard USB 2-port host controller (Port 2 and Port 3), and a standard USB function controller (Port 1).
- A standard USB 3-port host controller (Port 1, Port 2 and Port 3).

The chip is designed for the embedded USB applications, especially mobile and post-PC products, including cell phones, palm platforms, personal digital assistants, set top boxes, home gateway systems, and Internet appliances. Peer-to-Peer communication is made simple with the OTG243 as USB connectivity may be achieved without the intervention of a personal computer. The block diagram for the OTG243 is shown below.

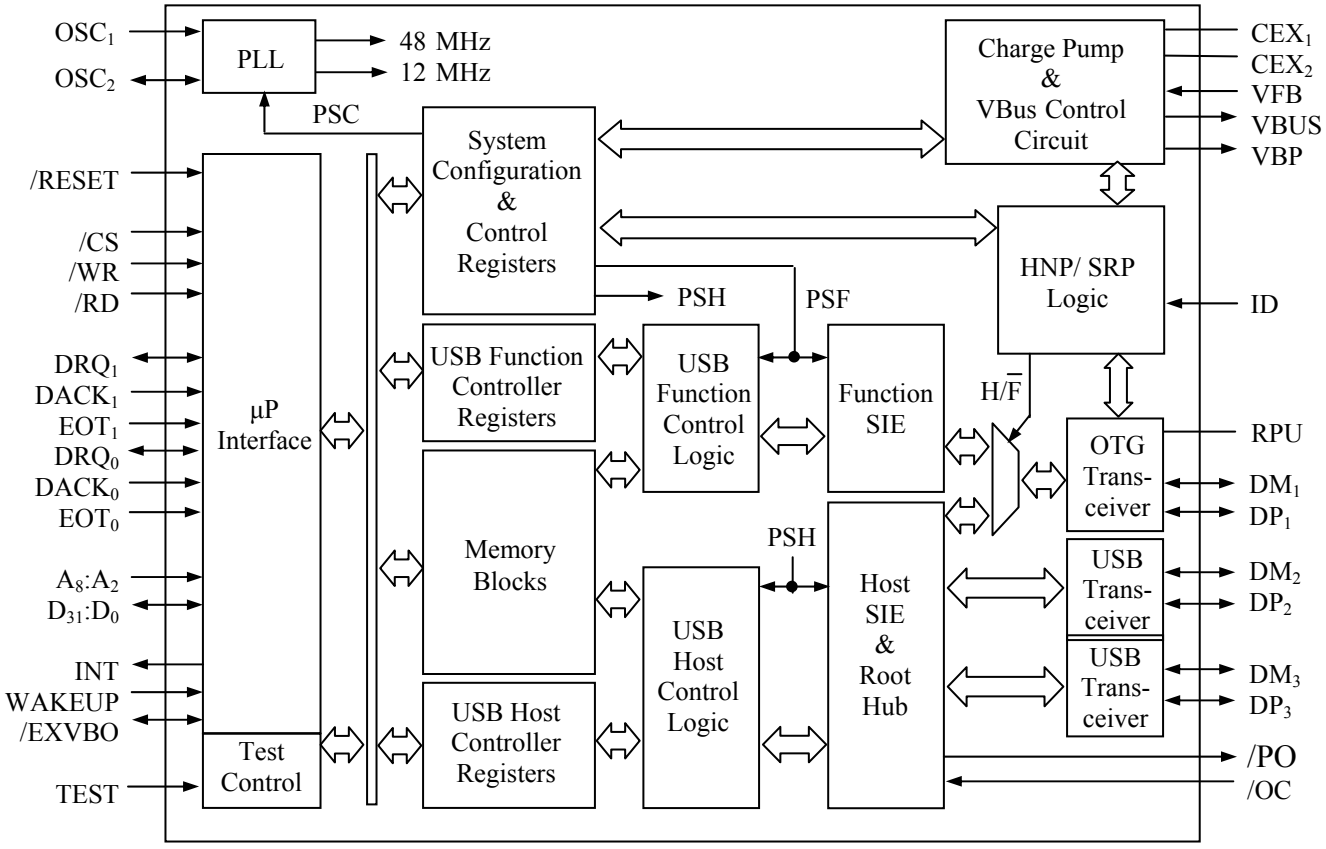


Figure 1: OTG243 block diagram

1	NC	21	V_{DD}	41	D_{26}	61	V_{DD}	81	VBUS
2	D_0	22	V_{DD}	42	D_{27}	62	V_{DD}	82	VFB
3	D_1	23	V_{SS}	43	V_{SS}	63	WAKEUP	83	/OC
4	D_2	24	TEST	44	V_{DD}	64	INT	84	/PO
5	V_{DD}	25	NC	45	DP_2	65	/RESET	85	ID
6	V_{DD}	26	/CS	46	DM_2	66	VBP	86	V_{SS}
7	D_3	27	/WR	47	DP_3	67	A_2	87	V_{DD}
8	D_4	28	/RD	48	DM_3	68	A_3	88	V_{DD}
9	D_5	29	D_{16}	49	NC	69	A_4	89	/EXVBO
10	D_6	30	D_{17}	50	NC	70	A_5	90	DRQ_1
11	D_7	31	D_{18}	51	NC	71	A_6	91	DRQ_0
12	V_{SS}	32	D_{19}	52	RPU	72	A_7	92	$DACK_1$
13	D_8	33	D_{20}	53	DP_1	73	A_8	93	$DACK_0$
14	D_9	34	D_{21}	54	DM_1	74	NC	94	EOT_1
15	D_{10}	35	D_{22}	55	V_{SS}	75	NC	95	EOT_0
16	D_{11}	36	D_{23}	56	D_{28}	76	AV_{DD}	96	V_{SS}
17	D_{12}	37	V_{DD}	57	D_{29}	77	AV_{SS}	97	AV_{SS}
18	D_{13}	38	V_{SS}	58	D_{30}	78	CEX_1	98	OSC_1
19	D_{14}	39	D_{24}	59	D_{31}	79	V_{DD}	99	OSC_2
20	D_{15}	40	D_{25}	60	V_{SS}	80	CEX_2	100	AV_{DD}

Figure 2**:** OTG243 pin assignment (LQFP)

1.2 References

General instructions on OTG243 interfacing are given in chapters 6 and 7 of the OTG243 data sheet (TDI document number: MU2001). This reference design describes a specific interfacing design of OTG243 with Motorola MCF5272 ColdFire®.

It is assumed that the user has knowledge on general principles of microprocessor interfacing, as well as some understanding on the Motorola MCF5272 and the OTG243. Reading Chapter 7 of USB Specification 2.0 is recommended.

1.3 Notation

For clarity, all OTG243 signal names in the following are in *italic* **bold**: e.g., ***A4*** and ***VBUS***, and active low signals are written with leading "/": e.g., ***/WR***.

MCF5272 names are in plain **bold**: e.g., **A4** and **nCS0**, and active low signals are written with leading "n": e.g, **CS0** is written as **nCS0**.

1.4 Software

TransDimension, together with SoftConnex Inc, its wholly owned subsidiary, offer total solutions including controller chips, reference designs, development kits, firmware for microprocessor interfacing, HCD (host controller driver), HNP (Host Negotiation Protocol), SRP (Session Request Protocol) as well as *USB Host* and *Function* stacks running under most real time operating systems.

2. Bus Interface

2.1 Recommendations

For the MCF5272, we recommend that:

- The OTG243 is interfaced directly to MCF5272's system bus.
- The OTG243 operates in 16-bit mode (pin ***/EXVBO*** pulled-down). This reference design has been tested in 16-bit mode, but should work just as well in 32-bit mode.
- The OTG243 is accessed through the MCF5272 chip-select as memory-mapped peripheral. Any of the chip-select signals **nCS[5:2]** can be programmed for an address location, with masking capabilities, port size, burst capability indication, and wait-state generation. **nCS2** is used for this reference design.
- The chosen chip-select is programmed to 16-bit access with a bus cycle compatible to that of the OTG243's.

The above recommendations are assumed throughout this document. Alternative interfacing schemes, such as 32-bit access to the OTG243, can function just as well.

2.2 Required Procedure

MCF5272 operates under big endian mode, but OTG243 operates under the little endian mode. Software is required to perform byte swapping for the data.

2.3 Hardware Design

This sub-section discusses hardware aspects of interfacing the OTG243 to the MCF5272. Software considerations are presented in Section 2.3.

The following signals of the OTG243 are involved in the bus interfacing. For simplicity and clarity, buffers are not inserted between the MCF5272 and the OTG243. One should use his/her own judgment on this issue based on a specific application.

*Operating Mode: /**EXVBO** and **TEST***

/EXVBO should be pulled down for 16-bit operation, and the ***TEST*** pin must be grounded.

*Bus Control: /**CS**, /**RD**, and /**WR***

In this reference design, the OTG243 is accessed through MCF5272's **nCS2** (base memory address 40000000). Thus OTG243 chip select ***/CS***, read strobe ***/RD***, and write strobe ***/WR*** should be tied to **nCS2**, **nOE/RD**, and **R/nW** of the MCF5272, respectively.

Address Bus: $\mathbf{A_8:A_2}$
The OTG243 address bus $\boldsymbol{A_8:A_2}$ is connected to **A8:A2** of the MCF5272.

Data Bus: $\boldsymbol{D_{31}:D_0}$

The lower 16-bit data bus of the OTG243 $\boldsymbol{D_{15}:D_0}$ should be connected to $\mathbf{D_{31}:D_{16}}$ of the MCF5272. This is due to MCF5272 data bus $\mathbf{D_{15}:D_0}$ becoming GPIO port C when configured as 16-bit external data bus. The upper 16-bit data bus of the OTG243 $\boldsymbol{D_{31}:D_{16}}$ should be pull-down with 15K resistors.

*Hardware Reset: **/RESET***

For many applications, the OTG243 ***/RESET*** can be tied to MCF5272's system reset (**nRSTI** or **nRSTO**). However, it is recommended that a MCF5272 GPIO pin be allocated as the OTG243 hardware reset for flexibility of user software.

In this reference design, **PC12** (GPIO Port C bit 12) of the MCF5272 is assigned to the OTG243's ***/RESET***, and its selection depends on the application. To improve reliability, a pull-up resistor is desired. An RC filter circuit is highly recommended to eliminate unexpected noise triggered reset.

*Interrupt: **INT***

The interrupt signal ***INT*** generated by the OTG243 must be tied to one of the six **nINT*n*** pins of the MCF5272. In this reference design, MCF5272 pin **nINT2** is employed, and its selection again depends on the application.

Note that the active level (active high or active low) and the output type (totem-pole or wired OR) of the OTG243 ***INT*** pin are programmable. For this reference design, the OTG243 ***INT*** pin is to be programmed to active low, totem-pole operation. A pull-up resistor is recommended.

Crystal Oscillator and PLL: ***OSC₁*** *and* ***OSC₂***

In the reference design, a 6 MHz parallel resonance quartz crystal is connected across ***OSC₁*** and ***OSC₂***. The following circuit is recommended.

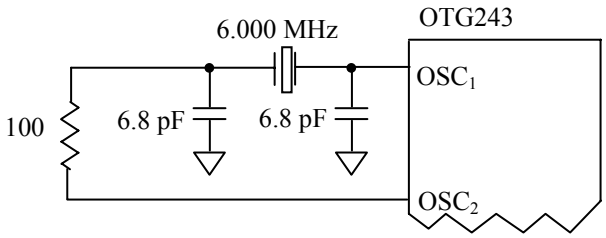


Figure 3: OTG243 crystal oscillator circuit

To meet the USB frequency accuracy and stability requirements, the crystal should have an accuracy and stability better than 200 ppm. For a 6 MHz resonance quartz crystal, the recommended ESR value should be less than 100 Ω.

DMA: ***DRQ₁, DACK₁, EOT₁, DRQ₂, DACK₂,*** *and* ***EOT₂***
In this reference design, DMA is not tested and not supported.

When these signals are not used, proper connections should be made by pulling up or down according to the application.

The logic levels of ***DRQ₁*** and ***DRQ₂*** at the time of hardware reset determine the frequency of the oscillation imposed on the ***OSC₁*** and/or ***OSC₂*** pins. In this reference design, a 6 MHz crystal is employed. Therefore the ***DRQ₁*** and ***DRQ₂*** should be tied with pull-down resistors smaller than 10kΩ.

Since ***DACK₁***, ***DACK₂***, ***EOT₁***, and ***EOT₂*** signals are all configured as inputs and active low signals right after reset, they should be pulled-up by resistors.

Note: Even though the MCF5272 has a one-channel DMA controller internal to MCF5272, which supports memory-to-memory DMA transfers that can be used for block data moves, it does not require any external signals for DMA transfer. It uses normal memory access signals for DMA transfer.

Remote Wakeup: ***WAKEUP***
This pin is only meaningful if Port 1 of the OTG243 is assuming the role of a USB function. In this reference design, a MCF5272 GPIO pin (**PC13**) is assigned to it. Since ***WAKEUP*** is active high, a pull-down resistor is recommended.

External Pull-Up: ***RPU***

If the internal pull-up resistor does not satisfy the USB 1.5KΩ pull-up tolerance, an external 1.5KΩ +/- 1% can be connected from ***RPU*** signal to ***DP₁*** signal.

This pin should be left floating if external 1.5KΩ pull-up resistor is not used.

*OverCurrent: **/OC***
It is recommended to add an external pull-up for OverCurrent signal.

*Power On: **/PO***
This ganged power-on signal is an output, so it is OK to leave it floating if not used.
However, do not use pull-up resistor if this signal is used in a low power application. If OTG243 is put into power-save mode with ***/PO*** signal asserted, there will be unnecessary current leakage through this pull-up resistor.

2.4 Software Configuration

Bus Cycle Timing

Bus cycle timing parameters for the OTG243 read/write operation are listed below. The OTG243 register read and register write cycles are illustrated in Figures 5 and 6, respectively.

Symbol	Parameter	Min	Max	Unit
t_{RPW}	/RD pulse width	55		ns
t_{WPW}	/WR pulse width	55		ns
t_{ACR}	Access cycle recovery time	25		ns
t_{ASL}	Address setup time before /RD or /WR goes low	0		ns
t_{AHH}	Address hold time after /RD or /WR high	0		ns
t_{DSW}	Data setup time before /WR high	45		ns
t_{DVR}	Data valid time after /RD low		55	ns
t_{DHR}	Data hold time after /RD high		3	ns
t_{DHW}	Data hold time after /WR high	0		ns
t_{CRWL}	/CS low to /RD or /WR low	0		ns
t_{RWCH}	/RD or /WR high to /CS high	0		ns

Figure 4: OTG243 bus cycle timing parameters

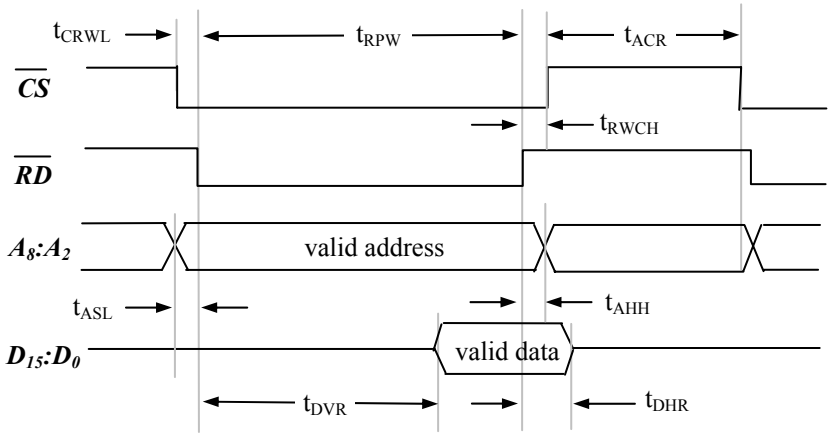


Figure 5: OTG243 register read cycle

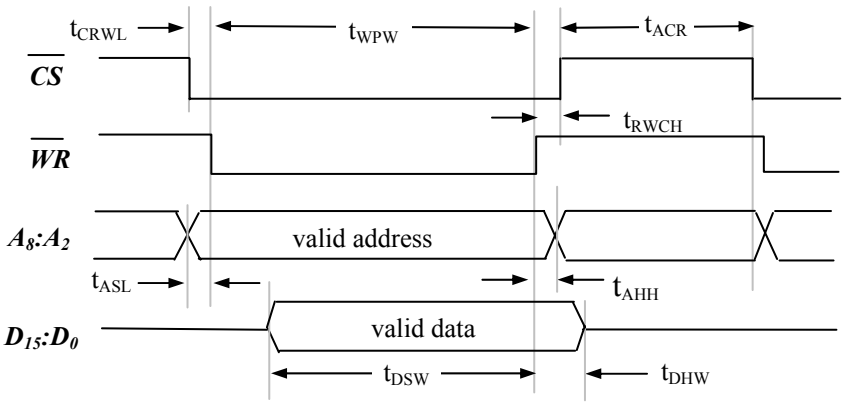


Figure 6: OTG243 register write cycle

MCF5272 Chip Select Programming

Based on the OTG243 register read/write cycle specification, the chip select base registers (CSBR2) and the chip select option registers (CSOR2) for **nCS2** may be programmed according to the following:

CSBR2

Addr : 0x050
Default value after reset : 0x0000_2300

Field	Bits	Function	Settings	Meaning	Default
BA	31:12	Base Address.	4000_0	Starting address	0000_2
EBI	11:10	External bus interface modes.	00	16/13-bit SRAM/ROM	00
BW	9:8	Bus width.	10	Word (16 bits)	11
SUPER	7	Supervisor mode.	0	User or Supervisor mode	0
TT	6:5	Transfer type.	00	Don't care, since CTM is not set.	00
TM	4:2	Transfer modifier.	000	Don't care, since CTM is not set.	000
CTM	1	Compare TM.	0	TT & TM register bits do not affect address match.	0
ENABLE	0	Enable	1	CS2 enabled	0

CSOR2

Addr : 0x054
Default value after reset : 0xFFFF_F078

Field	Bits	Function	Settings	Meaning	Default
BAM	31:12	Address mask	FFFF_F	Compare address bits	FFFF_F
ASET	11	Address setup enable	1	Delay assertion of chip select for one CLK cycle after address is asserted. During write transfers, both chip select and **R/nW** are delayed by 1 clock cycle.	0
WRAH	10	Controls the address, data and attribute hold time after the termination, internal or external with /TA, of a write cycle that hits in the chip select address space.	1	Hold address, data, and attribute signals an extra cycle after **nCS2** and **R/nW** negate on writes	0
RDAH	9	Controls the address and attribute hold time after the termination, internal or external with /TA, of a read cycle that hits in the chip select address space.	1	Hold address and attribute signals an extra cycle after chip select negate on reads.	0
EXTBURST	8	Enable extended burst.	-	Vailid only for **nCS7**.	0
-	7	Reserved, should be cleared.			0
WS	6-2	Wait state generator	00011	3 wait states	11110
RW	1	RW and MRW determine whether the selected memory region is read only or write only.	0	Don't care since MRW is cleared.	0
MRW	0	MRW must be set for value of RW be taken into consideration.	0	Memory covered by chip select is read/write	0

PBCNT

Addr : 0x088
Default value after reset : 0x0000_0000

Field	Bits	Function	Settings	Meaning	Default
PBCNT5	11:10	Port B Control Regitster. PB5/nTA select	00	Select PB5	00

Figure 7: MCF5272 register CSBR2, CSOR2, & PBCNT settings to generate **nCS2**

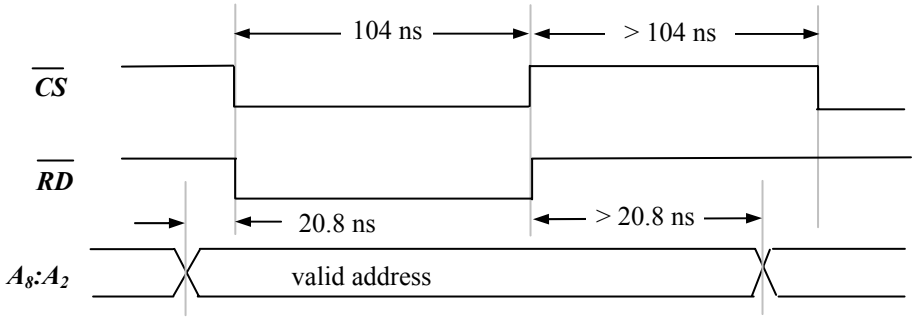


Figure 8: MCF5272 bus read cycle generated using parameters of Figure 7

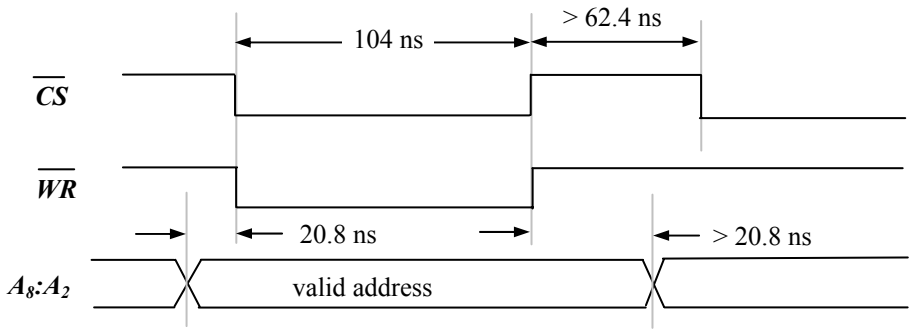


Figure 9: MCF5272 bus write cycle generated using parameters of Figure 7

The memory map of **nCS2** is determined by 2 parameters. The content of BA field in CSBR2 register determines the starting address of the **nCS2**. The content of BAM field in CSOR2 register determines the memory block size of **nCS2**. In this design the starting address is set to 0x40000000, and the block size is set 4K byte.

The wait states are controlled by the combination of ASET, WRAH, RDAH, and WS fields in CSOR2 register. In this design, ASET, WRAH, and RDAH are set and WS is set to 3 wait states. Also, the transfer acknowledge (**nTA)** signal is not utilized but this signal is assigned as GPIO port **PB5** in this reference design.

Note that these settings are based on the assumption that the MCF5272 is running at an external 48 MHz oscillator. They are set for the MCF5272 to generate near-optimal access cycles satisfying the OTG243 specification. It is advised that one starts with a much looser (slower) set of timing parameters, such as 1FH, applied to the WS field of this CSOR2 register, and then have them fine-tuned towards optimal performance.

Software Controlled OTG243 Reset

It is assumed that **PC12** of the MCF5272 is employed to support software controlled ***/RESET*** for the OTG243. The MCF5272 GPIO registers should be initialized according to Figure 12.

Register	Address	Register Full Name	Bit 12	Meaning	Default
PCDDR	0x0094	Port C Data Direction Register	1	output	0
PCDAT	0x0096	Port C Data Register	1	no reset	undefined

Figure 12: MCF5272 GPIO register settings to support software generated ***/RESET***

To issue an OTG243 reset through software, one must

Step 1: Write to GPIO register PCDAT with a bit pattern such that Bit 12 = 0. This asserts the active low OTG243 pin ***/RESET***.

Step 2: Wait for at least 40 µs.

Step 3: Write to GPIO register PCDAT with a bit pattern such that Bit 27 = 1. This de-asserts the active low OTG243 pin ***/RESET***.

Software Controlled Remote Wakeup

It is assumed that **PC13** of the MCF5272 is employed to support software controlled ***/WAKEUP*** for the OTG243 function operation. The MCF5272 GPIO registers should be initialized according to Figure 13.

Register	Address	Register Full Name	Bit 13	Meaning	Default
PCDDR	0x0094	Port C Data Direction Register	1	output	0
PCDAT	0x0096	Port C Data Register	0	no wakeup	undefined

Figure 13: MCF5272 GPIO register settings to support software generated ***WAKEUP***

To issue a remote wakeup to the OTG243 through software, one must

Step 1: Write to GPIO register PCDAT with a bit pattern such that Bit 13 = 1. This asserts the active high OTG243 ***WAKEUP***.

Step 2: Wait for at least 1 µs.

Step 3: Write to GPIO register PCDAT with a bit pattern such that Bit 13 = 0. This de-asserts the active high OTG243 ***WAKEUP***.

Interrupt: MCF5272 Configuration

In the following discussion, it is assumed that **nINT2** of the MCF5272 is connected to OTG243's ***INT*** pin, which has been programmed to be active low with totem-pole output.

The MCF5272's interrupt control registers should be initialized as follows:

Register	Address	Register Full Name	Bits	Bit Values	Meaning	Default
ICR1	0x020	Interrupt Control Register 1	27:24	1011	Interrupt priority level	0000
PITR	0x034	Programmable Interrupt Transition Register	30	0	Negative edge triggered	0

Figure 14: MCF5272 GPIO register settings to support OTG243 interrupt

Please note that the interrupt generated by the OTG243 is level sensitive. Caution must be taken when it is interfaced with an interrupt controller, such as the one in the MCF5272, that supports only edge-sensitive interrupt sources.

Interrupt: OTG243 Configuration

The software must configure the OTG243 before the MCF5272 enables the interrupt originated from it. The following steps must be carried out:

Step 1: Configure the OTG243 ***INT*** pin to be active low. This requires Bit 16 of the OTG243 HardwareMode Register (000H) be set to 0, which is the default.

Step 2: Configure the OTG243 ***INT*** pin to be totem-pole output. This requires Bit 21 of the IOConfiguration2 Register (04CH) to be set to 1 by user software. Note that the ***INT*** pin defaults to wired OR output, which should also work if a pull-up resistor is present.

Step 3: Enable interrupt sources on the OTG243 side, which involves four sets of registers as described in detail in Section 7.4 of the OTG243 Data Sheet.

USB System Initialization

It should be emphasized that all MCF5272 register settings and the OTG243 hardware system settings discussed above must be completed before the USB controllers within the OTG243 are activated.

2.5 OTG243 Access

OTG243 Memory Map

The OTG243 control registers and internal memory blocks are accessed through a two-level memory map as shown in Figure 9. It should be emphasized that all registers and data accesses are in 32-bit double word (DWORD), even if the OTG243 is placed on a 16-bit bus. In the latter case, a pair of 16-bit accesses (first for the least significant 16-bits, and the second for the most significant two bytes) must be issued successfully by the microprocessor for reading or writing a single DWORD. Thus the least significant two bits of the address bus (A_1 and A_0) are always treated as 00b.

The MCF5272 communicates with the OTG243 through the *Primary Memory Map* (PMM), consisting of 128 DWORD registers. Thus all OTG243 accesses to the OTG243 are register reads or register writes. In other words, the microprocessor does not access the OTG243's internal memories.

The *ETD Memory* (128 DWORDs) and the *Data Memory* (1K DWORDs) inside the OTG243 are accessed through an address register named MemoryAccessStartAddress Register (0A4H), and a data port register called PIODataPort Register (02CH) using the standard two-stage access methodology. If the **MemoryAccessType** bit (Bit 15 of the MemoryAccessStartAddress register) is 0, the ETD Memory is accessed. Otherwise, the Data Memory is read from or written into.

It must be emphasized that the address specified in the MemoryAccessStartAddress register is in DWORDs, not in bytes, relative to the beginning of the ETD Memory or the Data Memory, respectively. Using burst read and burst write, the OTG243 supports fast data movement between the microprocessor and on-chip memory.

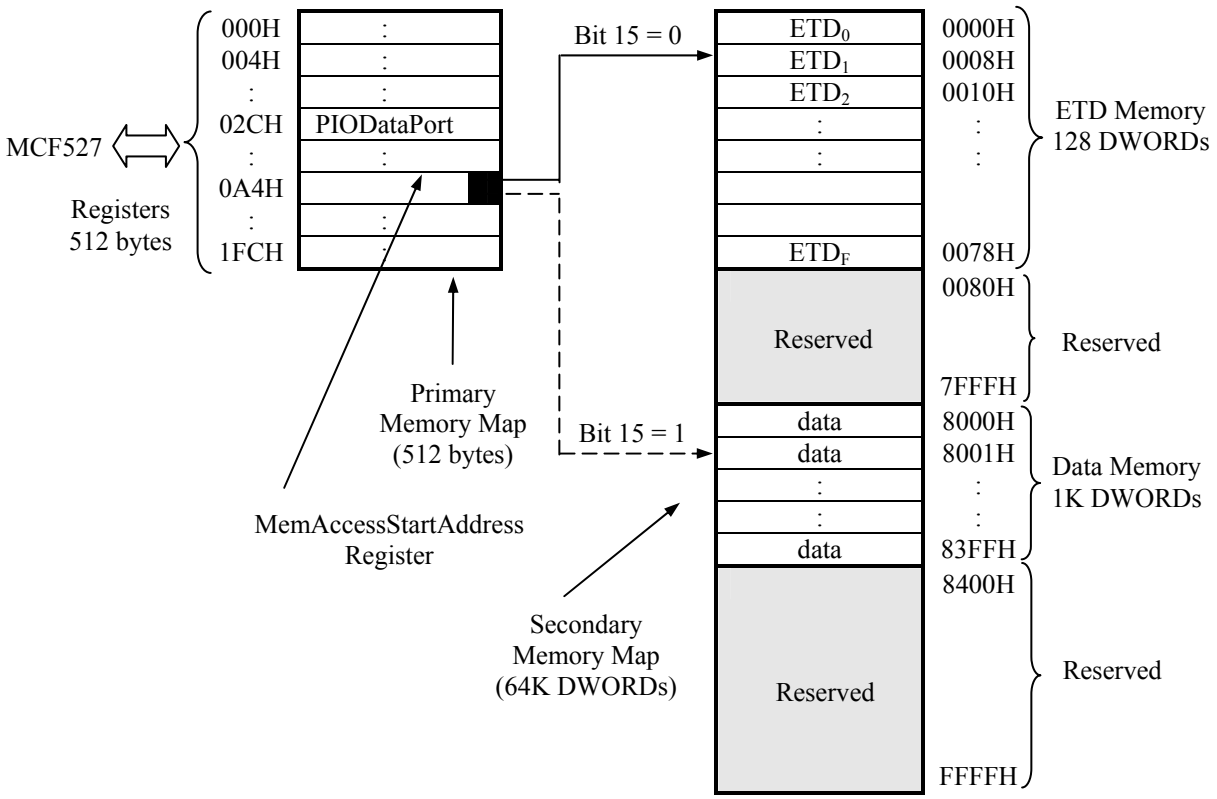


Figure 9: OTG243 memory map

OTG243 Register Access

In this reference design, the physical address used by the MCF5272 to access OTG243 address *m* in its PMP is 40000000H + *m*, where 000H ≤ *m* ≤ 1FFH. Note that the least significant two bits of *m* are always treated as 00B.

OTG243 On-Chip Memory Access

The ETD Memory (128 DWORDs) and Data Memory (1K DWORDs) can be accessed through a procedure called *Programmed I/O* (PIO), which is carried out as follows:

Step 1: Write into MemoryAccessStartAddress Register an *access word* indicating (i) memory segment - either ETD Memory or Data Memory; (ii) access address - offset to the beginning of the memory segment indicated in (i). Note that the unit of this address is DWORDs, not bytes; and (iii) intended access direction - Read or Write. Formats of the access word for the ETD Memory and that for the Data Memory are given in Figures 10 and 11, respectively.

Bit	Description
8:0	Address (relative to the beginning of the respective memory) in DWORDs.
14	Access direction. 1 for write and 0 for read.
15	Selection between ETD memory (0) and data memory (1).
13:9, 31:16	Reserved. Should be filled with 0's.

Figure 10: ETD Memory access word

Bit	Description
11:0	Address (relative to the beginning of the respective memory) in DWORDs.
14	Access direction. 1 for write and 0 for read.
15	Selection between ETD memory (0) and data memory (1).
13:12, 31: 16	Reserved. Should be filled with 0's.

Figure 11: Data Memory access word

Step 2: Wait until the PIO channel is ready by examining the **PIOReady** bit (Bit 0) of the PIOReady Register (044H). Continue to Step 3 only after the bit has become low.

Step 3: Write into, or read from the PIODataPort register (02CH) for one DWORD, or a block of consecutive DWORDs. In the latter case, the accessing address is increased automatically. The access direction (read/write) in this step should be consistent with that specified in the access word. (If not, the access direction indicated in the access word takes precedence.)

3. USB Port Circuits

This section discusses circuits between the USB ports of the OTG243 and their connectors. Note that these issues are generic and in fact independent to that of the MCF5272 interfacing. One should consult Chapter 7 of the USB specification 2.0, as well as Chapters 6 and 7 of the OTG243 data sheet for details.

3.1 OTG243 Port 2 and Port 3

These two ports can only serve as standard downstream host ports. Thus they use USB Type A receptacles.

USB Signal Lines

Two 15 kΩ pull-down resistors are required on the $\boldsymbol{DP_n}$ and $\boldsymbol{DM_n}$ (n = 2, 3) data lines to support detection of a device connecting or disconnecting event.

To satisfy the impedance matching requirement, a 33 Ω resistor should be inserted between a USB data line ($\boldsymbol{DP_n}$ or $\boldsymbol{DM_n}$) and its corresponding pin at the USB Type A connector.

If a port is not used, its ***DM$_n$*** and ***DP$_n$*** pins must be pulled down via 15 kΩ resistors. They cannot be grounded directly or be left floating.

USB Host Power Distribution

In this reference design, TI's dual power-distruibution switch TPS2042 is employed. When the current flowing through this device exceeds the current-limit threshold (0.9A) or a short is present, the ***/OC*** pin of the OTG243 is asserted.
As an alternative, a poly-switch resettable device (nanoSMD100, specially made by RayChem/Tyco for USB applications) can be used.

A sufficiently large capacitor (more than 120 μF) is applied to the VBus of each port, per USB specification. Ferrite beads are inserted in the VBus and ground circuits for EMI reduction.

3.2 OTG243 Port 1

This port can be configured as a standard USB host port, a standard USB function port, or an OTG port. The details are given in Section 6 of the OTG243 data sheet. In this reference design, Port 1 serves as a port for a USB OTG dual role device.

USB Signals

The USB signal circuits for Port 1 (DM1, DP1) are similar to that of Port 2 and Port 3, except that the two pull-down resistors are integrated with the OTG transceiver circuit. In addition, this reference design chooses the internal pull-up resistor when the OTG243 assumes the role of a full speed USB function.

VBus Circuit

In the reference design, the internal charge pump is used as the Vbus power source. As an A-Device, it supplies the power of 5V of up to 12 mA. As a B-Device, it is the power source for "VBus pulsing".

A capacitor of 0.47 μF must be connected between OTG243 pins ***CEX$_1$*** and ***CEX$_2$***. Two 2.2 μF capacitors and a 10 μH inductor constitutes a low pass filter for the charge pump output. A 10 Ω resistor and a 1 μF capacitor serve as part of the voltage feedback.

Software Considerations

Operating as a USB OTG controller, the OTG243 implements the HNP/SRP (Host Negotiation Protocol and Session Request Protocol), which configures Port 1 circuit dynamically. For details, please contact TransDimension technical support for details.

4. Power and Ground

The chip can be used with a single DC power supply of 3.3V. V_{DD} and AV_{DD} should be connected at only one point on a printed circuit board. This also applies to V_{SS} and AV_{SS}.

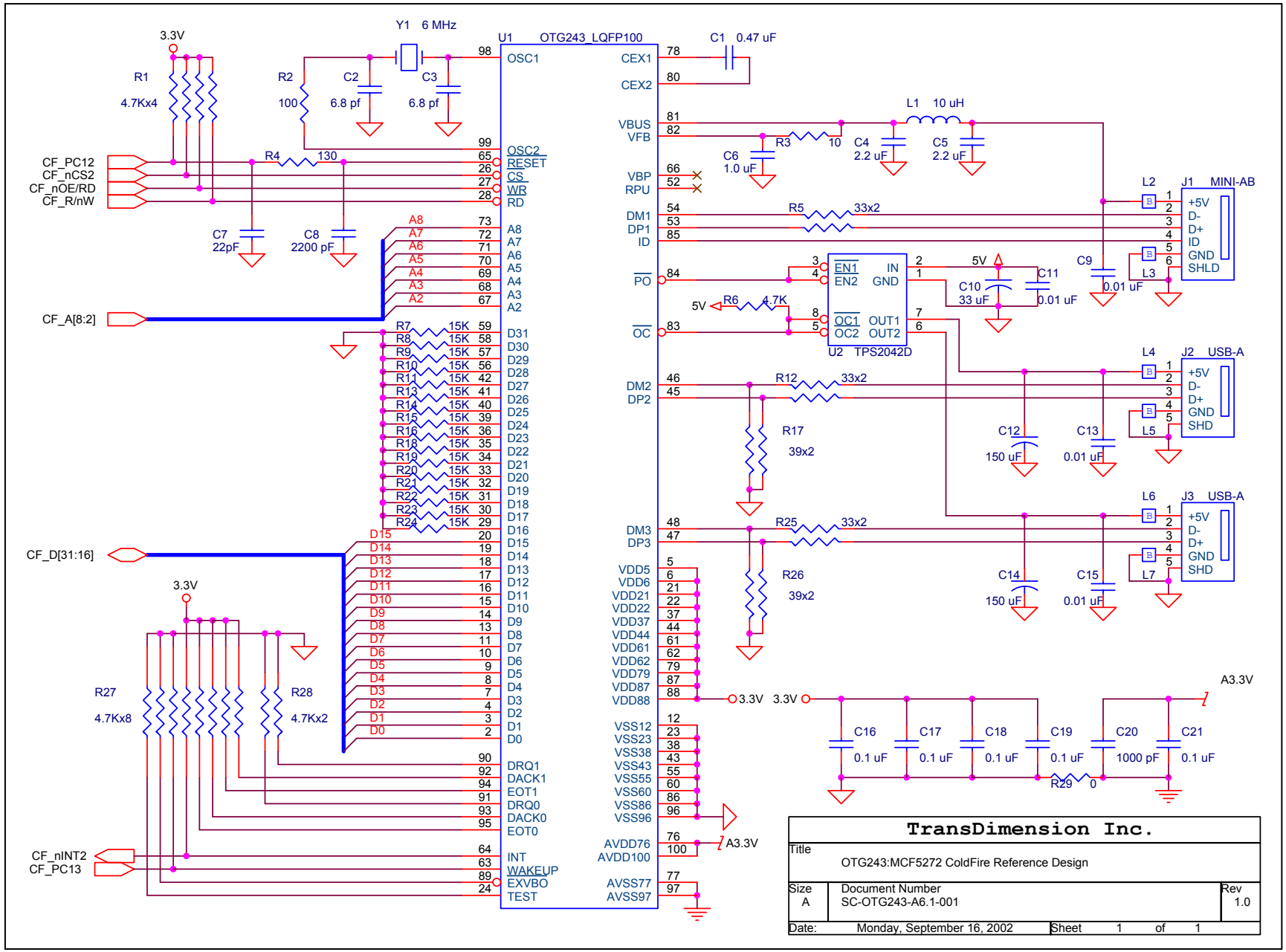
All logic I/O pins are LVCTTL compatible, and 5V tolerant.

5. Reference Design Schematics

The schematic drawing on Page 14 is based on several assumptions made in the above discussion. It must be modified according to one's application.

6. OTG243 Module for uCevolution Development Platform

TransDimension has developed an OTG243 module (CXB243) that can be plugged into the soDIMM bus of the uCevolution Development Platform with uCdimm ColdFire 5272 Microcontroller Module, allowing quick OTG243 evaluation and user software development. Contact TDI technical support for details.


3.3V
Y1 6 MHz
U1 OTG243_LQFP100
C1 0.47 uF
R1 4.7Kx4
R2 100
C2 6.8 pf
C3 6.8 pf
OSC1
CEX1
CEX2
L1 10 uH
VBUS
VFB
R3 10
C4 2.2 uF
C5 2.2 uF
C6 1.0 uF
VBP
RPU
CF_PC12
CF_nCS2
CF_nOE/RD
CF_R/nW
R4 130
OSC2
RESET
CS
WR
RD
DM1
DP1
ID
R5 33x2
L2 J1 MINI-AB
+5V
D-
D+
ID
GND
SHLD
C7 22pF
C8 2200 pF
PO
EN1
EN2
IN
GND
OC1
OC2
OUT1
OUT2
U2 TPS2042D
5V
R6 4.7K
C10 33 uF
C11 0.01 uF
C9 0.01 uF
L3
OC
CF_A[8:2]
A8
A7
A6
A5
A4
A3
A2
R7 15K
R8 15K
R9 15K
R10 15K
R11 15K
R12 15K
R13 15K
R14 15K
R15 15K
R16 15K
R17 15K
R18 15K
R19 15K
R20 15K
R21 15K
R22 15K
R23 15K
R24 15K
D31
D30
D29
D28
D27
D26
D25
D24
D23
D22
D21
D20
D19
D18
D17
D16
D15
D14
D13
D12
D11
D10
D9
D8
D7
D6
D5
D4
D3
D2
D1
D0
DM2
DP2
R12 33x2
R17 39x2
C12 150 uF
C13 0.01 uF
L4 J2 USB-A
L5
CF_D[31:16]
DM3
DP3
R25 33x2
R26 39x2
C14 150 uF
C15 0.01 uF
L6 J3 USB-A
L7
VDD5
VDD6
VDD21
VDD22
VDD37
VDD44
VDD61
VDD62
VDD79
VDD87
VDD88
3.3V
R27 4.7Kx8
R28 4.7Kx2
VSS12
VSS23
VSS38
VSS43
VSS55
VSS60
VSS86
VSS96
A3.3V
C16 0.1 uF
C17 0.1 uF
C18 0.1 uF
C19 0.1 uF
C20 1000 pF
C21 0.1 uF
R29 0
DRQ1
DACK1
EOT1
DRQ0
DACK0
EOT0
AVDD76
AVDD100
AVSS77
AVSS97
CF_nINT2
CF_PC13
INT
WAKEUP
EXVBO
TEST
TransDimension Inc.
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Size A
Document Number SC-OTG243-A6.1-001
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Sheet 1 of 1

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