TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

JT6C30-AS

DOT MATRIX LCD CONTROLLER AND DRIVER LSI

The JT6C30-AS is a dot matrix LCD controller and driver. The JT6C30-AS realizes low power consumption for an LCD using CMOS Si-gate technology.
The JT6C30-AS can be controlled by serial data from an MPU, and can display alphanumerics, kana and symbols.
The JT6C30-AS has all the functions necessary to drive a dot matrix LCD. Therefore, the JT6C30-AS can constitute a minimal drive and control system for an LCD.
The JT6C30-AS can display up to 80 digits using an expansion driver (e.g. T6B23). The JT6C30-AS has an 8×10-key matrix drivers and 40 LED drivers (an 8×5 matrix).

FEATURES

- Built-in controller for character-type LCD
- Direct Interface with MPU (serial interface)
- Data transfer clock : f_{osc} = 3.0MHz max
- Display data RAM : 80×8 bits
- Character generator ROM : 12000 bits (5×10×240)
- Character generator RAM : 512 bits (64×8)

  Character font ..... ① 5×8 dots : 8 characters
  ② 5×11 dots : 4 characters
- Built-in 8×10 key matrix scan controller
- Built-in 8×5 LED controller (buffer not built-in)
- Built-in LCD drivers

  50-out Column driver
  32-out Row driver
- Input port : 4 bits
- Output port : 4 bits

- Duty factor selection (programmable)

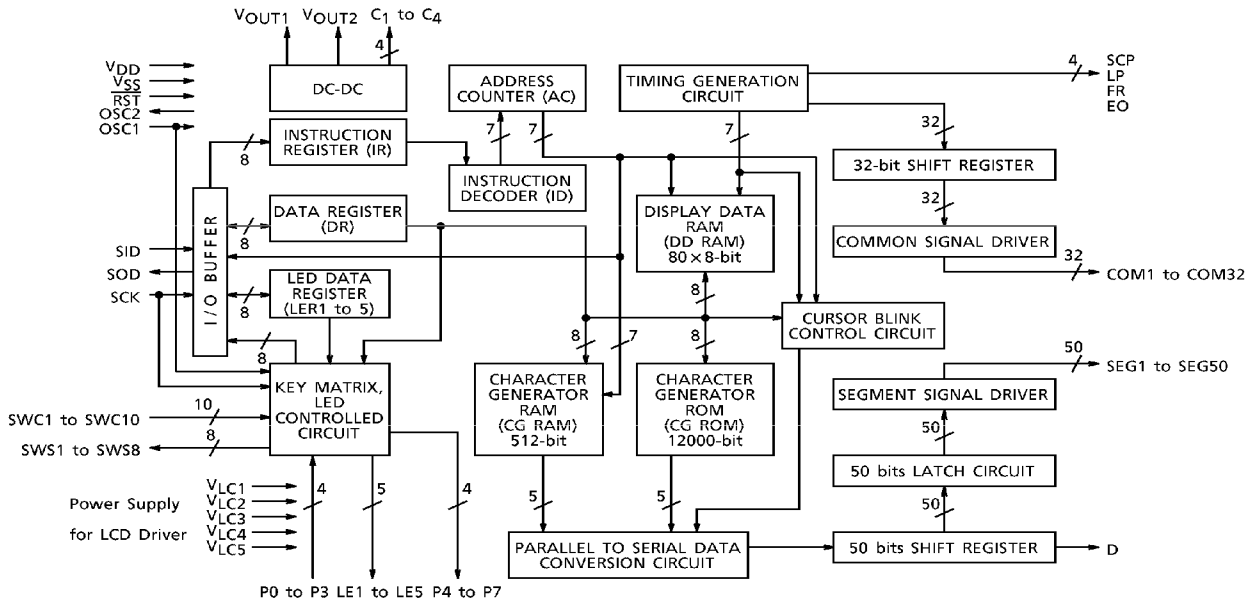
  1 / 8 duty cycle : (Font : 5 × 7 dots + cursor) × 1 line
  1 / 11 duty cycle : (Font : 5 × 10 dots + cursor) × 1 line
  1 / 16 duty cycle : (Font : 5 × 7 dots + cursor) × 2 lines
  1 / 22 duty cycle : (Font : 5 × 10 dots + cursor) × 2 lines
  1 / 32 duty cycle : (Font : 5 × 7 dots + cursor) × 4 lines

- Applications

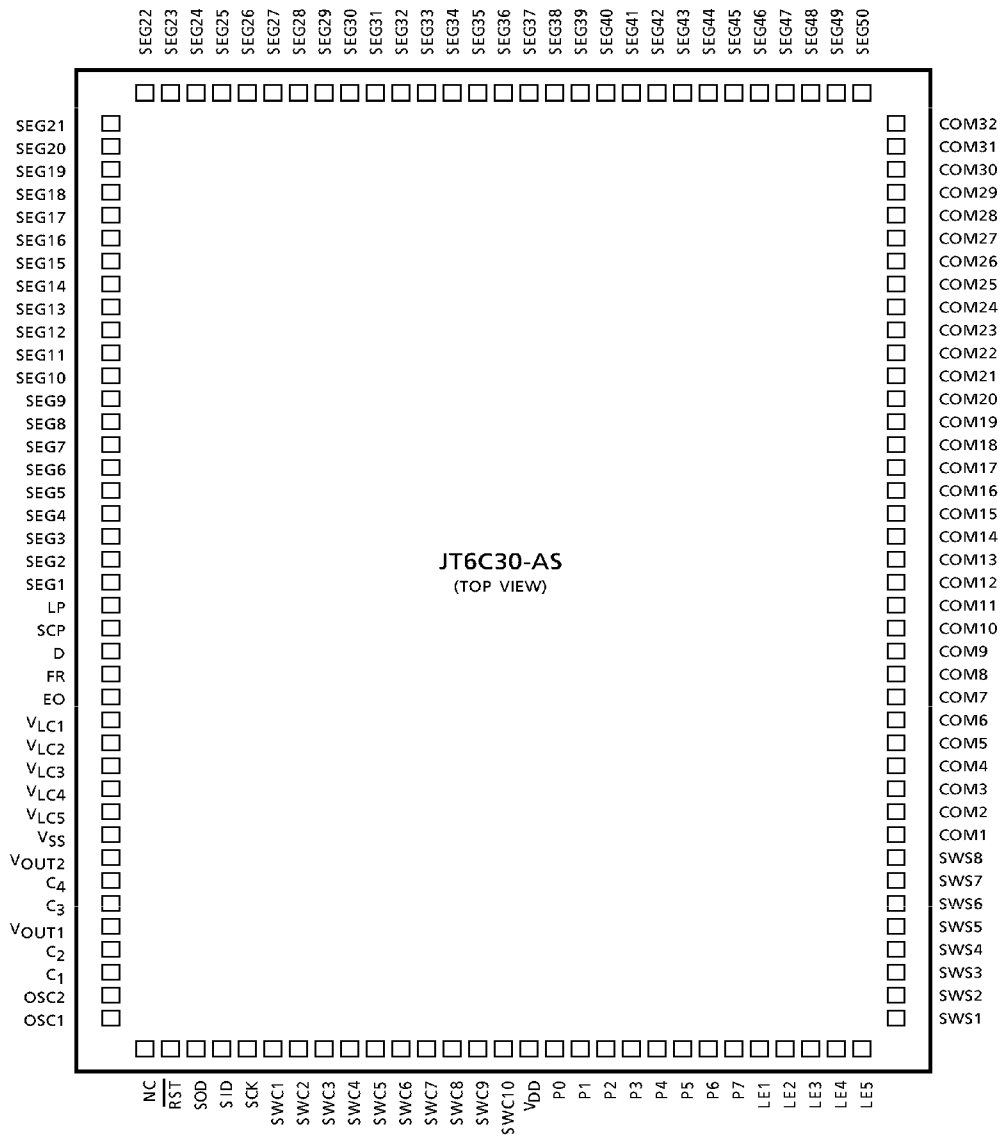
  Display clear, Cursor home, Display ON / OFF, Cursor ON / OFF
  Character blink, Character shift, Display shift, Cursor shift.

- Power supply : 5V ± 10%
- Low power consumption
- CMOS and Si-gate processes, Bare chip

BLOCK DIAGRAM



PAD ASSIGNMENT



PAD COORDINATES

Chip Size .... 5.260 × 6.880 (mm) 6.016 (mm□)
Number of pads 138
Chip Tip Coordinates 1 ..... −2630.0, −3440.0
Chip Tip Coordinates 2 ..... −2630.0, 3440.0
Chip Tip Coordinates 3 ..... 2630.0, 3440.0
Chip Tip Coordinates 4 ..... 2630.0, −3440.0

No.	NAME	X POINT	Y POINT
1	NC	−2230	−3171
2	$\overline{RST}$	−2049	−3171
3	SOD	−1864	−3171
4	SID	−1713	−3171
5	SCK	−1563	−3171
6	SWC1	−1413	−3171
7	SWC2	−1263	−3171
8	SWC3	−1113	−3171
9	SWC4	−962	−3171
10	SWC5	−812	−3171
11	SWC6	−662	−3171
12	SWC7	−512	−3171
13	SWC8	−361	−3171
14	SWC9	−211	−3171
15	SWC10	−61	−3171
16	V_{DD}	89	−3171
17	P0	239	−3171
18	P1	390	−3171
19	P2	540	−3171
20	P3	690	−3171
21	P4	840	−3171
22	P5	990	−3171
23	P6	1141	−3171
24	P7	1291	−3171
25	LE1	1474	−3171
26	LE2	1625	−3171
27	LE3	1811	−3171
28	LE4	1961	−3171
29	LE5	2148	−3171
30	SWS1	2390	−3036
31	SWS2	2390	−2850
32	SWS3	2390	−2700
33	SWS4	2390	−2513

No.	NAME	X POINT	Y POINT
34	SWS5	2390	−2363
35	SWS6	2390	−2176
36	SWS7	2390	−2026
37	SWS8	2390	−1840
38	COM1	2390	−1689
39	COM2	2390	−1539
40	COM3	2390	−1389
41	COM4	2390	−1239
42	COM5	2390	−1089
43	COM6	2390	−938
44	COM7	2390	−788
45	COM8	2390	−638
46	COM9	2390	−488
47	COM10	2390	−337
48	COM11	2390	−187
49	COM12	2390	−37
50	COM13	2390	113
51	COM14	2390	263
52	COM15	2390	414
53	COM16	2390	564
54	COM17	2390	714
55	COM18	2390	864
56	COM19	2390	1015
57	COM20	2390	1165
58	COM21	2390	1315
59	COM22	2390	1465
60	COM23	2390	1615
61	COM24	2390	1766
62	COM25	2390	1916
63	COM26	2390	2066
64	COM27	2390	2216
65	COM28	2390	2367
66	COM29	2390	2517

No.	NAME	X POINT	Y POINT
67	COM30	2390	2667
68	COM31	2390	2817
69	COM32	2390	2967
70	SEG50	2103	3175
71	SEG49	1952	3175
72	SEG48	1802	3175
73	SEG47	1652	3175
74	SEG46	1502	3175
75	SEG45	1352	3175
76	SEG44	1201	3175
77	SEG43	1051	3175
78	SEG42	901	3175
79	SEG41	751	3175
80	SEG40	601	3175
81	SEG39	450	3175
82	SEG38	300	3175
83	SEG37	150	3175
84	SEG36	0	3175
85	SEG35	– 151	3175
86	SEG34	– 301	3175
87	SEG33	– 451	3175
88	SEG32	– 601	3175
89	SEG31	– 751	3175
90	SEG30	– 902	3175
91	SEG29	– 1052	3175
92	SEG28	– 1202	3175
93	SEG27	– 1352	3175
94	SEG26	– 1503	3175
95	SEG25	– 1653	3175
96	SEG24	– 1803	3175
97	SEG23	– 1953	3175
98	SEG22	– 2103	3175
99	SEG21	– 2390	2967
100	SEG20	– 2390	2817
101	SEG19	– 2390	2667
102	SEG18	– 2390	2517
103	SEG17	– 2390	2367
104	SEG16	– 2390	2216
105	SEG15	– 2390	2066
106	SEG14	– 2390	1916

No.	NAME	X POINT	Y POINT
107	SEG13	– 2390	1766
108	SEG12	– 2390	1615
109	SEG11	– 2390	1465
110	SEG10	– 2390	1315
111	SEG9	– 2390	1165
112	SEG8	– 2390	1015
113	SEG7	– 2390	864
114	SEG6	– 2390	714
115	SEG5	– 2390	564
116	SEG4	– 2390	414
117	SEG3	– 2390	263
118	SEG2	– 2390	113
119	SEG1	– 2390	– 37
120	LP	– 2390	– 187
121	SCP	– 2390	– 374
122	D	– 2390	– 524
123	FR	– 2390	– 710
124	EO	– 2390	– 861
125	V_{LC1}	– 2390	– 1053
126	V_{LC2}	– 2390	– 1203
127	V_{LC3}	– 2390	– 1353
128	V_{LC4}	– 2390	– 1504
129	V_{LC5}	– 2390	– 1654
130	V_{SS}	– 2390	– 1804
131	V_{OUT2}	– 2390	– 1954
132	C_4	– 2390	– 2105
133	C_3	– 2390	– 2255
134	V_{OUT1}	– 2390	– 2405
135	C_2	– 2390	– 2555
136	C_1	– 2390	– 2715
137	OSC2	– 2390	– 2856
138	OSC1	– 2390	– 3006

PIN FUNCTIONS

SYMBOL	TYPE	NAME AND FUNCTION
SCK	Input	System Clock
SID	Input	Serial Data Input
SOD	Output	Serial Data Output
P0 to P3	Input	Input port
P4 to P7	Output	Output port
SWC1 to SWC10	Input	Key matrix inputs
SWS1 to SWS8	Output	Key matrix outputs, LED control data outputs
LP	Output	Latch Pulse : Latch pulse for the extension driver (e.g. T6B23)
SCP	Output	Shift Clock Pulse : Shift clock pulse for the extension driver (e.g. T6B23)
FR	Output	Frame Signal : FR signal for the extension driver (e.g. T6B23)
D	Output	Data : Display data for the extension driver (e.g. T6B23)
EO	Output	Enable Output : Enable signal to the extension driver (e.g. T6B23)
COM1 to COM32	Output	Common : Row outputs When 1/8 duty cycle is selected, COM9 to COM32 are disabled. When 1/16 duty cycle is selected, COM17 to COM32 are disabled.
SEG1 to SEG50	Output	Segment : Column outputs.
V_{LC5}	Input	Power supply for LCD drive
V_{LC1} to V_{LC4}	Input	Power supply for LCD drive
V_{DD}, V_{SS}	Input	Power supply and ground pins $V_{DD} = 5.0V \pm 10\%$, $V_{SS} = 0V$
$\overline{RST}$	Input	Reset : $\overline{RST}$ = L→Reset state
LE1 to LE5	Output	LED Enable outputs
OSC1, OSC2	—	When using the internal clock oscillator, connect a resistor between OSC1 and OSC2. When using an external clock, connect the clock to OSC1 and leave OSC2 open.
V_{OUT1}, V_{OUT2}	Output	DC-DC outputs using
C_1 to C_4	—	Connect capacitors for DC-DC converter.

FUNCTIONAL DESCRIPTION OF EACH BLOCK

- Register

The JT6C30-AS has seven 8-bit registers. The registers are the Instruction Register (IR), the Data Register (DR), and five LED control data registers (LER1 to LER5).
The IR holds an instruction code, a DD RAM address data, or a CG RAM address data.
The DR temporarily holds the data that is to be written into the DD RAM or the CG RAM. The data in DR are automatically written into the DD RAM or the CG RAM.
The LER1 to LER5 registers hold the data for controlling the LED.
The relation between the Register Select signal (RS) and operation is shown in Fig. 1.

RW	RS	OPERATION
0	0	Write into IR
0	1	Write into DR
1	0	Read Busy flag and Address Counter
1	1	Read from DR

Fig. 1

- Address Counter (AC)

The JT6C30-AS has a 7-bit Address Counter. The Address Counter points to an address in DD RAM or CG RAM, register code or to the cursor position. The Set DD RAM, CG RAM Address or Register Code instruction specifies which type of address Address Counter contains. The Address Counter is automatically incremented (or decremented) after the data has been written or read.

- Display data RAM (DD RAM)

This display data RAM (DD RAM) stores the display data as 8-bit character codes.
Its capacity is 80 characters × 8 bits. The relation between the DD RAM address and the display position is as shown below.
The DD RAM address corresponds to a HEX code as shown in Fig. 2.

	MSB						LSB
AC	DB6	DB5	DB4	DB3	DB2	DB1	DB0

Example : When DD RAM address = 4CH

MSB						LSB
1	0	0	1	1	0	0
4			C			

Fig. 2

(1) The relation between the DD RAM address and the display position in 1-Line Display mode. (N = 0, H = 0)

1	2	3	4	5		79	80	← Display position
00	01	02	03	04	----------	4E	4F	← DD RAM address

a) Using one JT6C30-AS, the first 10 characters are displayed as shown below.

1	2	3	4	5	6	7	8	9	10
00	01	02	03	04	05	06	07	08	09

b) When a Display Shift operation is executed, the relation between the DD RAM address and the display position is as shown below.

	1	2	3	4	5	6	7	8	9	10
Left shift display	01	02	03	04	05	06	07	08	09	0A

	1	2	3	4	5	6	7	8	9	10
Right shift display	4F	00	01	02	03	04	05	06	07	08

(2) The relation between the DD RAM address and the display position in 2-Line Display mode (N = 1, H = 0)

	1	2	3	4		39	40	← Display position
1st Line	00	01	02	03	----------	26	27	← DD RAM address
2nd Line	40	41	42	43	----------	66	67	

(Note) The DD RAM address of the 2nd Line is not the next address after the last address of the 1st Line.

a) Using one JT6C30-AS, the first 20 characters (10 characters × 2 lines) are displayed as shown below.

	1	2	3	4	5	6	7	8	9	10
1st Line	00	01	02	03	04	05	06	07	08	09
2nd Line	40	41	42	43	44	45	46	47	48	49

b) When a Display Shift operation is executed, the relation between the DD RAM address and the display position is as shown below.

Left shift display

	1	2	3	4	5	6	7	8	9	10
	01	02	03	04	05	06	07	08	09	0A
	41	42	43	44	45	46	47	48	49	4A

Right shift display

	1	2	3	4	5	6	7	8	9	10
	27	00	01	02	03	04	05	06	07	08
	67	40	41	42	43	44	45	46	47	48

(3) The relation between the DD RAM address and the display position in 4-line Display mode (N = 0, H = 1)

	1	2	3	4		19	20	← Display position
1st Line	00	01	02	03	----------	12	13	
2nd Line	20	21	22	23	----------	32	33	← DD RAM address
3rd Line	40	41	42	43	----------	52	53	
4th Line	60	61	62	63	----------	72	73	

(Note) The DD RAM address of the 2nd-line is not the next address after the last address of the 1st line.

a) Using one JT6C30-AS, the first 40 characters (10 characters × 4 lines) are displayed as shown below.

	1	2	3	4	5	6	7	8	9	10
1st Line	00	01	02	03	04	05	06	07	08	09
2nd Line	20	21	22	23	24	25	26	27	28	29
3rd Line	40	41	42	43	44	45	46	47	48	49
4th Line	60	61	62	63	64	65	66	67	68	69

b) When a Display Shift operation is executed, the relation between the DD RAM address and the display position is as shown below.

Left shift display

1	2	3	4	5	6	7	8	9	10
01	02	03	04	05	06	07	08	09	0A
21	22	23	24	25	26	27	28	29	2A
41	42	43	44	45	46	47	48	49	4A
61	62	63	64	65	66	67	68	69	6A

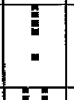
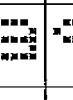
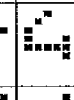
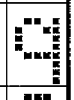
Right shift display

1	2	3	4	5	6	7	8	9	10
13	00	01	02	03	04	05	06	07	08
33	20	21	22	23	24	25	26	27	28
53	40	41	42	43	44	45	46	47	48
73	60	61	62	63	64	65	66	67	68

- Character generator ROM (CG ROM)

  The character generator ROM is used to generate the character patterns (5 × 10 dots × 240 characters) from the 8-bit character codes. The relation between the character codes and character patterns is as shown overleaf.

RELATION BETWEEN CHARACTER CODES AND CHARACTER PATTERN (CG ROM type 0000)

HIGHER 4 BITs / LOWER 4 BITs	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
XXXX0000	CGRAM (0)															
XXXX0001	(1)															
XXXX0010	(2)															
XXXX0011	(3)															
XXXX0100	(4)															
XXXX0101	(5)															
XXXX0110	(6)															
XXXX0111	(7)															
XXXX1000	(0)															
XXXX1001	(1)															
XXXX1010	(2)															
XXXX1011	(3)															
XXXX1100	(4)															
XXXX1101	(5)															
XXXX1110	(6)															
XXXX1111	(7)															

- Character generator RAM (CG RAM)

  the character generator RAM is used to display the user's own original character patterns (5×7 dots×8 types or 5×10 dots×4 types)
  The relation between the character codes and the CG RAM address and character patterns is as shown in Fig. 3 and Fig. 4

  (1) For 5×7-dot character patterns

CHARACTER CODES (DD RAM DATA)									CG RAM ADDRESS						CHARACTER PATTERNS (CG RAM DATA)								
7	6	5	4	3	2	1	0		5	4	3	2	1	0	7	6	5	4	3	2	1	0
0	0	0	0	*	0	0	0		0	0	0	0	0	0	*	*	*	1	1	1	1	0
												0	0	1				1	0	0	0	1
												0	1	0				1	0	0	0	1
												0	1	1				1	1	1	1	0
												1	0	0				1	0	0	0	1
												1	0	1				1	0	0	0	1
												1	1	0				1	1	1	1	0
												1	1	1	*	*	*	0	0	0	0	0
0	0	0	0	*	0	0	1		0	0	1	0	0	0	*	*	*	0	1	1	1	1
												0	0	1				1	0	0	0	0
												0	1	0				1	0	0	0	0
												0	1	1				0	1	1	1	0
												1	0	0				0	0	0	0	1
												1	0	1				0	0	0	0	1
												1	1	0				1	1	1	1	0
												1	1	1	*	*	*	0	0	0	0	0
												0	0	0	*	*	*	1	1	1	1	1
												0	0	1				0	0	1	0	0
0	0	0	0	*	1	1	1		1	1	1	0	1	1				0	0	1	0	0
												1	0	0				0	0	1	0	0
												1	0	1				0	0	1	0	0
												1	1	0				0	0	1	0	0
												1	1	1	*	*	*	0	0	0	0	0

Character Pattern Example (1)

← Cursor Position

Character Pattern Example (2)

← Cursor Position

Fig. 3

* : Invalid

(Note 1) Character code bit 0 to bit 2 correspond to CG RAM address bit 3 to bit 5.
(Note 2) Bit 0 to bit 2 of the CG RAM address indicate the row within the character bit map. The 8th row (the bottom row) corresponds to the cursor position on the LCD display. Normally the 8th row should be blank (all 0s), otherwise the lowest line of the character will be obscured when used with the cursor.
(Note 3) Character pattern line positions correspond to CG RAM data bit 0 to bit 4. CG RAM data bit 5 to bit 7 is not used for display; the data can be used for general RAM data.
(Note 4) If bit 4 to bit 7 are all 0, a CG RAM character is indicated. The value of bit 3 does not matter. Character codes 00H and 08H select the same character.
(Note 5) 1 : ON, 0 : OFF

(2) For 5 × 10-dot character patterns

CHARACTER CODES (DD RAM DATA) 7 6 5 4 3 2 1 0	CG RAM ADDRESS 5 4 3 2 1 0	CHARACTER PATTERNS (CG RAM DATA) 7 6 5 4 3 2 1 0	
0 0 0 0 * 0 0 *	0 0 0 0 0 0	* * * 0 0 0 1 0	Character Pattern Example
	0 0 0 0 1	* * * 0 0 0 0 0	
	0 0 1 0	* * * 0 0 1 1 0	
	0 0 1 1	* * * 0 0 0 1 0	
	0 1 0 0	* * * 0 0 0 1 0	
	0 1 0 1	* * * 0 0 0 1 0	
	0 1 1 0	* * * 0 0 0 1 0	
	0 1 1 1	* * * 0 0 0 1 0	
	1 0 0 0	* * * 1 0 0 1 0	
	1 0 0 1	* * * 0 1 1 0 0	
	1 0 1 0	* * * 0 0 0 0 0	← Cursor Position
	1 0 1 1	* * * * * * * *	
	1 1 0 0	* * * * * * * *	
	1 1 0 1	* * * * * * * *	
	1 1 1 0	* * * * * * * *	
	1 1 1 1	* * * * * * * *	
	0 0 0 0	* * *	
	0 0 0 1	* * *	
	0 0 1 0	* * *	
0 0 0 0 * 1 1 *	1 1 1 0 0 0		
	1 0 0 1		
	1 0 1 0	* * *	
	1 0 1 1	* * * * * * * *	
	1 1 0 0	* * * * * * * *	
	1 1 0 1	* * * * * * * *	
	1 1 1 0	* * * * * * * *	
	1 1 1 1	* * * * * * * *	* : Invalid

Fig. 4

(Note 1) Character code bit 1 and bit 2 correspond to CG RAM address bit 4 and bit 5.

(Note 2) Bit 0 to bit 3 of the CG RAM address indicate the row within the character bit map. The 11th row corresponds to the cursor position on the LCD display. Normally the 11th row should be blank (all 0s), otherwise the lowest line of the character will be obscured when used with the cursor. Lines 12 to 16 are not used for display data and can be used for general RAM data.

(Note 3) If bit 4 to bit 7 are all 0, a CG RAM character is indicated. The values of bits 0 and 3 do not matter. Character codes 00H, 01H, 08H and 09H all select the same character.

(Note 4) 1 : ON, 0 : OFF

- Timing generation circuit

  The timing generation circuit generates timing signals for operating internal circuits such as the DD RAM, CG ROM and CG RAM.
  The circuit is designed so that access by the MPU does not disturb the display. When data is written to the DD RAM, only the portion of RAM being written to is affected.
  This circuit also generates timing signals which operate the extension drive (e.g. the T6B23).
  The relation between the timing singals in 1-Line Display mode is as shown below.

Fig. 5

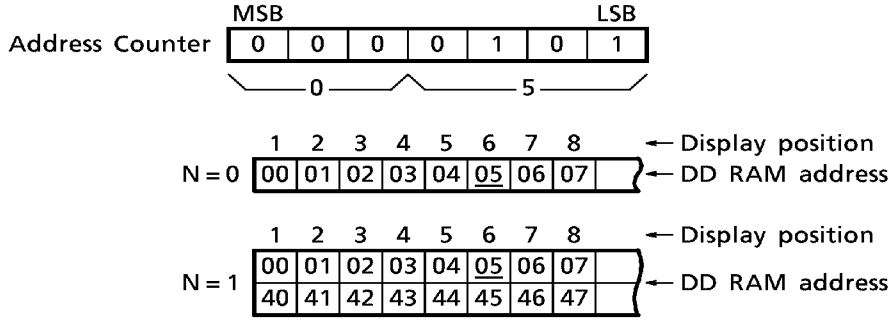
(Note1) SEG1 to SEG50 Data for the JT6C30-AS
SEG51 to SEG400 Data for the extension driver
(Note2) In 2-Line Display mode, "SEG400 Data" changes to "SEG200 Data".
In 4-Line Display mode, "SEG400 Data" changes to "SEG100 Data".

- LCD driver circuit

  The LCD drive circuit consists of 16 row drivers and 40 column drivers. When the character font type and the number of lines have been selected by the appropriate command, the valid row drivers automatically output drive waveforms, and the other row drivers output OFF waveforms.

- Cursor / blink display control circuit

  This circuit generates the cursor or blink display. The cursor or blink is displayed in the digit which corresponds to the DD RAM address set in the Address Counter.
  When the Address Counter is set to 05H, the cursor is displayed as shown below.



  (Note) The cursor or blink display is also displayed when the CG RAM address is set in the Address Counter. In this case the cursor or blink is displayed regardless of the DD RAM address.

- Reset

  When $\overline{RST}$ = L, the JT6C30-AS is reset and commands (1) to (4) are automatically executed. If a hard reset is not used, the MPU should execute commands (1) to (4).

  (1) Display Clear

  (2) Function Set ..... BL = 1 : The blink is displayed by switching between all dots ON and the displayed characters.
  ..... N = 0, H = 1 : 4-line display
  F = 0 : 5 × 7-dot character font

  (3) Entry Mode Set ..... I / D = 1 : + 1
  S = 0 : No Shift

  (4) Display ON / OFF Control ... D = 0 : Display OFF
  C = 0 : Cursor OFF
  B = 0 : Blink OFF

- Key matrix, LED control circuit

  This control circuit generates key scan signals and LED control signals. The key data that are input to the SWC1 to SWC10 are written in the Scan Data Register at the timing of the key scan signal. The SWS1 to SWS8 output the key scan signals and the LED data signals. LE1 to LE5 output the LED Enable signals.
  The JT6C30-AS controls an 8×5 LED matrix using LED data signals and Enable signals.
  The key scan signals and the LED control signals are shown in Fig. 6.

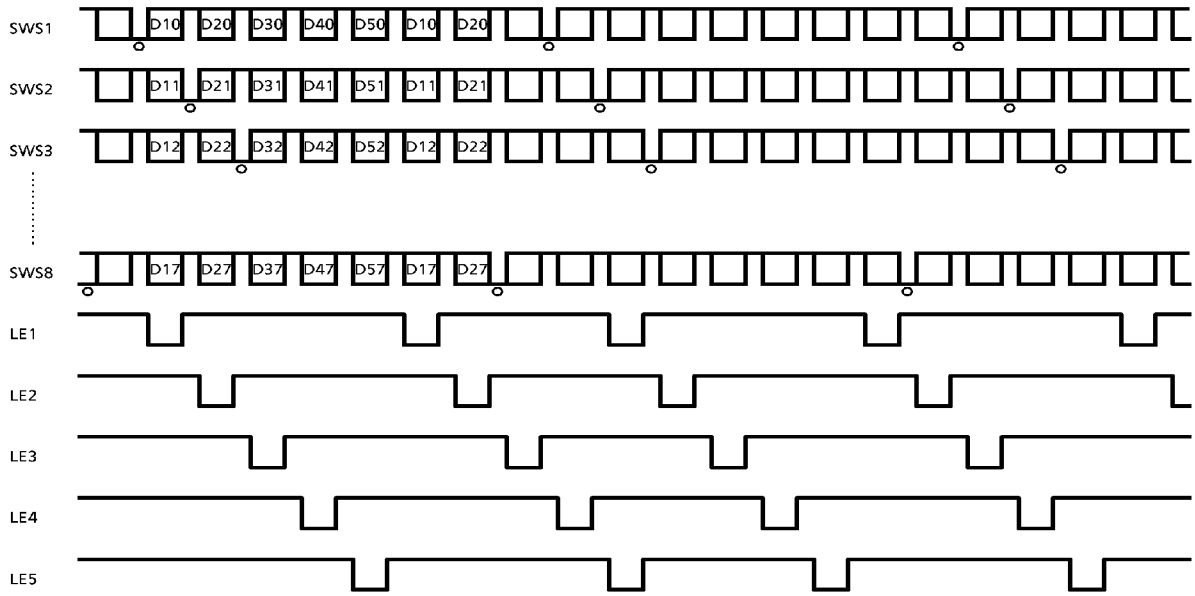


Fig. 6

(Note) D : LED control signals
1) D10 to D17 : The data on each bit of the LER1
2) D20 to D27 : The data on each bit of the LER2
3) D30 to D37 : The data on each bit of the LER3
4) D40 to D47 : The data on each bit of the LER4
5) D50 to D57 : The data on each bit of the LER5
° : Key scan signal

The structure of the 8×10-key scan matrix and the 8×5 LED matrix is shown in Fig. 7

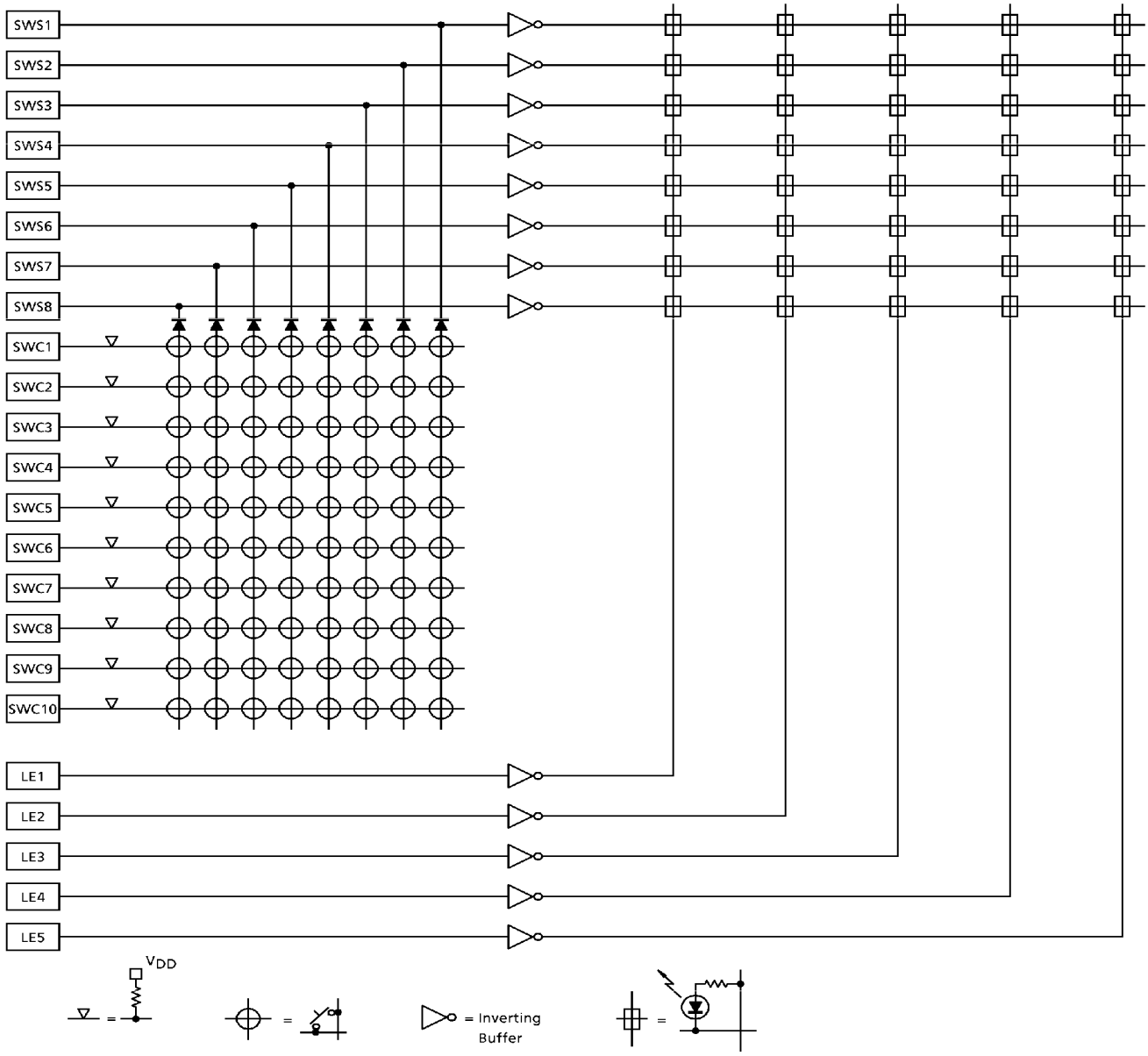
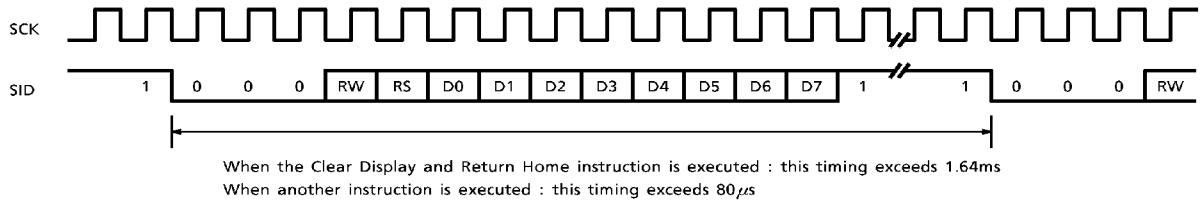


Fig. 7

- Interface to MPU

(1) Input data format

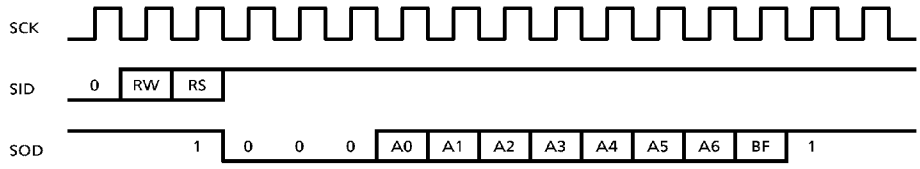


When the Clear Display and Return Home instruction is executed : this timing exceeds 1.64ms
When another instruction is executed : this timing exceeds 80μs

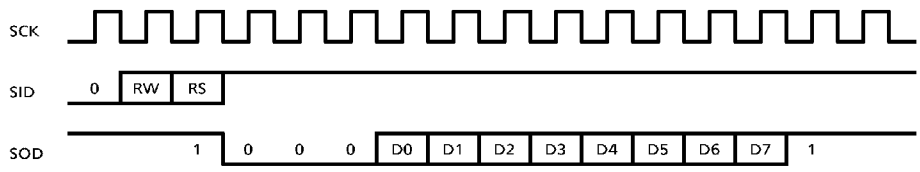
(2) Output data format

When the RW bit is 1, SOD outputs the Busy flag (BF), DD RAM data, CG RAM data, LED data, key scan data and port data.

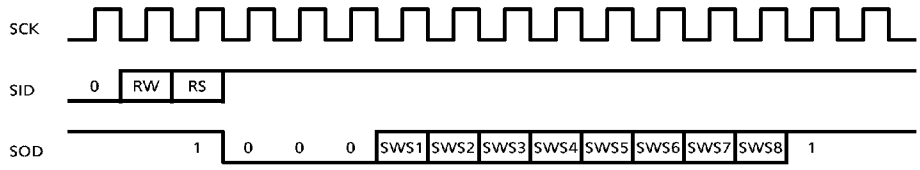
a) Busy flag (BF)



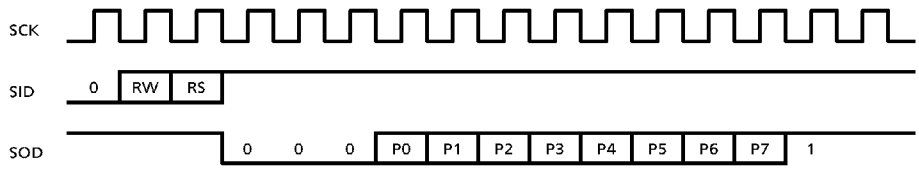
b) DD RAM data or LED data (8-bit)



c) Scan Data Register data (8-bit)



d) Port data (input : 4-bit, output : 4-bit)



(Note) P0 to 3 : Input port data
P4 to 7 : Output port data set beforehand

INSTRUCTION

The MPU can directly control seven registers. The registers are the Instruction register (IR), Data register (DR) and five LED control data registers (LER1 to LER5).

While the JT6C30-AS is executing an instruction, it cannot execute any other instructions (except for the Read Busy flag and Address instruction). The Busy flag is maintained at 1 (Busy state) until the instruction completes. Thus the MPU must check that the Busy flag is 0 (Not Busy state) before sending the next instruction.

If the MPU sends an instruction to the JT6C30-AS without performing a Busy check, the MPU must wait the execution time of the instruction before sending the next instruction.

DESCRIPTION OF INSTRUCTIONS

INPUT (SID)

INSTRUC-TION	CODE										DESCRIPTION		EXECUTION TIME f_{OSC} = 250kHz (MAX.)
	RW	RS	D7	D6	D5	D4	D3	D2	D1	D0			
Clear Display	0	0	0	0	0	0	0	0	0	1	Clears all display data and sets the DD RAM address to 00H.		1.64ms
Return Home	0	0	0	0	0	0	0	0	1	*	Sets the DD RAM address 00H and returns the display to home position. The contents of the DD RAM do not change.		1.64ms
Set Entry Mode	0	0	0	0	0	0	0	1	I / D	S	Sets cursor shift direction and display shift. These operations are executed when data is written.		40μs
Display ON / OFF Control	0	0	0	0	0	0	1	D	C	B	Sets ON / OFF for entire display (D), cursor ON / OFF (C), cursor position blink (B)		40μs
Cursor / Display shift	0	0	0	0	0	1	S / C	R / L	CRS	*	Shifts cursor and display without changing DD RAM contents		40μs
Set Function	0	0	0	0	1	BL	N	F	H	T	Sets blink mode (BL), sets number of display lines (N, H), character font (F), and test mode (T)		40μs
Set the CG RAM Address	0	0	0	1	CG RAM Address						Sets the CG RAM Address.	CRS = 0	40μs
Set Register Code					*	*	Register Code				Sets the register code.	CRS = 1	40μs
Set the DD RAM Address	0	0	1	DD RAM Address							Sets the DD RAM Address		40μs
Write Data to the CG RAM or DD RAM	0	1	Write Data								Writes data into the CG RAM or DD RAM		46μs
Write LED Data	0	1	Write LED Data								Writes data into the LED data registers (LER1 to LER5) or writes data into the output port		0μs
			Write Port Data		*								

* : Invalid

INSTRUC-TION	CODE										DESCRIPTION	EXECUTION TIME f_{OSC} = 250 kHz (max)
	RS1	RS2	D7	D6	D5	D4	D3	D2	D1	D0		
Read Busy Flag and Address	1	0	*								Reads Busy Flag (BF) and DD RAM Address	0μs
Read Data	1	1	*								Reads DD RAM data, CG RAM data, key scan data or port data	0μs

* : Invalid

OUTPUT (SOD)

INSTRUC-TION	OUTPUT DATA									DESCRIPTION	EXECUTION TIME f_{OSC} = 250kHz (MAX.)
		D7	D6	D5	D4	D3	D2	D1	D0		
Read Busy Flag and Address	0 0 0	BF	A6	A5	A4	A3	A2	A1	A0	Reads Busy Flag (BF) and DD RAM Address	0μs
Read DD RAM Data	0 0 0	D7	D6	D5	D4	D3	D2	D1	D0	Reads DD RAM data or LED data	0μs
Read Key Scan Data	0 0 0	SWS8	SWS7	SWS6	SWS5	SWS4	SWS3	SWS2	SWS1	Reads key scan data	0μs
Read Port Data	0 0 0	P7	P6	P5	P4	P3	P2	P1	P0	Reads Port data	0μs
—		I / D = 1 : Increment I / D = 0 : Decrement S = 1 : Display Shift On S / C = 1 : Display Shift S / C = 0 : Cursor Shift R / L = 1 : Shift to the Right R / L = 0 : Shift to the Left CRS = 0 : CG RAM Address is Valid CRS = 1 : Register Code is Valid BL = 1 : Display Blink on (all dots on) BL = 0 : Display Blink on (character-character reverse image) N = 0, H = 0 : 1-line Display N = 1, H = 0 : 2 -line Display N = 0, H = 1 : 4-line Display F = 1 : 5 × 10 dots F = 0 : 5 × 7 dots T = 1 : Enable Test Mode T = 0 : Cancel Test Mode									

REGISTER CODES

REGISTER NAME	CODE				
	D3	D2	D1	D0	(HEX)
LED Data Register (LER1)	0	0	0	0	0H
LED Data Register (LER2)	0	0	0	1	1H
LED Data Register (LER3)	0	0	1	0	2H
LED Data Register (LER4)	0	0	1	1	3H
LED Data Register (LER5)	0	1	0	0	4H
Scan Data Register (SWCR1)	0	1	0	1	5H
Scan Data Register (SWCR2)	0	1	1	0	6H
Scan Data Register (SWCR3)	0	1	1	1	7H
Scan Data Register (SWCR4)	1	0	0	0	8H
Scan Data Register (SWCR5)	1	0	0	1	9H
Scan Data Register (SWCR6)	1	0	1	0	AH
Scan Data Register (SWCR7)	1	0	1	1	BH
Scan Data Register (SWCR8)	1	1	0	0	CH
Scan Data Register (SWCR9)	1	1	0	1	DH
Scan Data Register (SWCR10)	1	1	1	0	EH
Port	1	1	1	1	FH

Fig. 8

- Clear display

	RW	RS	D7	----------						D0
Instruction Code	0	0	0	0	0	0	0	0	0	1

When the JT6C30-AS executes this instruction, code 20H (code 20H must be the "Space code") is written to every address in the DD RAM. This command resets the DD RAM address in the Address Counter.
The display is inhibited and the cursor or blink is moved to the left of the display. (In 2-Line Display mode, the cursor moves to the left of 1st line of the display.) The I/D of Entry mode is set to 0. The S of Entry mode does not change.

- Return home

	RW	RS	D7	----------						D0	
Instruction Code	0	0	0	0	0	0	0	0	1	*	* : invalid

The DD RAM address in the Address Counter is reset by this instruction, and the display shift is cancelled (this is known as returning to the home position). The contents of the DD RAM do not change. The cursor or blink moves to the extreme left of the display. (In 2-Line Display mode, the cursor moves to the extreme left of the 1st line of the display.)

- Set Entry mode

	RW	RS	D7	----------					D0
Instruction Code	0	0	0	0	0	0	0	1	I/D	S

I/D : The Address Counter is incremented (I/D = 1) or decremented (I/D = 0) after the data has been written to or read from DD RAM.
The same is true when date is written to or read from CG RAM.

S : If S = 1, the entire display is shifted left (I/D = 1) or right (I/D = 0) when data is written to the DD RAM. (The cursor position does not move)
If S = 0, the display is not shifted.

- Display ON/OFF control

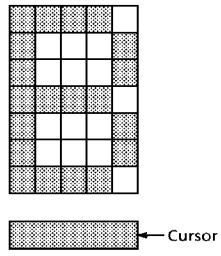
	RW	RS	D7	----------					D0
Instruction Code	0	0	0	0	0	0	1	D	C	B

D : D = 1, display is ON; D = 0, display is OFF.
When D is reset, the contents of the DD RAM do not change. Therefore, it can be displayed as before by setting D.

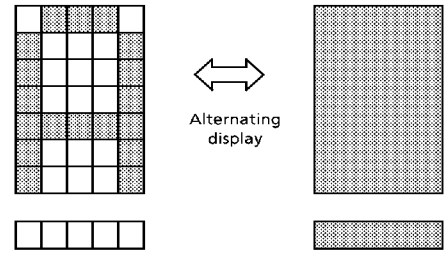
C : C = 1, cursor display is ON; C = 0, cursor display is OFF.
5 × 7-dot character font : cursor display uses 5 dots in the 8th line
5 × 10-dot character font : cursor display uses 5 dots in the 11th line

B : B = 1, character blink is ON (Same position of cursor position); B = 0, character blink is OFF.
Selectable blink : All dots on
Character-character reverse image.
Cursor and blink can operate at same time.
Blink period : Font 5 × 7-dot, f_{OSC} = 250kHz
(1 / 250k) × 5 × 80 × 8 × 32 = 409.6 (ms)

Font 5 × 10-dot, f_{OSC} = 250kHz
(1 / 250k) × 5 × 80 × 11 × 32 = 563.2 (ms)



(1) Cursor display example (5 × 7 dots)



(2) Blink display example (BL = 1)

- Cursor Display Shift

	RW	RS	D7	----------						D0	
Instruction Code	0	0	0	0	0	1	S/C	R/L	CRS	*	* : invalid

When this instruction is executed, the cursor or display is shifted to the right or left without display data being written.
In 2-Line Display mode, the cursor is shifted from the 40th digit of the 1st line to the 1st digit of the 2nd line.

S/C	R/L	CRS	FUNCTION	ADDRESS COUNTER (AC)
0	0	*	Shift the cursor to the left.	AC = AC – 1
0	1	*	Shift the cursor to the right.	AC = AC + 1
1	0	*	Shift the whole display to the left. The cursor follows the display shift direction.	AC = AC
1	1	*	Shift the whole display to the right. The cursor follows the display shift direction.	
0	*	0	CG RAM address is valid.	R/L = 0 : AC = AC – 1
		1	Register Code is valid.	R/L = 1 : AC = AC + 1

* : invalid

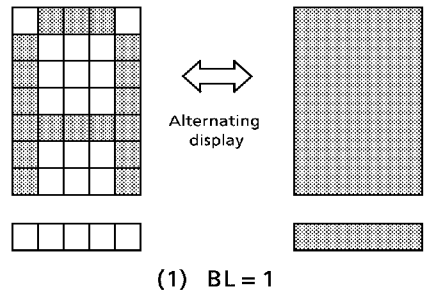
When S/C = 1, the contents of the Address Counter do not change.

- Set Function

	RW	RS	D7							D0
Instruction Code	0	0	0	0	1	BL	N	F	H	T

BL : BL = 1, Blink ON (All dots ON)
BL = 0, Blink ON (character reverse image-character)

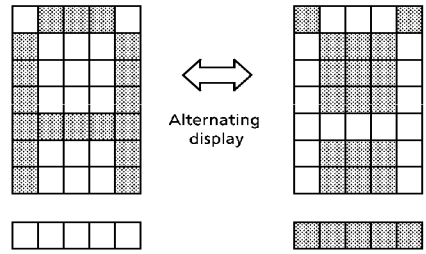
N	F	H	DISPLAY LINES	CHARACTER FONT	DUTY
0	0	0	1	5 × 7 dots	1/8
0	1	0	1	5 × 10 dots	1/11
1	0	0	2	5 × 7 dots	1/16
1	1	0	2	5 × 10 dots	1/22
0	0	1	4	5 × 7 dots	1/32



(1) BL = 1

T : T = 1, Test mode
Excuting this instruction, sets T = 0.

(Note) Execute this instruction first in a program before executing any other instructions.
After this instruction has been used once, it cannot be used again, except to change the Blink mode setting.



(2) BL = 0

- Set CG RAM Address or Register Code

	RW	RS	D7	----------						D0	
Instruction Code	0	0	0	1	A	A	A	A	A	A	CG RAM address
					*	*	A′	A′	A′	A′	Register Code

This instruction writes CG RAM address or register code data (e.g. AAAAAA (bin)) into the Address Counter.
The previous instruction (Cursor Display Shift) determines whether the data is a CG RAM address or register code.
Before this instruction is executed, Cursor Display Shift instruction must be executed.

- Set DD RAM Address

	RW	RS	D7	----------						D0
Instruction Code	0	0	1	A	A	A	A	A	A	A

This instruction writes the DD RAM address data (e.g. AAAAAAA (bin)) into the Address Counter.

- Write Data to DD RAM or CG RAM

	RW	RS	D7	----------						D0
Instruction Code	0	1	D	D	D	D	D	D	D	D

This instruction writes 8-bit data (e.g. DDDDDDDD (bin)) to DD RAM or CG RAM.
The previous instruction (Set DD RAM or CG RAM Address) determines whether the data will be written to DD RAM or CG RAM.
Before this instruction is executed, the Set DD RAM or CG RAM Address must be executed.
After the data has been written, the address is automatically incremented or decremented by 1.

- Write LED Data or Port Data

	RW	RS	D7	----------						D0	
Instruction Code	0	1	D	D	D	D	D	D	D	D	LED Data
			D′	D′	D′	D′	*	*	*	*	Port Data

This instruction writes 8-bit data (e.g. DDDDDDDD (bin)) to a LED Data register or Port.
When the data is written to port, the lower 4 bits (P0 to P3) is invalid.
The previous instruction (Set Register Code) determines whether the data will be written to a LED Data register (LER1 to LER5) or port.
The LER1 data controls eight LEDs using outputs SWS1 to SWS8 and LE1. Hence, the JT6C30-AS can control an 8×5 LED matrix using LER1 to LER5 data and LE1 to LE5.

- Read Busy Flag and DD RAM Address

	RW	RS	D7	----------						D0	
Instruction Code	1	0	*	*	*	*	*	*	*	*	* : invalid

This instruction makes SOD output the Busy flag and the DD RAM address.
The Busy flag indicates whether the JT6C30-AS can receive an instruction or not. The MPU must check the Busy flag before sending the next instruction to the JT6C30-AS.

- Read data from DD RAM, CG RAM or Register

	RW	RS	D7	----------						D0	
Instruction Code	1	1	*	*	*	*	*	*	*	*	* : invalid

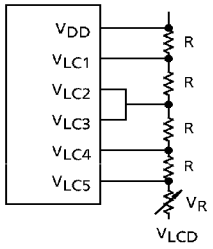
This instruction makes SOD output DD RAM data (8-bit), key scan data (8-bit) or port data (input: 4-bit, output: 4-bit).
The previous instruction (Set DD RAM, CG RAM Address or Register Code) determines whether the data will be read from DD RAM, CG RAM or a register (except for LER1 to LER5). Before this instruction is executed, the Set DD RAM, CG RAM Address or Register Code instruction must be executed.
After the data has been read, the address is automatically incremented or decremented by 1.

POWER SUPPLY FOR LCD DRIVE

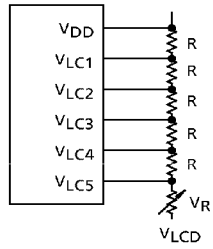
Various voltage levels must be applied to the JT6C30-AS's pins V_{LC1} to V_{LC5} to obtain the LCD drive waveforms.
The voltage levels vary according to the duty factor. The following table shows the relation.

DUTY FACTOR / POWER SUPPLY BIAS	1/8	1/16	1/32
	$\frac{1}{4}$	$\frac{1}{5}$	$\frac{1}{7}$
V_{LC1}	$V_{DD} - 1/4V_{LCD}$	$V_{DD} - 1/5V_{LCD}$	$V_{DD} - 1/7V_{LCD}$
V_{LC2}	$V_{DD} - 1/2V_{LCD}$	$V_{DD} - 2/5V_{LCD}$	$V_{DD} - 2/7V_{LCD}$
V_{LC3}	$V_{DD} - 1/2V_{LCD}$	$V_{DD} - 3/5V_{LCD}$	$V_{DD} - 5/7V_{LCD}$
V_{LC4}	$V_{DD} - 3/4V_{LCD}$	$V_{DD} - 4/5V_{LCD}$	$V_{DD} - 6/7V_{LCD}$
V_{LC5}	$V_{DD} - V_{LCD}$	$V_{DD} - V_{LCD}$	$V_{DD} - V_{LCD}$

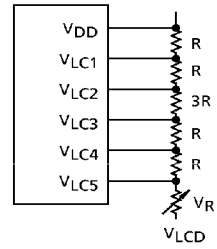
$V_{LCD} = V_{CC} - V_{LC5}$



(1) 1/4 Bias



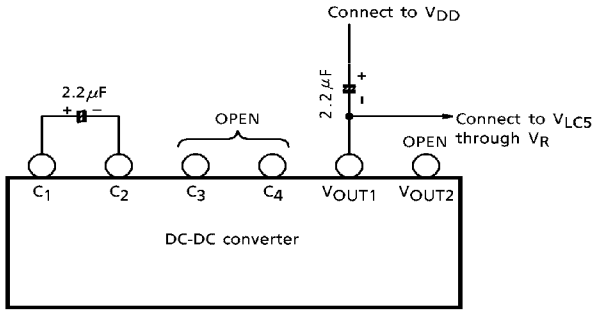
(2) 1/5 Bias



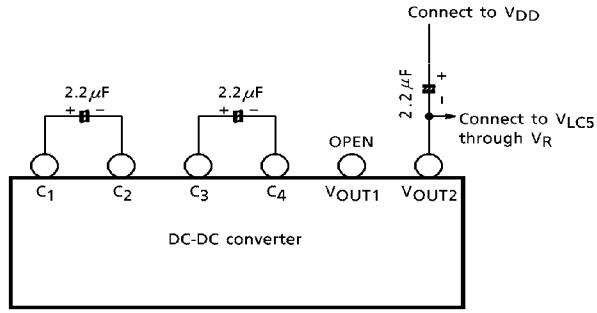
(3) 1/7 Bias

DC-DC CONVERTER (Doubler and tripler)

The JT6C30-AS has an on-chip DC-DC doubler and tripler.
A 2.2μF capacitor is recommended for this DC-DC converter.



(1) Doubler mode

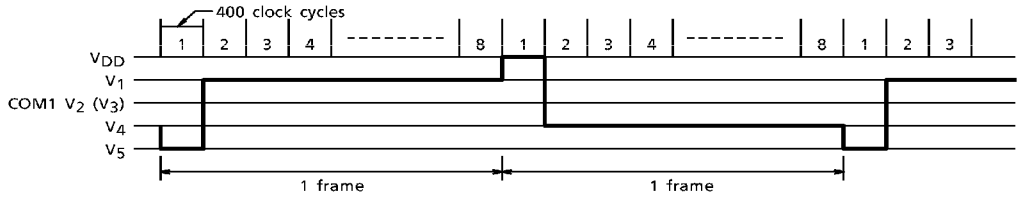


(2) Tripler mode

THE RELATION BETWEEN OSCILLATION FREQUENCY AND LCD FRAME FREQUENCY

LCD frame frequency example (f_{OSC} = 250kHz)

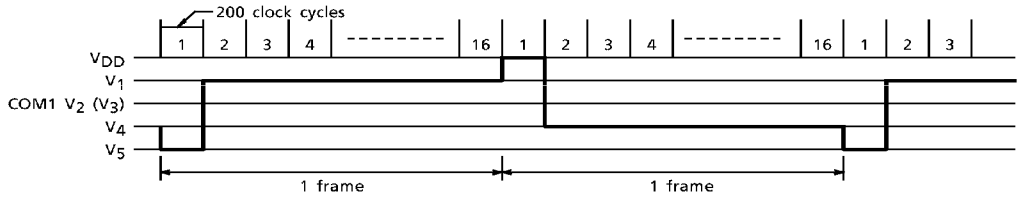
(1) 1 / 8 duty cycle



1 frame = 4 μs × 400 × 8 = 12800 μs = 12.8 ms

frame frequency = $\frac{1}{12.8 \text{ ms}}$ = 78.1 Hz

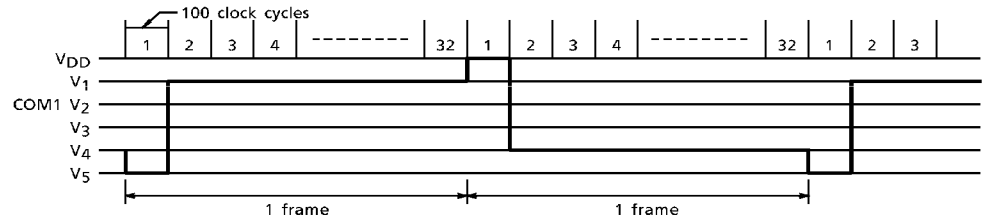
(2) 1 / 16 duty cycle



1 frame = 4 μs × 200 × 16 = 12800 μs = 12.8 ms

frame frequency = $\frac{1}{12.8 \text{ ms}}$ = 78.1 Hz

(3) 1 / 32 duty cycle



1 frame = 4 $\mu s \times 100 \times 32 = 12800\ \mu s = 12.8$ ms

frame frequency = $\frac{1}{12.8\ \text{ms}} = 78.1$ Hz

ABSOLUTE RATINGS (Ta = 25°C)

ITEM	SYMBOL	RATING	UNIT
Power Supply Voltage (1)	V_{DD}	− 0.3 to 7.0	V
Power Supply Voltage (2)	V_{LC1} to V_{LC5}	V_{DD} − 13.5 to V_{DD} + 0.3	V
Input Voltage	V_{IN}	− 0.3 to V_{DD} + 0.3	V
Operating Temperature	T_{opr}	− 20 to 75	°C
Storage Temperature	T_{stg}	− 55 to 125	°C

(Note 1) All voltage values are referenced to $V_{SS} = 0V$

(Note 2) Ensure that the following condition is always maintained.

$V_{DD} \geqq V_{LC1} \geqq V_{LC2} \geqq V_{LC3} \geqq V_{LC4} \geqq V_{LC5}$

ELECTRICAL CHARACTERISTICS

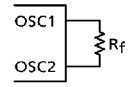
DC CHARACTERISTICS

TEST CONDITIONS (Unless otherwise noted, V_{DD} = 5.0V ± 10%, V_{SS} = 0V, Ta = − 20 to 75°C)

ITEM		SYMBOL	TEST CIR-CUIT	TEST CONDITIONS	MIN	TYP.	MAX	UNIT	PIN NAME
Operating Voltage (1)		V_{DD}	—	—	4.5	—	5.5	V	—
Operating Voltage (2)		V_{LCD}	—	$V_{LCD} = V_{DD} - V_{LC5}$	4.5	—	11.0	V	—
Input Voltage (1)	H Level	V_{IH1}	—	—	V_{DD} − 1.0	—	V_{DD}	V	SCK, SID $\overline{RST}$, P0 to P3
	L Level	V_{IL1}	—	—	0	—	1.0	V	
Hyseterisis Voltage		V_H	—	—	—	0.7	—	V	SCK, SID $\overline{RST}$
Input Voltage (2)	H Level	V_{IH2}	—	—	V_{DD} − 1.2	—	V_{DD}	V	SWC1 to SWC10
	L Level	V_{IL2}	—	—	0	—	1.9	V	
Output Voltage (1)	H Level	V_{OH1}	—	I_{OH} = − 0.625mA	V_{DD} − 0.3	—	—	V	D, SCP LP, EO, FR
	L Level	V_{OL1}	—	I_{OL} = 0.625mA	—	—	0.3	V	
Output Voltage (2)	H Level	V_{OH2}	—	I_{OH} = − 250μA	V_{DD} − 0.8	—	—	V	SWS1 to SWS8, LE1 to LE5, SOD, P4 to P7
	L Level	V_{OL2}	—	I_{OL} = 2.0mA	—	—	0.4	V	
Row Output Resistance		RCOM	—	I_d = ± 50μA	—	—	20	kΩ	COM1 to 32
Column Output Resistance		RSEG	—	I_d = ± 50μA	—	—	30	kΩ	SEG1 to 50
Input Leakage Current		I_{IL}	—	V_{IN} = 0 to V_{DD}	—	—	1	μA	SCK, SID
Power Supply Current		I_{DD}	—	(Note 1)	—	500	700	μA	V_{DD}
Clock Oscillation Frequency		f_{osc}	—	(Note 2)	250	310	370	kHz	OSC1, OSC2
External Clock Frequency		f_{IN}	—	(Note 3)	125	250	370	kHz	OSC1
External Clock Duty		f_{Duty}	—	(Note 4)	45	50	55	%	OSC1
External Clock Rise Time		t_r	—	(Note 5)	—	—	200	ns	OSC1
External Clock Fall Time		t_f	—	(Note 5)	—	—	200	ns	OSC1
Output Voltage (Doubler Mode)		VUP2	—	(Note 6)	—	− 4.3	− 4.1	V	V_{OUT1}

(Note 1) Current Consumption : V_{DD} = 5.0V, internal clock (R_f = 91kΩ), f_{CE} = 4MHz, DC-DC converter in Doubler Mode

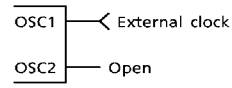
(Note 2) External R_f oscillation



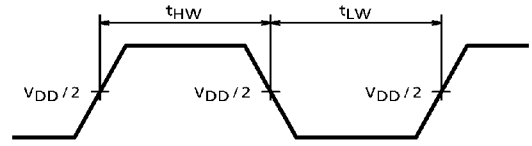
R_f = 91kΩ ± 2%

Oscillation frequency depends on OSC1 and OSC2 pin capacitance, therefore wiring must be as short as possible.

(Note 3) External clock operation

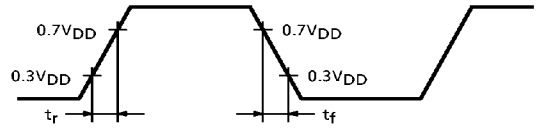


(Note 4) Applied to OSC1 pin



$f_{Duty} = t_{HW} / (t_{HW} + t_{LW}) \times 100$ (%)

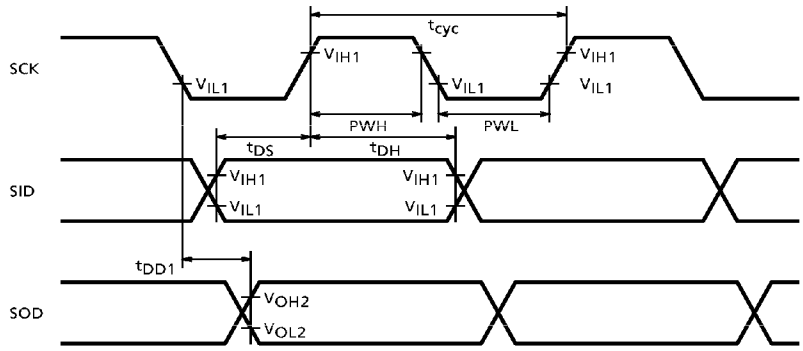
(Note 5) Applied to OSC1 pin



(Note 6) DC-DC converter in Doubler mode:
V_{DD} = 5.0V, internal clock (R_f = 91kΩ),
$C_1 - C_2$ = 2.2μF, $V_{DD} - V_{OUT1}$ = 2.2μF, Iload = 700μA, Ta = 90°C

AC CHARACTERISTICS

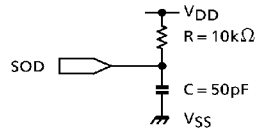
- Serial interface



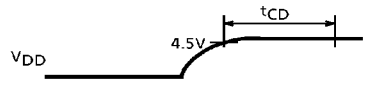
TEST CONDITION (V_{DD} = 5.0V ± 10%, V_{SS} = 0V, Ta = − 20 to 75°C)

ITEM		SYMBOL	MIN	TYP.	MAX	UNIT
SCK Cycle Time		t_{cyc}	333	4000	8000	ns
SCK Pulse Width	H Level	PWH	$\frac{t_{cyc}}{2} - 30$	—	—	ns
	L Level	PWL				
Data Set-up Time to SCK		t_{DS}	50	—	—	ns
Data Hold Time so SCK		t_{DH}	120	—	—	ns
Data Delay Time so SCK		t_{DD1}	—	—	120	ns

(Note) AC testing load circuit for SOD



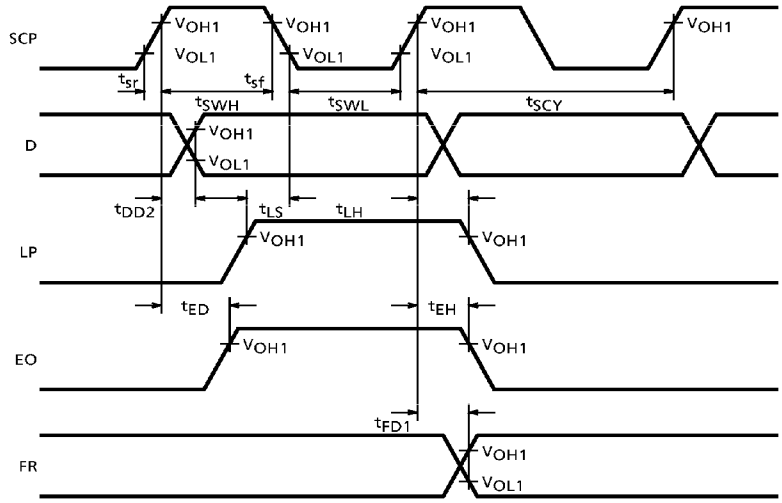
- Power-on sequence



TEST CONDITION (V_{SS} = 0V, Ta = − 20 to 75°C)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNIT
Command Disable Time	t_{CD}	—	—	15	ms

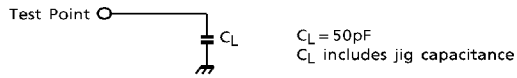
- Expansion driver interface
  (e.g. T6B23)



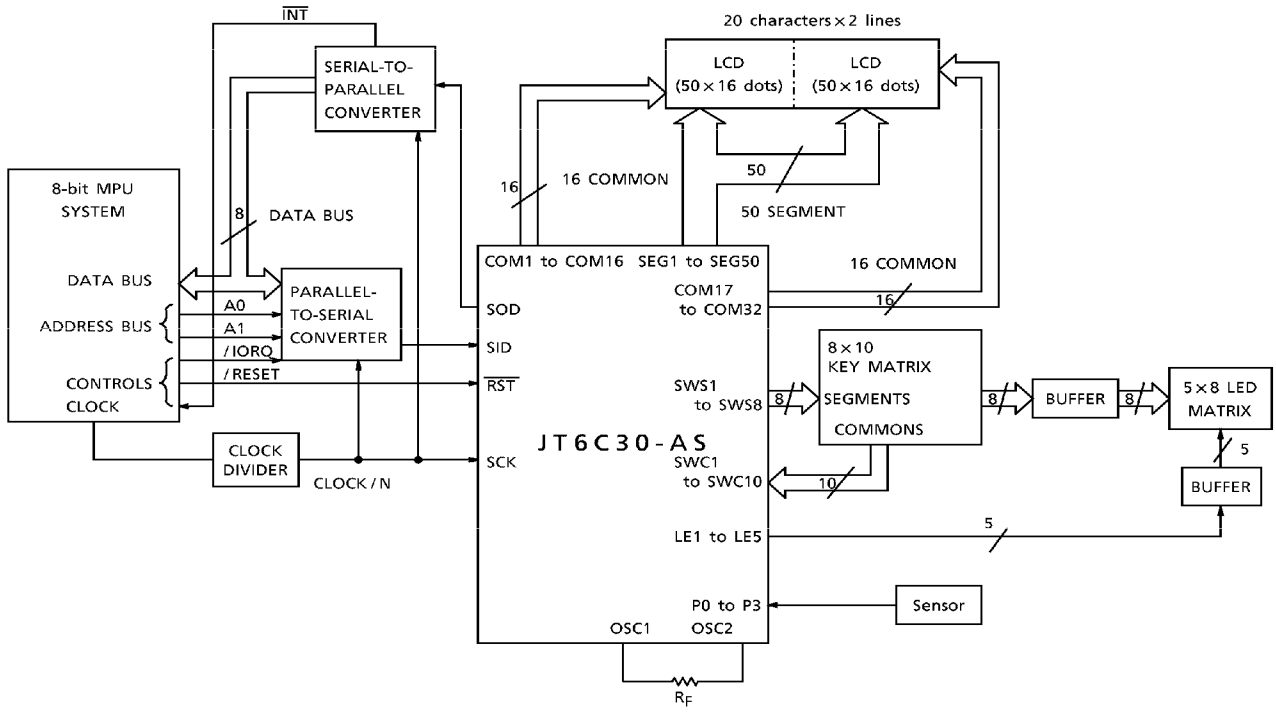
TEST CONDITIONS (V_{DD} = 5.0V ± 10%, V_{SS} = 0V, Ta = − 20 to 75°C)

PARAMETER	SYMBOL	MIN	MAX	UNIT
SCP Cycle Time	t_{SCY}	2000	—	ns
SCP Pulse Width	$t_{SWH, L}$	800	—	ns
SCP Rise and Fall Time	t_{sr}, t_{sf}	—	100	ns
Data Delay from SCP	t_{DD2}	—	100	ns
LP Set-up Time SCP	t_{LS}	− 120	0	ns
LP Hold Time from SCP	t_{LH}	− 100	0	ns
EO Delay Time from SCP	t_{ED}	—	100	ns
EO Hold Time from SCP	t_{EH}	− 100	0	ns
FR Delay Time from SCP	t_{FD1}	− 100	100	ns

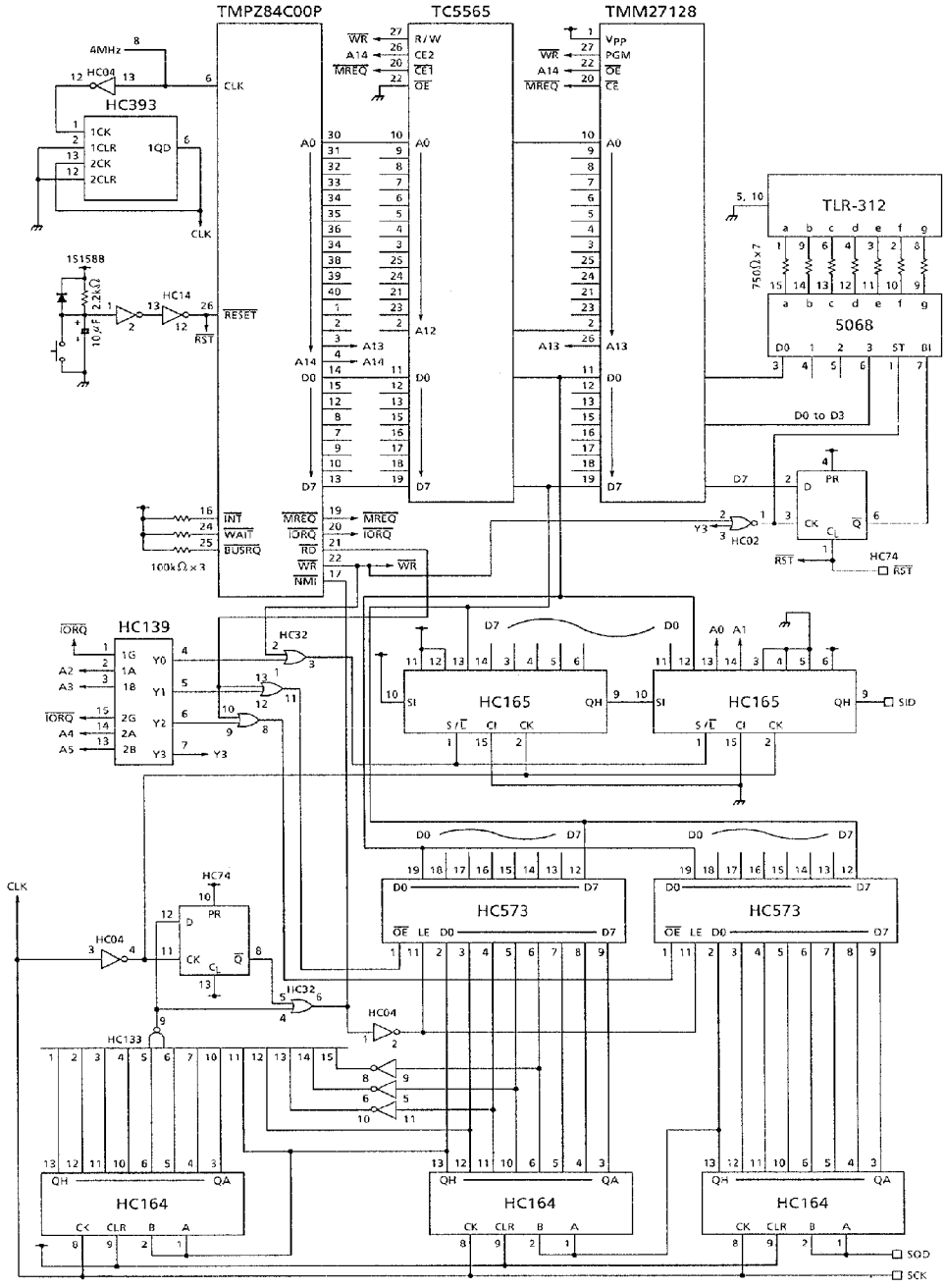
(Note) AC testing load circuit for interface timing

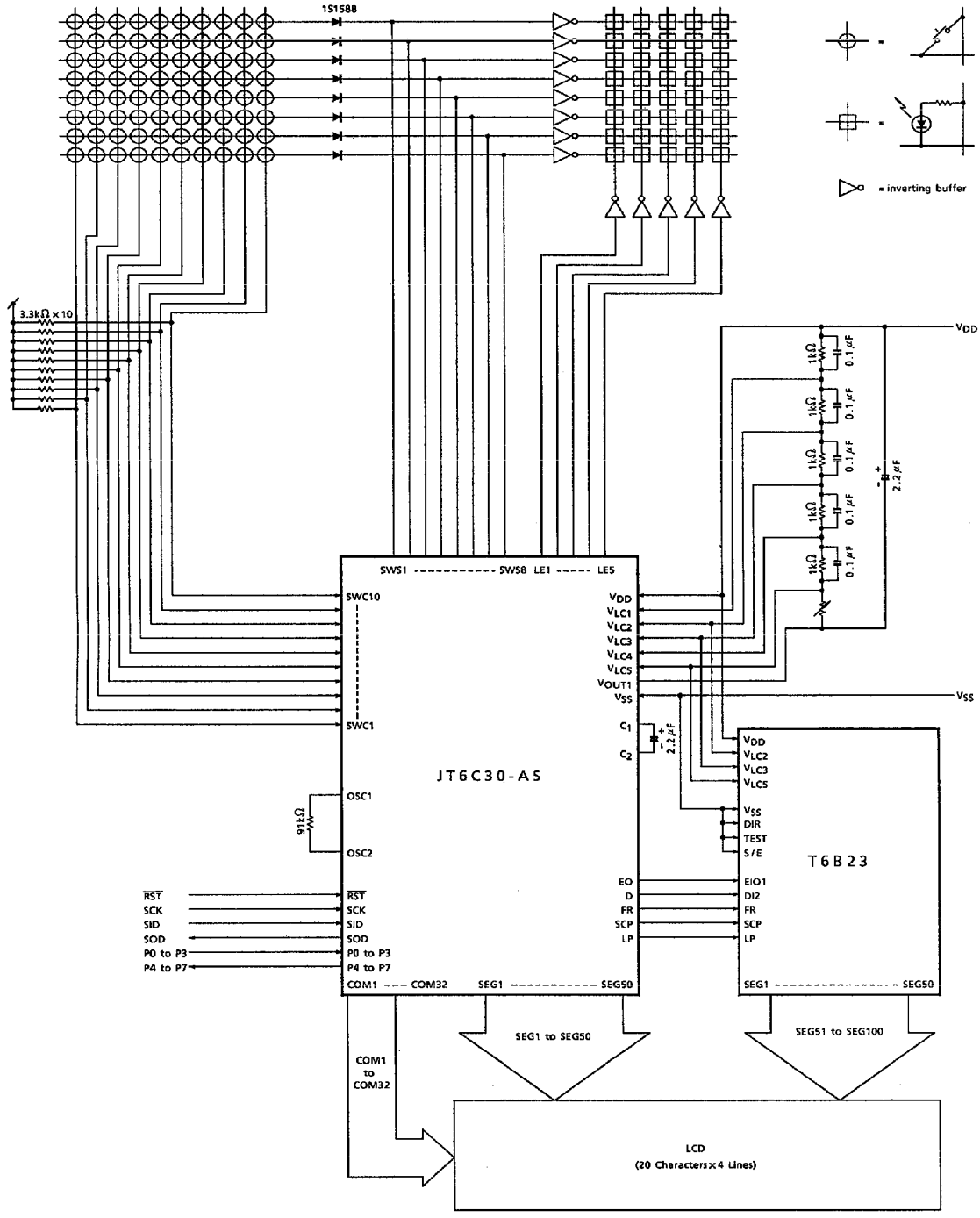


APPLICATION CIRCUIT



APPLICATION-A




1S1588
= inverting buffer
3.3kΩ×10
VDD
1kΩ
0.1μF
2.2μF
SWS1
SWS8
LE1
LE5
SWC10
SWC1
VDD
VLC1
VLC2
VLC3
VLC4
VLC5
VOUT1
VSS
C1
C2
JT6C30-AS
OSC1
91kΩ
OSC2
RST
SCK
SID
SOD
P0 to P3
P4 to P7
COM1
COM32
SEG1
SEG50
T6B23
EO
D
FR
SCP
LP
EIO1
DI2
DIR
TEST
S/E
SEG51 to SEG100
COM1 to COM32
LCD
(20 Characters×4 Lines)