

DESCRIPTION

The HYM536A414B is a 4M x 36-bit EDO mode CMOS DRAM module consisting of nine HY5117404B in 24/26 pin SOJ on a 72 pin glass-epoxy printed circuit board. 0.1 μ F and 0.01 μ F decoupling capacitor is mounted for each DRAM.

The HYM536A414BM/BSLM are Tin-Lead plated and HYM536A414BMG/BSLMG are Gold plated socket type Single In-line Memory Modules suitable for easy interchange and addition of 16M byte memory.

FEATURES

- Low power dissipation
Max. self-refresh 14.9mW (SL-part)
Max. battery back-up 24.8mW (SL-part)
Max. CMOS standby 19.8mW (SL-part)
49.5mW
Max. TTL standby 99.0mW

Speed	Power
50	7.18W
60	5.94W
70	4.95W

- Single power supply of 5V $\pm$ 10%
- TTL compatible inputs and outputs
- Fast access time

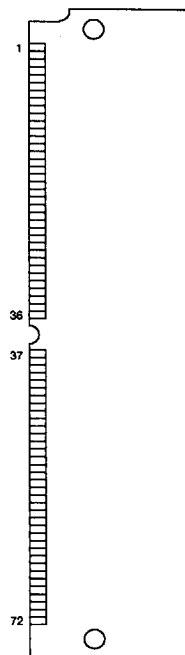
Speed	tRAC	tCAC	tHPC
50	50ns	13ns	20ns
60	60ns	15ns	25ns
70	70ns	18ns	30ns

- EDO mode operation
- CAS-before-RAS, RAS-only, Hidden refresh and Self-refresh
- 2048 refresh cycles / 256ms (SL-part)
2048 refresh cycles / 32ms

PIN DESCRIPTION

RAS0	Row Address Strobe
CAS0	Column Address Strobe
WE	Write Enable
OE	Output Enable
A0-A10	Address Input
DQ0-DQ35	Data Input/Output
PD1-PD5	Presence Detect
Vcc	Power (+ 5V)
Vss	Ground

PIN CONNECTION



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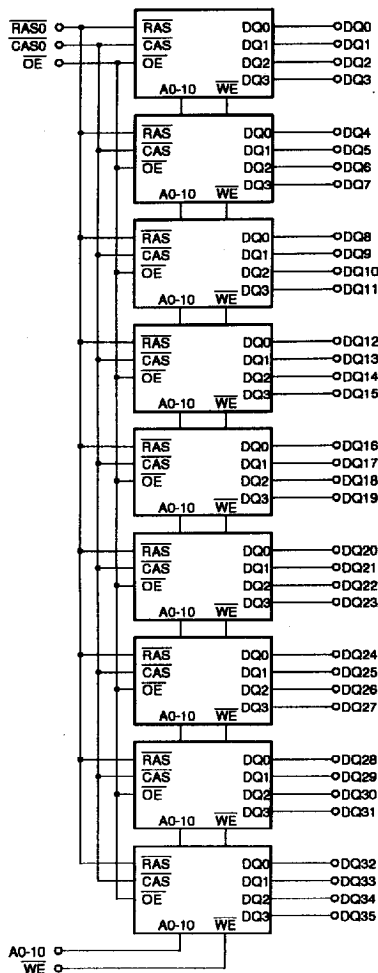
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PIN NAME

#	NAME	#	NAME
1	Vss	37	DQ19
2	DQ0	38	DQ20
3	DQ1	39	Vss
4	DQ2	40	CAS0
5	DQ3	41	A10
6	DQ4	42	NC
7	DQ5	43	NC
8	DQ6	44	RAS0
9	DQ7	45	NC
10	Vcc	46	DQ21
11	PD5	47	WE
12	A0	48	Vss
13	A1	49	DQ22
14	A2	50	DQ23
15	A3	51	DQ24
16	A4	52	DQ25
17	A5	53	DQ26
18	A6	54	DQ27
19	OE	55	DQ28
20	DQ8	56	DQ29
21	DQ9	57	DQ30
22	DQ10	58	DQ31
23	DQ11	59	Vcc
24	DQ12	60	DQ32
25	DQ13	61	DQ33
26	DQ14	62	DQ34
27	DQ15	63	DQ35
28	A7	64	NC
29	DQ16	65	NC
30	Vcc	66	NC
31	A8	67	PD1
32	A9	68	PD2
33	NC	69	PD3
34	NC	70	PD4
35	DQ17	71	NC
36	DQ18	72	Vss

BLOCK DIAGRAM



PRESENCE DETECT PIN

PIN	-50	-60	-70
PD1	Vss	Vss	Vss
PD2	NC	NC	NC
PD3	Vss	NC	Vss
PD4	Vss	NC	NC
PD5	Vss	Vss	Vss

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ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
TA	Ambient Temperature	0 to 70	°C
TSTG	Storage Temperature	-55 to 125	°C
VIN, VOUT	Voltage on Any Pin Relative to VSS	-1.0 to 7.0	V
VCC	Voltage on VCC Relative to VSS	-1.0 to 7.0	V
IOS	Short Circuit Output Current	50	mA
Pd	Power Dissipation	9	W

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(TA= 0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
VCC	Supply Voltage	4.5	5.0	5.5	V
VIH	Input High Voltage	2.4	-	VCC+ 1.0	V
VIL	Input Low Voltage	-1.0	-	0.8	V

NOTE : All voltages are referenced to VSS.

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DC CHARACTERISTICS

(TA= 0°C to 70°C, VCC= 5V± 10%, VSS= 0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED/ POWER	MIN.	MAX.	UNIT	NOTE
ILI	Input Leakage Current (Any Input Pin)	VSS≤ VIN≤ VCC+ 1.0, All other pins not under test= VSS		-90	90	μA	
ILO	Output Leakage Current (High Impedance State)	VSS≤ VOUT≤ VCC, RAS & CAS at VIH		-10	10	μA	
ICC1	VCC Supply Current, Operating	tRC= tRC (min.)	50 60 70	- - -	1305 1080 900	mA	1,2,3
ICC2	VCC Supply Current, TTL Standby	RAS & CAS at VIH, other inputs≥ VSS		-	18	mA	
ICC3	VCC Supply Current, RAS-only refresh	tRC= tRC (min.)	50 60 70	- - -	1305 1080 900	mA	1,3
ICC4	VCC Supply Current, EDO mode	tHPC= tHPC (min.)	50 60 70	- - -	1170 990 810	mA	1,2,3
ICC5	VCC Supply Current, CMOS Standby	RAS & CAS ≥ VCC-0.2V	SL-part	- -	9 3.6	mA	5
ICC6	VCC Supply Current, CAS-before-RAS refresh	tRC= tRC (min.)	50 60 70	- - -	1305 1080 900	mA	1,3
ICC7	VCC Supply Current, Battery Back Up (SL-part only)	tRC= 62.5μs, CAS= CBR cycling or 0.2V WE= VCC-0.2V A0-A10= VCC-0.2V or 0.2V DQ0-DQ35= VCC-0.2V, 0.2V, or open	tRAS≤ 300ns	-	2.7	mA	1,4,5
			tRAS≤ 1μs	-	4.5		
ICC8	VCC Supply Current Self Refresh (SL-part only)	RAS & CAS= VIL OE & WE & A0-A10= VCC-0.2V or 0.2V, DQ0-DQ35= VCC - 0.2V, 0.2V or open			2.7	mA	5
VOL	Output Low Voltage	IOL= 4.2mA		-	0.4	V	
VOH	Output High Voltage	IOH= -5mA		2.4	-	V	

NOTE :

1. ICC1, ICC3, ICC4, ICC6 and ICC7 depend on cycle rate.
2. ICC1, ICC3, ICC4, and ICC6 depend on output loading. Specified values are obtained with the output open.
3. ICC1 is specified as average current. for ICC1, ICC3 and ICC6, address can be changed maximum two times while RAS= VIL for ICC4, address can be changed maximum once while CAS= VIH.
4. Only tRAS(max.)= 1μs is applied to refresh of battery backup but tRAS(max.)= 10μs is applied to normal functional operation.
5. ICC5(max.)= 3.6mA, ICC7 and ICC8 are applied to SL-part only (HYM536A414BSLM/BSLMG).

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AC CHARACTERISTICS

(TA= 0°C to 70°C, VCC= 5V± 10%, VSS = 0V, unless otherwise noted.) NOTE : 1, 2, 3

#	SYMBOL	PARAMETER	HYM536A414B M-Series						UNT	NOTE
			-50		-60		-70			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	tRC	Random Read or Write Cycle Time	84	-	104	-	124	-	ns	
2	tRWC	Read-Modify-Write Cycle Time	113	-	137	-	160	-	ns	
3	tHPC	EDO Mode Cycle Time	20	-	25	-	30	-	ns	
4	tHPRWC	EDO Mode Read-Modify-Write Cycle Time	61	-	70	-	78	-	ns	
5	tRAC	Access Time from RAS	-	50	-	60	-	70	ns	4,9,10
6	tCAC	Access Time from CAS	-	13	-	15	-	18	ns	4,9
7	tAA	Access Time from Column Address	-	25	-	30	-	35	ns	4,10
8	tCPA	Access Time from CAS Precharge	-	30	-	35	-	40	ns	4
9	tCLZ	CAS to Output Low Impedance	3	-	3	-	3	-	ns	4
10	tCEZ	Output Buffer Turn-off Delay	3	13	3	15	3	18	ns	5
11	tT	Transition Time (Rise and Fall)	2	50	2	50	2	50	ns	3
12	tRP	RAS Precharge Time	30	-	40	-	50	-	ns	
13	tRAS	RAS Pulse Width	50	10K	60	10K	70	10K	ns	
14	tRASP	RAS Pulse Width (EDO Mode)	50	200K	60	200K	70	200K	ns	
15	tRSH	RAS Hold Time	13	-	15	-	18	-	ns	
16	tCSH	CAS Hold Time	40	-	45	-	50	-	ns	
17	tCAS	CAS Pulse Width	8	10K	11	10K	14	10K	ns	
18	tRCD	RAS to CAS Delay	18	37	20	45	20	52	ns	9
19	tRAD	RAS to Column Address Delay Time	10	25	15	30	15	35	ns	10
20	tCRP	CAS to RAS Precharge Time	5	-	5	-	5	-	ns	
21	tCP	CAS Precharge Time	8	-	10	-	12	-	ns	
22	tASR	Row Address Set-up Time	0	-	0	-	0	-	ns	
23	tRAH	Row Address Hold Time	8	-	10	-	10	-	ns	
24	tASC	Column Address Set-up Time	0	-	0	-	0	-	ns	
25	tCAH	Column Address Hold Time	10	-	10	-	10	-	ns	
26	tAR	Column Address Hold Time from RAS	50	-	50	-	50	-	ns	
27	tRAL	Column Address to RAS Lead Time	25	-	30	-	35	-	ns	
28	tRCS	Read Command Set-up Time	0	-	0	-	0	-	ns	
29	tRCH	Read Command Hold Time Referenced to CAS	0	-	0	-	0	-	ns	6
30	tRRH	Read Command Hold Time Referenced to RAS	0	-	0	-	0	-	ns	6
31	tWCH	Write Command Hold Time	8	-	10	-	10	-	ns	
32	tWCR	Write Command Hold Time from RAS	45	-	50	-	55	-	ns	
33	tWP	Write Command Pulse Width	8	-	10	-	10	-	ns	
34	tRWL	Write Command to RAS Lead Time	10	-	12	-	12	-	ns	
35	tCWL	Write Command to CAS Lead Time	10	-	12	-	12	-	ns	
36	tDS	Data-In Set-up Time	0	-	0	-	0	-	ns	7
37	tDH	Data-In Hold Time	10	-	10	-	10	-	ns	7
38	tDHR	Data-In Hold Time Referenced to RAS	50	-	50	-	50	-	ns	
39	tREF	Refresh Period (2048 cycles)	-	32	-	32	-	32	ms	
		SL-part	-	256	-	256	-	256	ms	12
40	tWCS	Write Command Set-up Time	0	-	0	-	0	-	ns	8

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AC CHARACTERISTICS

(continued)

continued)

#	SYMBOL	PARAMETER	HYM536A814B M-Series						UNIT	NOTE
			-50		-60		-70			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
41	tCWD	CAS to WE Delay Time	30	-	34	-	40	-	ns	8
42	tRWD	RAS to WE Delay Time	67	-	79	-	92	-	ns	8
43	tAWD	Column Address to WE Delay Time	42	-	49	-	57	-	ns	8
44	tCSR	CAS Set-up Time (CBR Cycle)	5	-	5	-	5	-	ns	
45	tCHR	CAS Hold Time (CBR Cycle)	10	-	10	-	10	-	ns	
46	tRPC	RAS to CAS Precharge Time	5	-	5	-	5	-	ns	
47	tCPT	CAS Precharge Time (CBR Counter Test)	15	-	20	-	25	-	ns	
48	tROH	RAS Hold Time Reference to OE	10	-	10	-	10	-	ns	
49	tOEA	OE Access Time	-	13	-	15	-	18	ns	
50	tOED	OE to Data Delay	13	-	15	-	18	-	ns	
51	tOEZ	Output Buffer Turn Off Delay Time from OE	3	13	3	15	3	18	ns	5
52	tOEH	OE Command Hold Time	13	-	15	-	18	-	ns	
53	tCPWD	WE Delay Time from CAS Precharge	47	-	54	-	62	-	ns	8
54	tRHCP	RAS Hold Time from CAS Precharge	30	-	35	-	40	-	ns	
55	tWRP	WE to RAS Precharge Time (CBR Cycle)	10	-	10	-	10	-	ns	
56	tWRH	WE to RAS Hold time (CBR Cycle)	10	-	10	-	10	-	ns	
57	tRASS	RAS Pulse Width (Self Refresh Cycle)	100	-	100	-	100	-	μs	
58	tRPS	RAS Precharge Time (Self Refresh Cycle)	110	-	130	-	150	-	ns	
59	tCHS	CAS Hold Time (Self Refresh Cycle)	-50	-	-50	-	-50	-	ns	
60	tDOH	Output Data Hold Time	3	-	3	-	3	-	ns	
61	tREZ	Output Buffer Turn-off Delay (RAS)	-	15	-	15	-	15	ns	5,15
62	tWEZ	Output Buffer Turn-off Delay (WE)	-	15	-	15	-	15	ns	5
63	tWPE	WE Pulse Width for Output Disable	10	-	10	-	10	-	ns	
64	tOEP	OE Pulse Width for Output Disable	10	-	10	-	10	-	ns	
65	tOCH	OE Low to CAS High Delay Time	0	-	0	-	0	-	ns	
66	tCHO	CAS High to OE High Hold Time	10	-	10	-	10	-	ns	
67	tWED	WE to Data Delay Time	15	-	15	-	15	-	ns	

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NOTE :

1. An initial pause of 200 μ s is required after power-up followed by 8 RAS cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 CAS-before-RAS initialization cycles instead of 8 RAS-only refresh cycles are required. The device should be carefully initialized to be prevented from being entered into multi bit test mode.
2. If RAS= Vss during power-up, the HYM536A414B could begin an active cycle. This condition results in higher power-up current than necessary demands from the power-up. It is recommended that RAS and CAS track with Vcc during power-up or be held at a valid VIH in order to minimize the power-up current.
3. Refer to the HY5117404B data sheet for detailed information.
4. Measured with a load equivalent to 2 TTL loads and 100pF. (VOH= 2.0V, VOL= 0.8V)
5. tCEZ(max.), tOEZ(MAX), tREZ(MAX) and tWEZ(MAX) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either tRCH or tRRH must be satisfied for a read cycle.
7. These parameters are referenced to CAS leading edge in early write cycles and to WE leading edge in late write or read-modify-write cycles.
8. twcs is not a restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If twcs $\geq$ twcs(min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle.
9. Operation within the tRCD(max.) limit insures that tRAC(max.) can be met. tRCD(max.) is specified as a reference point only. If tRCD is greater than the specified tRCD(max.) limit, then access time is controlled by tCAC.
10. Operation within the tRAD(max.) limit insures that tRAC(max.) can be met. tRAD(max.) is specified as a reference point only. If tRAD is greater than the specified tRAD(max.) limit, then access time is controlled by tAA.
11. Measured with the specified current load and 100pF.
12. A burst of 2048 CAS-before-RAS refresh cycles must be executed within 32ms after exiting self refresh (for SL-part).
13. If tCWD $\geq$ twcs(MIN.), tRWD $\geq$ tRWD(MIN.), tAWD $\geq$ tAWD(MIN.) and tCPWD $\geq$ tCPWD(MIN.), the cycle is a read modify write cycle and the data output will contain data read from the selected cell. If neither of the above conditions are met, the condition of the data out (at access time and until CAS goes back to VIH) is indeterminated.
14. In CAS before RAS self refresh mode.
In case of using distributed CAS before RAS refresh, refresh 2048 times during a 256ms after reset
In case of using burst CAS before RAS refresh, refresh 2048 times during a 32ms after reset
In case of using RAS only refresh, refresh against all refresh address during a 32ms after reset
15. If RAS goes to high before CAS high going, the open circuit condition of the output is achieved by CAS high going. If CAS goes to high before RAS high going, the open circuit condition of the output is achieved by RAS high going.

CAPACITANCE

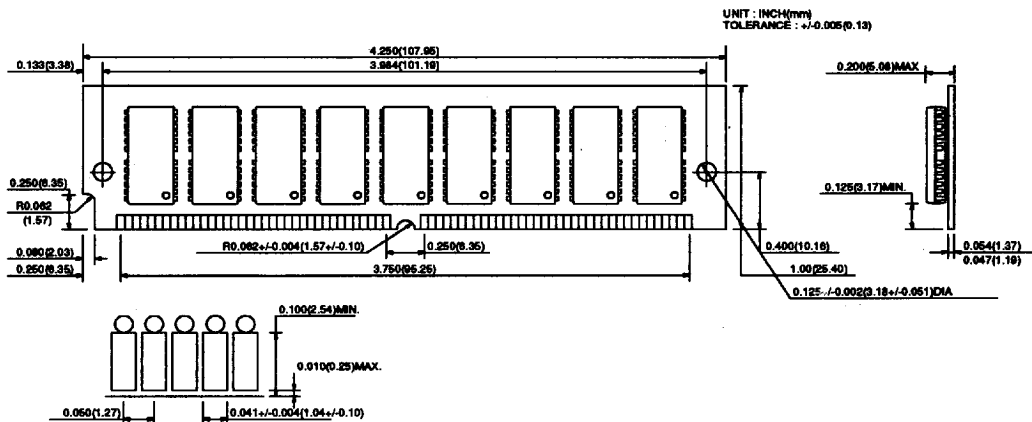
(TA= 25°C, VCC= 5V $\pm$ 10%, VSS= 0V, f= 1MHz, unless otherwise noted.)

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
CIN1	Input Capacitance (A0-A10)	-	65	pF
CIN2	Input Capacitance (WE, OE)	-	80	pF
CIN3	Input Capacitance (RAS0)	-	80	pF
CIN4	Input Capacitance (CAS0)	-	80	pF
CDQ	Data Input/output Capacitance (DQ0-DQ35)	-	17	pF

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PACKAGE INFORMATION

72 pin Single In-line Memory Module (M ; Tin-Lead plated, MG ; Gold plated)
HYM536A414B/BSL (SOJ Mounted)



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ORDERING INFORMATION

PART NUMBER	SPEED	POWER	PACKAGE	PLATING
HYM536A414BM	50/60/70		SIMM	Tin-Lead
HYM536A414BSLM	50/60/70	SL-part	SIMM	Tin-Lead
HYM536A414BMG	50/60/70		SIMM	Gold
HYM536A414BSLMG	50/60/70	SL-part	SIMM	Gold

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