

E10160VHR

ECL Gate Array with ROM

PRELIMINARY

DESCRIPTION

Fujitsu's E10160VHR array utilizes advanced technology to produce an array with high I/O capability, high density, high speed, and excellent power dissipation combined with an on-chip ROM of 160K bits. The internal structure allows up to 13,440 gates, including high-drive and I/O macrocells. High-drive internal macrocells allow a maximum fanout of 40. Interconnection is implemented with four layers of metallization. The E10160VHR is especially well suited for such high-performance systems as mainframe and supermini computers, high-end workstations, telecommunications, and instrumentation for control store and fast look-up table applications.

VH series ECL arrays are designed using Fujitsu's integrated design system software in conjunction with either an Amdahl 5860 or Fujitsu M-780 mainframe supercomputer. The VH series has an extensive cell library.

FEATURES

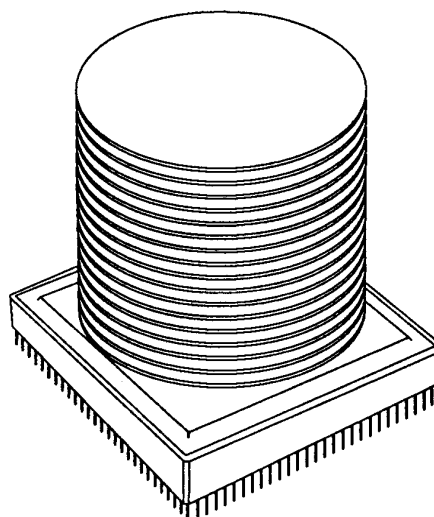
- High Performance Logic
 - 80 ps/gate typical at 2.95 mW¹
 - 135 ps/gate typical at 1.11 mW¹
- 13440 Maximum Equivalent Gates
- 163840 bit = (1024w x 20b) x 8 Mask ROM
- High I/O Count
 - 294 I/O available
- 3-level Series Gating
- Loaded Delay Performance
 - 250 ps/gate typical at 4.6 mW²
 - 300 ps/gate typical at 2.95 mW²
 - 350 ps/gate typical at 1.11 mW²
- ROM access time = 3.0 ns max
- I/O Options
 - 10KH ECL
 - 100K ECL
- ECL Output Options
 - 25Ω, 50Ω, and 100Ω
 - Series terminated
- Advanced Packaging Solutions
 - 441-pin ceramic pin grid array package
 - Supplied with pre-attached heat sinks
 - Multiple heat sink options available
 - TAB processing used

E10160VHR Gate Array Summary

Maximum Internal Gates	13440
Bits of ROM	163840
Maximum I/O	294
Maximum Outputs	204

Notes:

1. Unloaded F/I = F/O = 1, L = 0 mm.
2. Loaded F/I = F/O = 3, L = 3 mm.



441-Pin Ceramic Pin Grid Array

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