2K × 8 Bit Electrically Erasable PROM

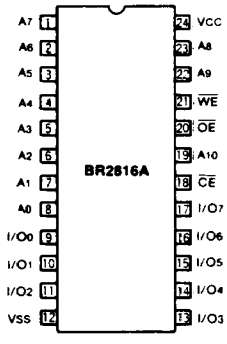
FEATURES

- **2048 × 8 Bit 5V E^2PROM**
- **Single 5-Volt Supply**
- **Fast Read Access Time: 250ns**
- **TTL Level Byte Write: 10ms Max.**
- **Internally Latched Address and Data in Write Cycle**
- **Automatic Erase Before Write**
- **Automatic Write Time-Out**
- **On-Chip False Write Protection**
- **TTL Compatible Inputs and Outputs**
- **JEDEC Approved Byte Wide Memory Pinout**
- **Compatible with Xicor 2816A**

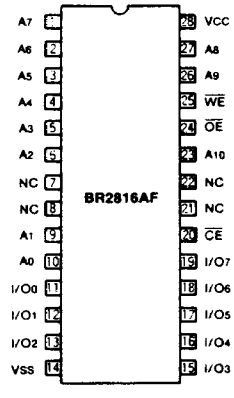
The BR2816A is a 5-Volt 2048 × 8 bit electrically erasable programmable read only memory (E^2PROM). It is remarkably easy to use, operating from a single 5-Volt power supply with read and write cycle timing very similar to that of a static RAM. Byte modification in the 5V programming mode is initiated with a 150ns TTL low level write signal. Address and data bus information is internally latched, freeing the system for other tasks during the write period. The BR2816A automatically erases the selected byte before writing and completes an erase/write cycle in a maximum of 10ms. Advanced power up/down protection mechanisms are incorporated in the BR2816A.

The BR2816A is the ideal device to use in applications that require a nonvolatile memory capable of in-system modification. The device's integrated features and simple microprocessor interface ensure both design ease and minimized board space requirements. Typical applications include self-calibrating equipment, tax table storage in point-of-sale terminals, key storage for data encryption, programmable character generators, and terrain mapping for military avionics.

BR2816A



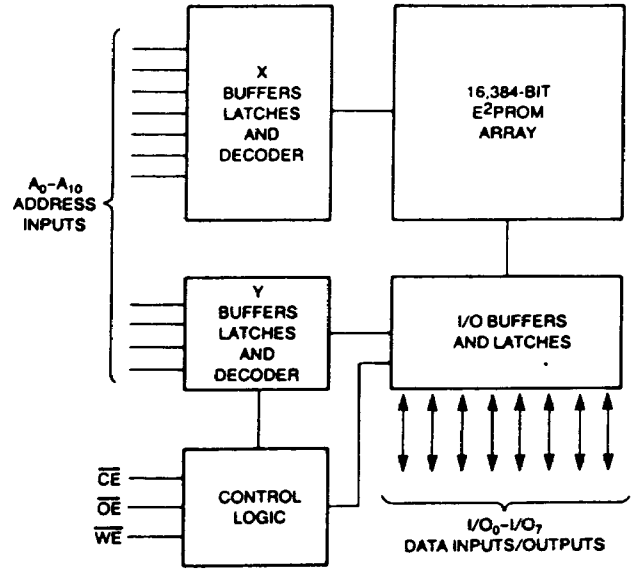
BR2816AF



Pin Names

A_0-A_{10}	ADDRESS INPUTS
I/O_0-I/O_7	DATA INPUTS/OUTPUTS
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{WE}$	WRITE ENABLE
V_{CC}	+5V
V_{SS}	GROUND

Block Diagram



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DEVICE OPERATION

Read

Data is read from the BR2816A by applying a high to $\overline{WE}$, a low to $\overline{CE}$ and a low to $\overline{OE}$. Data is available within t_{AA} time from when the address inputs are valid, within t_{CE} time after $\overline{CE}$ is brought low, or within t_{OE} time after $\overline{OE}$ is brought low, whichever is later. The I/O pins remain in a high impedance state whenever $\overline{OE}$ or $\overline{CE}$ are high to eliminate bus contention in a system environment.

Write

In the 5-Volt programming mode, the write cycle is initiated by applying a low to both $\overline{WE}$ and $\overline{CE}$ while $\overline{OE}$ is high. The address inputs are latched into the device on the falling edge of $\overline{WE}$ or $\overline{CE}$ (whichever is last) to specify the byte location that is to be written. Data on the I/O pins is then latched into the device by bringing either $\overline{WE}$ or $\overline{CE}$ high. Both addresses and data are latched in a brief 200ns interval using a 5V supply and TTL write signals. Once the data is latched, the BR2816A will automatically erase the selected byte and write the new data in less than 10ms. The system is freed for other functions during this period. The I/O pins will be in a high impedance state while the write operation is in progress. Thus, the system can determine the completion of the write operation by performing a read of the last location written and comparing the data read with the data previously written. If this mode of write verification is employed, it is recommended that resistive pull-ups to the V_{CC} supply be incorporated on the outputs. In this case, the data read prior to completion of the write operation will be all 1's.

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
V_{IH}	X	X	Standby	High Z	Standby
V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}	Active
V_{IL}	V_{IH}	⌐_⌐	5V Byte Write	D_{IN}	Active
V_{IL}	V_{IH}	V_{IH}	Read and Write Inhibit	High Z	Active

Standby

Power consumption may be reduced by approximately 55% by deselecting the device with a TTL high applied to $\overline{CE}$.

Endurance

The standard BR2816A is designed for applications requiring up to 10,000 write cycles per byte. The /E2 suffix versions are designed for applications requiring up to 100 write cycles per byte. (See Ordering Information.)

False Write Protection

Four mechanisms for power-up, power-down, and power-noise protection are incorporated in the BR2816A to prevent an unintentional write to the device.

V_{CC} Level Detection

Whenever V_{CC} is below 3.0 volts, write cycles to the device will automatically be inhibited.

Time Delay

During power-up the BR2816A automatically prevents any write operation for a period between 5 and 20ms after V_{CC} reaches the V_{WI} level. This will provide the system with sufficient time to bring $\overline{WE}$ or $\overline{CE}$ to a high level before a write can occur. Read cycles can be executed during the initialization period.

$\overline{OE}$ Gating

The BR2816A inhibits all write operations while the $\overline{OE}$ input is low.

Noise Protected $\overline{WE}$

A write pulse of less than 20ns duration on the $\overline{WE}$ input will not activate a write cycle.

ABSOLUTE MAXIMUM RATINGS[1]

Temperature Under Bias ..... -55°C to +125°C
Storage Temperature ..... -65°C to +125°C
Voltage on any Pin with Respect to Ground[2] ..... -0.5V to +6V
D.C. Output Current 5mA

Operating Range

Range	Ambient Temperature
Standard	0°C to 75°C

DC OPERATING CHARACTERISTICS

Over Operating Range , V_{CC} = 5V ± 5%, unless otherwise specified.

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
V_{IL}	Input Low Voltage		0.8	V	
V_{IH}	Input High Voltage	2.0		V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 2.1mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -400μA
V_{WI}	V_{CC} Trip Voltage for Write Inhibit	3.0	3.5	V	
I_{LI}	Input Leakage Current		10	μA	V_{IN} = 0 to 5.25V
I_{LO}	Output Leakage Current		±10	μA	V_{OUT} = 0 to 5.25V
I_{CC}	V_{CC} Current (Active)		110	mA	$\overline{CE}$ = $\overline{OE}$ = V_{IL} All I/O's = OPEN Other Inputs = 5.25V
I_{SB}	V_{CC} Current (Standby): Standard		40	mA	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL}

CAPACITANCE

T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Unit	Conditions
$C_{I/O}$	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}	Input Capacitance	6	pF	V_{IN} = 0V

Notes:

1. Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages higher than the rated maxima.
3. AC conditions of test: Input pulse levels - 0 to 3.0V, input rise and fall times - 10ns, input and output timing levels - 1.5V, output load - 1 TTL gate and C_L = 100 pF.
4. $\overline{WE}$ is noise protected. A write pulse of less than 20ns duration will not activate a write cycle.
5. Data must be valid within 1 μs after the initiation of a write cycle.

AC CHARACTERISTICS[3]

Over Operating Range, V_{CC} = 5V ± 5%, unless otherwise specified.

Read Cycle - See Figure 1.

Symbol	Parameter	BR2816A 250 Limits		BR2816A 300 Limits		BR2816A 350 Limits		BR2816A 450 Limits		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	250		300		350		450		ns
t_{CE}	Chip Enable Access Time		250		300		350		450	ns
t_{AA}	Address Access Time		250		300		350		450	ns
t_{OE}	Output Enable Access Time: Standard		100		120		135		150	ns
t_{LZ}	Chip Enable to Output in Low Z	10		10		10		10		ns
t_{HZ}	Chip Disable to Output in High Z: Standard	10	100	10	100	10	100	10	100	ns
t_{OLZ}	Output Enable to Output in Low Z	10		10		10		10		ns
t_{OHZ}	Output Disable to Output in High Z: Standard	10	70	10	80	10	100	10	100	ns
t_{OH}	Output Hold from Address Change	20		20		20		20		ns

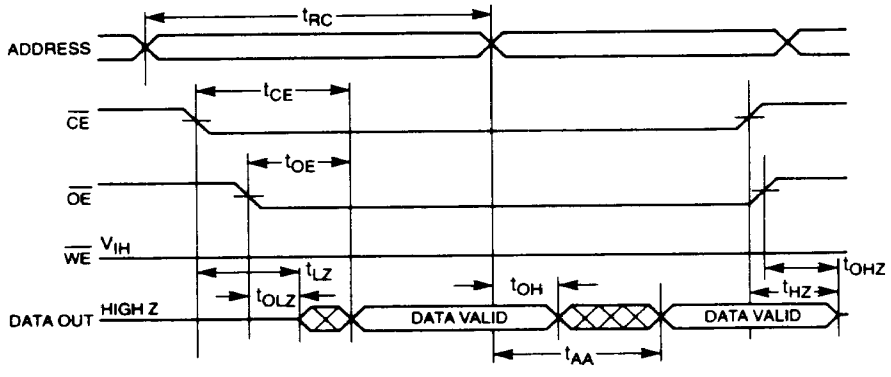


Figure 1. Read Cycle

Write Cycle – See Figures 2 and 3.
5-Volt Programming Mode

Symbol	Parameter	Limits		Units
		Min.	Max.	
t_{WC}	Write Cycle Time	10		ms
t_{AS}	Address Setup Time	10		ns
t_{AH}	Address Hold Time Standard	70		ns
t_{CS}	Write Setup Time	0		ns
t_{CH}	Write Hold Time	0		ns
t_{CW}	Chip Enable to End of Write Input	150		ns
t_{OES}	Output Enable Setup Time	10		ns
t_{OEH}	Output Enable Hold Time	10		ns
t_{WP}[4]	Write Pulse Width	150		ns
t_{DL}	Data Latch Time	50		ns
t_{DV}[5]	Data Valid Time		1	μs
t_{DS}	Data Setup Time	50		ns
t_{DH}	Data Hold Time	10		ns
t_{INIT}	Power-Up Initialization Period (See Text)	5	20	ms

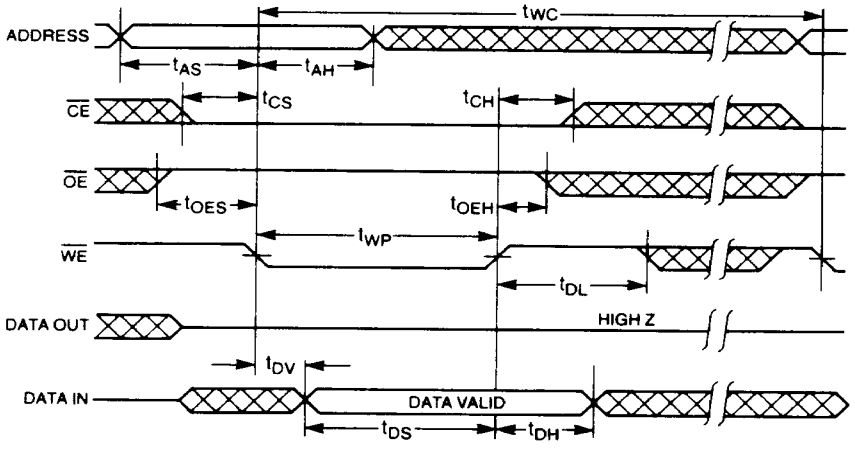


Figure 2. $\overline{WE}$ Controlled Write Cycle

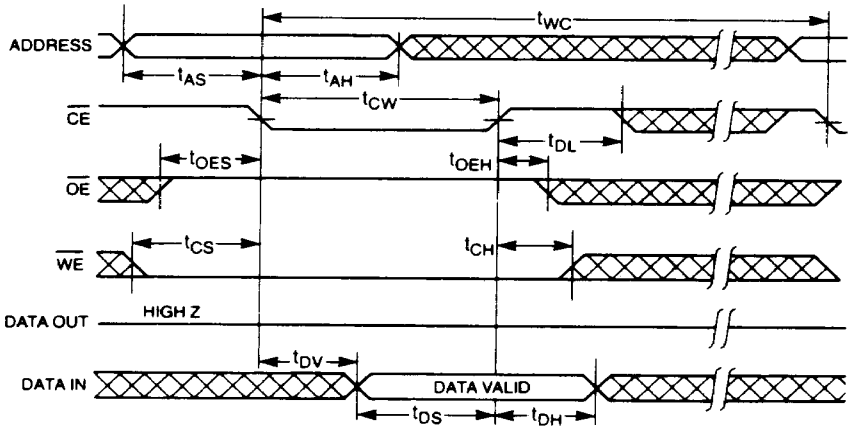
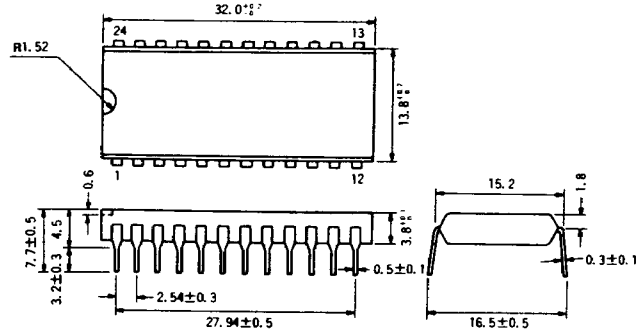


Figure 3. $\overline{CE}$ Controlled Write Cycle

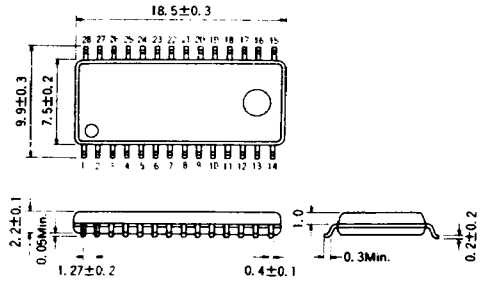
PACKAGE INFORMATION: UNIT IN MM.

BR2816A



DIP24pin

BR2816AF



MF28pin

ORDERING INFORMATION:

Part Number	Access Time (ns)	Temperature Range (°C)	Endurance (cycles)	Package
BR2816A -250 BR2816AF -250	250	0 - 70	10,000	DIP24 MF28
BR2816A -300 BR2816AF -300	300	0 - 70	10,000	DIP24 MF28
BR2816A -350 BR2816AF -350	350	0 - 70	10,000	DIP24 MF28
BR2816A -450 BR2816AF -450	450	0 - 70	10,000	DIP24 MF28

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