Field Programmable Gate Arrays

Features

- **High Performance**
  - **System Speeds > 100 MHz**
  - **Flip-Flop Toggle Rates > 250 MHz**
  - **1.2 ns Input Delay**
  - **3.5 ns Output Delay**
- **Thousands of Registers**
- **Cache Logic™ Design**
  - **Complete/Partial In-System Reconfiguration**
  - **No Loss of Data or Machine State**
  - **Adaptive Hardware**
- **Automatic Component Generators**
  - **Reusable Custom Hard Macro Functions**
- **Very Low Power Consumption**
  - **Standby Current of 500 µA**
  - **Typical Operating Current of 50 to 170 mA**
- **Programmable Clock Options**
  - **Independently Controlled Column Clocks**
  - **Independently Controlled Column Resets**
  - **Clock Skew Less Than 1 ns Across Chip**
- **Independently Configurable I/O (PCI Compatible)**
  - **TTL/CMOS Input Thresholds**
  - **Open Collector/Tri-state Outputs**
  - **Programmable Slew-Rate Control**
  - **I/O Drive of 16 mA (Combinable to 64 mA)**

Description

AT6000 Series SRAM-Based Field Programmable Gate Arrays (FPGAs) provide the density and performance of custom gate arrays without the prototyping and debugging delays associated with mask-programmed devices.

Supporting system speeds greater than 100 MHz and using a typical operating current of 50 to 170 mA, AT6000 Series devices are ideal for high-speed, compute-intensive designs. These FPGAs are designed to implement Cache Logic™, the ability to implement adaptive hardware and perform hardware acceleration.

The patented AT6000 Series architecture employs a symmetrical grid of small, yet powerful cells connected to a flexible busing network. Independently controlled clocks and resets govern every column of cells. The array is surrounded by programmable I/O.

Devices range in size from 2,000 to 20,000 usable gates, and 1024 to 6400 registers. Pin locations are consistent throughout the AT6000 Series for easy design migration. High-I/O versions are available for the lower gate count devices.

AT6000 Series Field Programmable Gate Arrays

Device	AT6002	AT6003	AT6005	AT6010
Usable Gates	2,000-4,000	3,000-6,000	5,000-10,000	10,000-20,000
Cells	1,024	1,600	3,136	6,400
Registers (maximum)	1,024	1,600	3,136	6,400
I/O (maximum)	96	120	108	204
Typ. Operating Current (mA)	30	45	80	170
Cell Rows x Columns	32 x 32	40 x 40	56 x 56	80 x 80

Description (Continued)

AT6000 Series FPGAs utilize a reliable 0.8-µm single-poly, double-metal CMOS process and are 100% factory-tested.

Atmel's PC- and workstation-based Integrated Development System is used to create AT6000 Series designs. Multiple design entry methods are supported, including those from Viewlogic, Mentor, Exemplar, Cadence and Synopsys.

The Atmel architecture was developed to provide the highest levels of performance, functional density and design flexibility in an FPGA. The cells in the Atmel array are small, very efficient and contain the most important and most commonly used logic and wiring functions. The cell's small size leads to arrays with large numbers of cells, greatly multiplying the functionality in each cell. A simple, high-speed busing network provides fast, efficient communication over medium and long distances.

The Symmetrical Array

At the heart of the Atmel architecture is a symmetrical array of identical cells (Figure 1). The array is continuous and completely uninterrupted from one edge to the other, except for bus *repeaters* spaced every eight cells (Figure 2).

In addition to logic and storage, cells can also be used as wires to connect functions together over short distances and are useful for routing in tight spaces. Buses support fast, efficient communication over medium and long distances.

The Busing Network

There are two kinds of buses: local and express (see Figures 2 and 3).

Local buses are the link between the array of cells and the busing network. There are two local buses— North-South 1 and 2 (NS1 and NS2)— for every column of cells, and two local buses— East-West 1 and 2 (EW1 and EW2)— for every row of cells. In a sector each local bus is connected to every cell in its column or row, thus providing every cell in the array with read/write access to two North-South and two East-West buses.

Figure 1. Symmetrical Array Surrounded by I/O

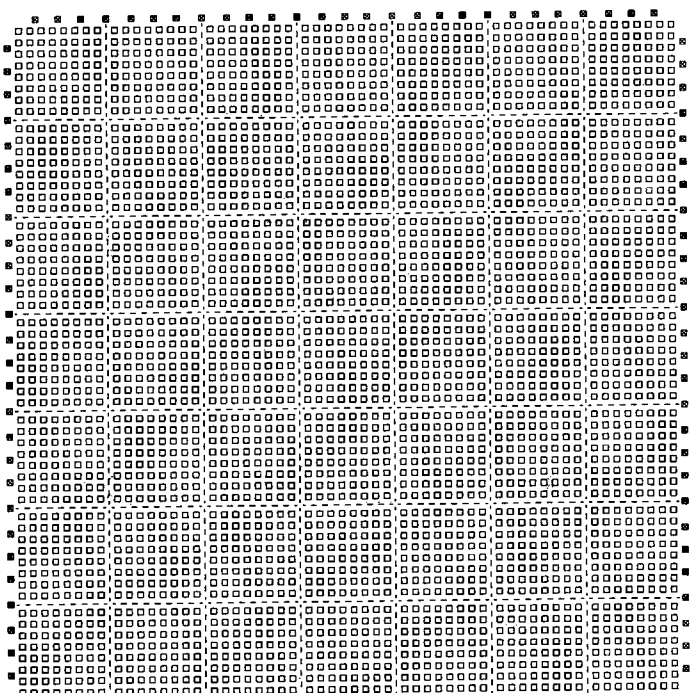


Figure 2. Busing Network

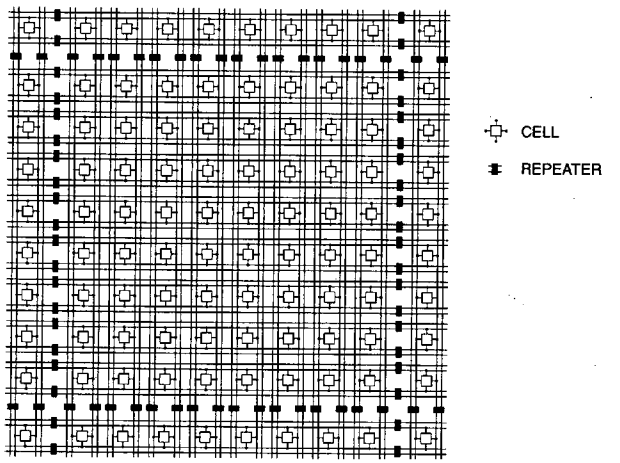
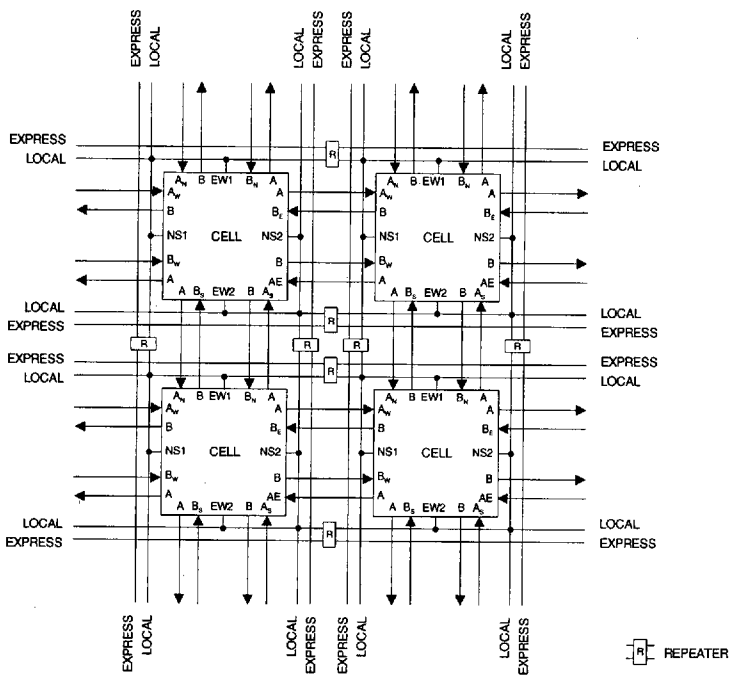


Figure 3. Cell-to-Cell and Bus-to-Bus Connections



Each cell, in addition, provides the ability to route a signal on a 90° turn between the NS1 bus and EW1 bus and between the NS2 bus and EW2 bus.

Express buses are not connected directly to cells, and thus provide higher speeds. They are the fastest way to cover long, straight-line distances within the array.

Each express bus is paired with a local bus, so there are two express buses for every column and two express buses for every row of cells.

Connective units, called repeaters, spaced every eight cells, divide each bus, both local and express, into segments spanning eight cells. Repeaters are aligned in rows and columns thereby partitioning the array into 8 x 8 sectors of cells. Each repeater is associated with a local/express pair, and on each side of the repeater are connections to a local-bus segment and an express-bus segment. The repeater can be programmed to provide any one of twenty-one connecting functions. These functions are symmetric with respect to both the two repeater sides and the two types of buses.

Among the functions provided are the ability to:

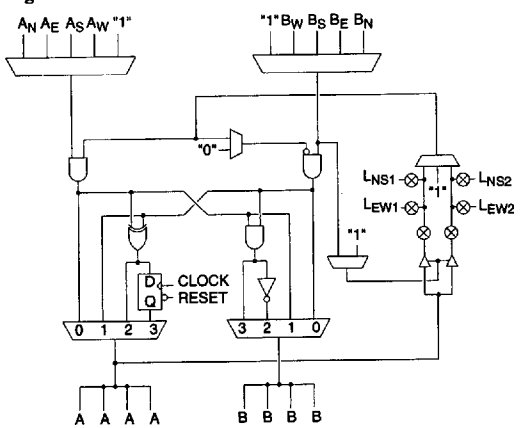
- Isolate bus segments from one another
- Connect two local-bus segments
- Connect two express-bus segments
- Implement a local/express transfer

In all of these cases, each connection provides signal regeneration and is thus uni-directional. For bi-directional connections, the basic repeater function for the NS2 and EW2 repeaters is augmented with a special programmable connection allowing bi-directional communication between local-bus segments. This option is primarily used to implement long, tri-state buses.

The Cell Structure

The Atmel cell (Figure 4) is simple and small and yet can be programmed to perform all the logic and wiring functions needed to implement any digital circuit. Its four sides are functionally identical, so each cell is completely symmetrical.

Figure 4. Cell Structure



Read/write access to the four local buses— NS1, EW1, NS2 and EW2— is controlled, in part, by four bi-directional pass gates connected directly to the buses. To read a local bus, the pass gate for that bus is turned on and the three-input multiplexer is set accordingly. To write to a local bus, the pass gate for that bus and the pass gate for the associated tri-state driver are both turned on. The two-input multiplexer supplying the control signal to the drivers permits either: (1) active drive, or (2) dynamic tri-stating controlled by the B input. Turning between L_{NS1} and L_{EW1} or between L_{NS2} and L_{EW2} is accomplished by turning on the two associated pass gates. The operations of reading, writing and turning are subject to the restriction that each bus can be involved in no more than a single operation.

In addition to the four local-bus connections, a cell receives two inputs and provides two outputs to each of its North (N), South (S), East (E) and West (W) neighbors. These inputs and outputs are divided into two classes: "A" and "B." There is an A input and a B input from each neighboring cell and an A output and a B output driving all four neighbors. Between cells, an A output is always connected to an A input and a B output to a B input.

Within the cell, the four A inputs and the four B inputs enter two separate, independently configurable multiplexers. Cell flexibility is enhanced by allowing each multiplexer to select also the logical constant "1." The two multiplexer outputs enter the two upstream AND gates.

Downstream from these two AND gates are an Exclusive-OR (XOR) gate, a register, a downstream AND gate, an inverter and two four-input multiplexers producing the A and B outputs. These multiplexers are controlled in tandem (unlike the A and B input multiplexers) and determine the function of the cell.

- In State 0— corresponding to the "0" inputs of the multiplexers— the output of the left-hand upstream AND gate is connected to the cell's A output, and the output of the right-hand upstream AND gate is connected to the cell's B output.
- In State 1— corresponding to the "1" inputs of the multiplexers— the output of the left-hand upstream AND gate is connected to the cell's B output, the output of the right-hand upstream AND gate is connected to the cell's A output.
- In State 2— corresponding to the "2" inputs of the multiplexers— the XOR of the outputs from the two upstream AND gates is provided to the cell's A output, while the NAND of these two outputs is provided to the cell's B output.
- In State 3— corresponding to the "3" inputs of the multiplexers— the XOR function of State 2 is provided to the D input of a D-type flip-flop, the Q output of which is connected to the cell's A output. Clock and asynchronous reset signals are supplied externally as described later. The AND of the outputs from the two upstream AND gates is provided to the cell's B output.

Logic States

The Atmel cell implements a rich and powerful set of logic functions, stemming from 44 cell states. Some states use both A and B inputs. Other states are created by selecting the "1" input on either or both of the input multiplexers.

There are 20 purely combinatorial states with a range of functions, including NOR, AND, NAND, OR and two-input multi-

Figure 5a. Combinatorial States

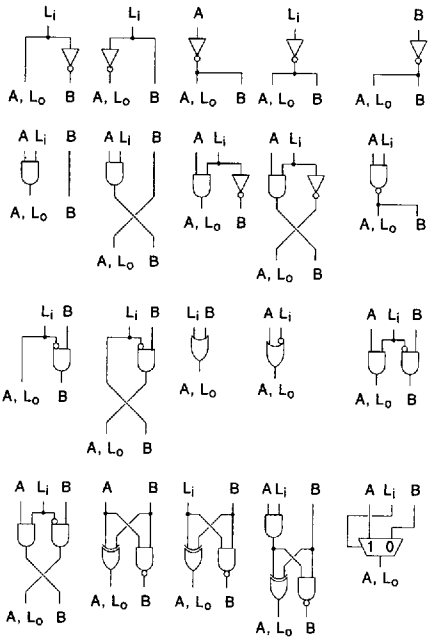


Figure 5b. Register States

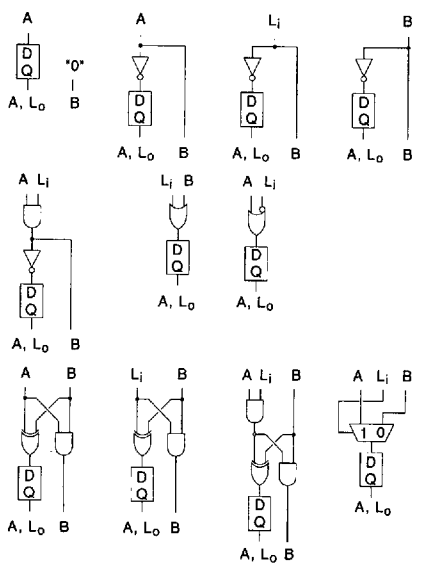


Figure 5c. Constant States

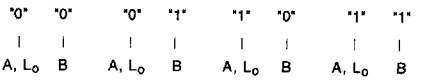


Figure 6a. Two-Input AND Feeding XOR

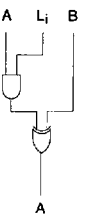
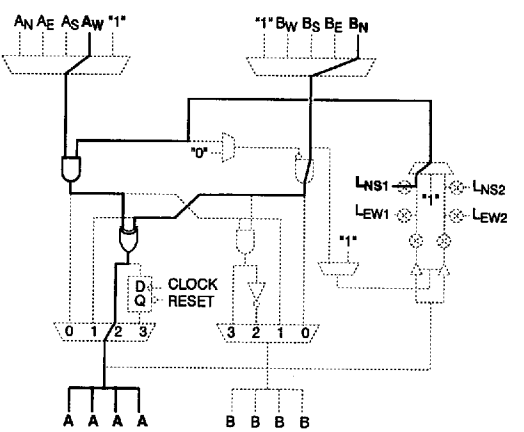


Figure 6b. Cell Configuration (A•L) XOR B



plexer (Figure 5a). There are 11 register states ranging from a simple register to a register preceded by a two-input multiplexer (Figure 5b). Five constant states produce all combinations of constant values at the two cell outputs (Figure 5c). There are five tri-state states. More complex functions are created by using cells in combination.

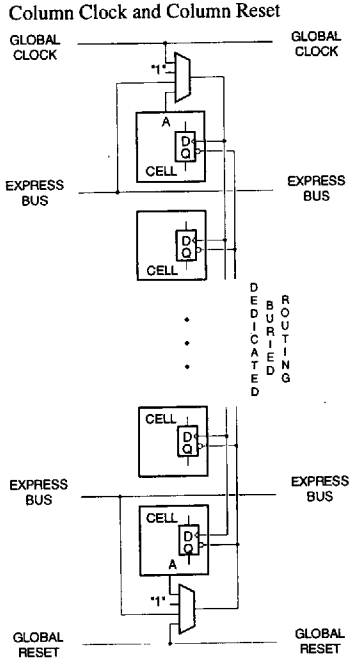
A two-input AND feeding an XOR (Figure 6a) is produced using a single cell (Figure 6b). A two-to-one multiplexer selects the logical constant "0" and feeds it to the right-hand AND gate. The AND gate acts as a feed-through, letting the B input pass through to the XOR. The three-to-one multiplexer on the right side selects the local-bus input, L_{NS1}, and passes it to the left-hand AND gate. The A and L_{NS1} signals are the inputs to the AND gate. The output of the AND gate feeds into the XOR, producing the logic state (A•L) XOR B.

Clock Distribution

Along the top edge of the array is logic for distributing clock signals to the D flip-flop in each logic cell (Figure 7). The distribution network is organized by column and permits columns of cells to be independently clocked. At the head of each column is a user-configurable multiplexer providing the clock signal for that column. It has four inputs:

- Global clock supplied through the CLOCK pin
- Express bus adjacent to the distribution logic
- "A" output of the cell at the head of the column
- Logical constant "1" to conserve power (no clock)

Figure 7. Column Clock and Column Reset



Through the global clock, the network provides low-skew distribution of an externally supplied clock to any or all the columns of the array. The global clock pin is also connected directly to the array via the A input of the upper left and right corner cells (AW on the left, and AN on the right). The express bus is useful in distributing a secondary clock to multiple columns when the global clock line is used as a primary clock. The A output of a cell is useful in providing a clock signal to a single column. The constant "1" is used to reduce power dissipation in columns using no registers.

Asynchronous Reset

Along the bottom edge of the array is logic for asynchronously resetting the D flip-flops in the logic cells (Figure 7). Like the clock network, the asynchronous reset network is organized by column and permits columns to be independently reset. At the bottom of each column is a user-configurable multiplexer providing the reset signal for that column. It has four inputs:

- Global asynchronous reset supplied through the $\overline{\text{RESET}}$ pin
- Express bus adjacent to the distribution logic
- "A" output of the cell at the foot of the column
- Logical constant "1"to conserve power

The asynchronous reset logic uses these four inputs in the same way that the clock distribution logic does. Through the global asynchronous reset, any or all columns can be reset by an externally supplied signal. The global asynchronous reset pin is also connected directly to the array via the A input of the lower left and right corner cells (AS on the left, and AE on the right). The express bus can be used to distribute a secondary reset to multiple columns when the global reset line is used as a primary reset, the A output of a cell can also provide an asynchronous reset signal to a single column, and the constant "1" is used by columns with registers requiring no reset. All registers are reset during power-up.

Input/Output

The Atmel architecture provides a flexible interface between the logic array, the configuration control logic and the I/O pins.

Two adjacent cells— an "exit" and an "entrance" cell— on the perimeter of the logic array are associated with each I/O pin.

There are two types of I/Os: A-type (Figure 8a) and B-type (Figure 8b). For A-type I/Os, the edge-facing A output of an exit cell is connected to an output driver, and the edge-facing A input of the adjacent entrance cell is connected to an input buffer. The output of the output driver and the input of the input buffer are connected to a common pin.

B-type I/Os are the same as A-type I/Os, but use the B inputs and outputs of their respective entrance and exit cells. A- and B-type I/Os alternate around the array.

Control of the I/O logic is provided by user-configurable memory bits.

TTL/CMOS Inputs

A user-configurable bit determining the threshold level— TTL or CMOS— of the input buffer.

Open Collector/Tri-state Outputs

A user-configurable bit which enables or disables the active pull-up of the output device.

Slew Rate Control

A user-configurable bit which controls the slew rate— fast or slow— of the output buffer. A slow slew rate, which reduces noise and ground bounce, is recommended for outputs that are not speed-critical. Fast and slow slew rates have the same DC-current sinking capabilities, but the rate at which each allows the output devices to reach full drive differs.

Pull-up

A user-configurable bit controlling the pull-up transistor in the I/O pin. It's primary function is to provide a logical "1" to unused input pins. When on, it is roughly equivalent to a 25K resistor to V_{CC}.

Enable Select

User-configurable bits determining the output-enable for the output driver. The output driver can be static, always on, always off, or dynamically controlled by a signal generated in the array. Four options are available from the array: (1) the control is low and always driving; (2) the control is high and never driving; (3) the control is connected to a vertical local bus associated with the output cell; and (4) the control is connected to a horizontal local bus associated with the output cell. The power-up default is never driving.

In addition to the functionality provided by the I/O logic, the entrance and exit cells provide the ability to register both inputs and outputs. Also, these perimeter cells (unlike interior cells) are connected directly to express buses: the edge-facing A and B outputs of the entrance cell are connected to express buses, as are the edge-facing A and B inputs of the exit cell. These buses are perpendicular to the edge, and provide a rapid means of bringing I/O signals to and from the array interior and the opposite edge of the chip.

Chip Configuration

The Integrated Development System generates the SRAM bit pattern required to configure a AT6000 Series device. A PC parallel port, microprocessor, EPROM or serial configuration memory can be used to download configuration patterns.

Users select from several configuration modes. Many factors, including board area, configuration speed and the number of designs implemented in parallel can influence the user's final choice.

Configuration is controlled by dedicated configuration pins and dual-function pins that double as I/O pins when the device is in operation. The number of dual-function pins required for each mode varies.

The devices can be partially reconfigured while in operation. Portions of the device not being modified remain operational during configuration. Simultaneous configuration of more than one device is also possible. Full configuration takes as little as a millisecond, partial configuration is even faster.

Refer to the Pin Function Description section following for a brief summary of the pins used in configuration. For more information about configuration, refer to the AT6000 Series Configuration data sheet.

Figure 8a. A-Type I/O Logic

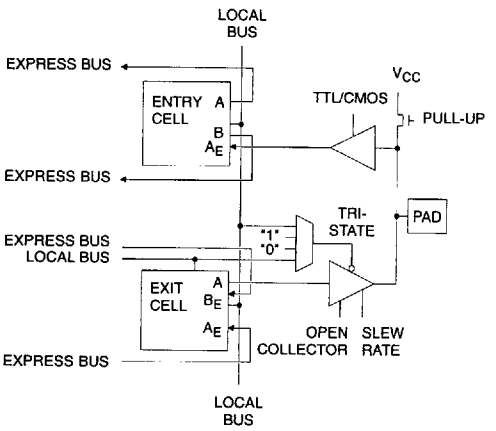
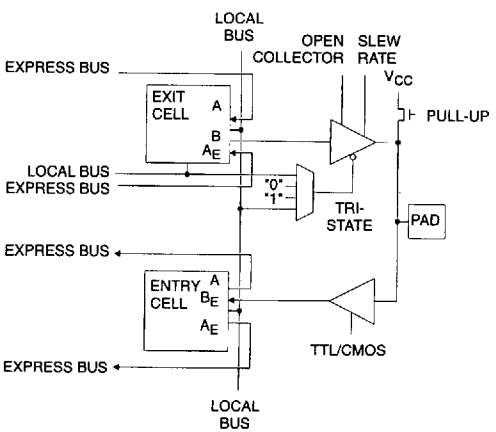


Figure 8b. B-Type I/O Logic



Pin Function Description

This section provides abbreviated descriptions of the various AT6000 Series pins. For more complete descriptions, refer to the AT6000 Series Configuration data sheet.

Pinout tables for the AT6000 series of devices follow.

Power Pins

V_{CC}, V_{DD}, GND, V_{SS}

V_{CC} and GND are the I/O supply pins, V_{DD} and V_{SS} are the internal logic supply pins. V_{CC} and V_{DD} should be tied to the same trace on the printed circuit board. GND and V_{SS} should be tied to the same trace on the printed circuit board.

Input/Output Pins

All I/O pins can be used in the same way (refer to the I/O section of the architecture description). Some I/O pins are dual-function pins used during configuration of the array. When not being used for configuration, dual-function I/Os are fully functional as normal I/O pins. On initial power-up, all I/Os are configured as TTL inputs with a pull-up.

Dedicated Timing and Control Pins

$\overline{CON}$

Configuration-in-process pin. After power-up, $\overline{CON}$ remains low until power-up initialization is complete. $\overline{CON}$ is an open collector signal. After power-up initialization, forcing $\overline{CON}$ low begins the configuration process.

$\overline{CS}$

Configuration enable pin. All configuration pins are ignored if $\overline{CS}$ is high. $\overline{CS}$ must be held low throughout the configuration process. $\overline{CS}$ is a TTL-type input pin.

M0, M1, M2

Configuration mode pins used to determine the configuration mode. All three are TTL-type input pins.

CCLK

Configuration clock pin. CCLK is an input or an output depending on the configuration mode selected. It is an output in two modes. The output modes support configuration using the fewest external components. In either of these modes, the configuration time will vary from part to part depending on clock speed. CCLK is a TTL-type input in modes that use it as an input and a CMOS-type output in those modes that use it as an output. When not in use, CCLK is set low.

CLOCK

External logic source used to drive the internal global clock line. Registers toggle on the rising edge of CLOCK. The CLOCK signal is neither used nor affected by the configuration modes. It is always a TTL input.

$\overline{RESET}$

Array register asynchronous reset. $\overline{RESET}$ drives the internal global reset. The $\overline{RESET}$ signal is neither used nor affected by the configuration modes. It is always a TTL input.

Dual-Function Pins

When $\overline{CON}$ is high, dual-function I/O pins act as device I/Os; when $\overline{CON}$ is low, dual-function pins are used as configuration control or data signals as determined by the configuration modes. Care must be taken when using these pins to ensure that configuration activity does not interfere with other circuitry associated with the pin's net.

D0 or I/O

Serial configuration modes use D0 as the serial data input pin. Parallel configuration modes use D0 as the least-significant bit. Input data must meet setup and hold requirements with respect to the rising edge of CCLK.

D1 to D7 or I/O

Parallel configuration modes use these pins as inputs. Serial configuration modes do not use them. Data must meet setup and hold requirements with respect to the rising edge of CCLK.

$\overline{CEN}$ or I/O

During address count-up/down configuration, $\overline{CEN}$ is an output. $\overline{CEN}$ can be used as the output enable of a parallel EPROM. In this case, it should be configured as a constant high, and not used as a configurable I/O pin.

A0 to A16 or I/O

During address count-up/down configuration, these pins are outputs and act as the address pins for a parallel EPROM. A0A16 eliminate the need for an external address counter if the user wishes to use an inexpensive parallel EPROM to program a device. Addresses change after the rising edge of the CCLK signal.

$\overline{CSOUT}$ or I/O

When cascading devices, $\overline{CSOUT}$ is an output used to enable other devices. $\overline{CSOUT}$ should be connected to the CS input of the downstream device. The $\overline{CSOUT}$ function is optional and can be disabled during initial programming when cascading is not used. When cascading devices, $\overline{CSOUT}$ should be dedicated to configuration and not used as a configurable I/O.

$\overline{\text{CHECK}}$ or I/O

During configuration, $\overline{\text{CHECK}}$ is an input that can be used to enable the data check function at the beginning of a configuration cycle. No data is written to the device while $\overline{\text{CHECK}}$ is low. Instead, the configuration file being applied to D0-D7 is compared with the current contents of the internal configuration RAM. If a mismatch is detected between the data being loaded and the data already in the RAM, the $\overline{\text{ERR}}$ pin goes low. The $\overline{\text{CHECK}}$ function is optional and can be disabled during initial programming.

$\overline{\text{ERR}}$ or I/O

During configuration, $\overline{\text{ERR}}$ is an output. When the $\overline{\text{CHECK}}$ function is activated and a mismatch is detected between the current configuration data stream and the data already loaded in the configuration RAM, $\overline{\text{ERR}}$ goes low. The $\overline{\text{ERR}}$ output is a registered signal. Once a mismatch is found, the signal is set and is only reset after the configuration cycle is complete. $\overline{\text{ERR}}$ is also asserted for configuration file errors. The $\overline{\text{ERR}}$ function is optional and can be disabled during initial programming.

Device Pinout Selection

	AT6002	AT6003	AT6005	AT6010
84 PLCC	64 I/O	64 I/O	64 I/O	—
100 VQFP	80 I/O	80 I/O	80 I/O	—
132 PQFP	96 I/O	108 I/O	108 I/O	108 I/O
144 TQFP	96 I/O	120 I/O	108 I/O	120 I/O
180 CPGA	—	—	108 I/O	156 I/O
208 PQFP	—	—	—	172 I/O
240 PQFP	—	—	—	204 I/O

Bit-Stream Sizes (bytes of data)

Mode(s)	Type [1, 2]	Beginning Sequence	AT6002	AT6003	AT6005	AT6010
1	P	Preamble	2677	4153	8077	16393
2	P	Preamble	2677	4153	8077	16393
3	S	Null Byte/Preamble	2678	4154	8078	16394
4	S	Null Byte/Preamble	2678	4154	8078	16394
5	P	Preamble	2677	4153	8077	16393
6	P	Preamble/Preamble	2678	4154	8078	16394

Notes: 1. P = Parallel.
2. S = Serial.

Pinout Assignment

Left Side (Top to Bottom)										
AT6002	AT6003	AT6005	AT6010	84 PLCC	100 VQFP	132 PQFP	144 TQFP	180 CPGA	208 PQFP	240 PQFP
—	—	—	I/O51(A)	—	—	—	—	B1	1	1
I/O24 or A7	I/O30 or A7	I/O27 or A7	I/O50(A) or A7	12	1	18	1	C1	2	2
—	I/O29	—	I/O49(A)	—	—	—	2	D1	3	3
—	—	—	I/O48(B)	—	—	—	—	—	—	4
—	—	—	VCC	—	—	—	—	PWR[1]	4	5
—	—	—	I/O47(A)	—	—	—	—	E1	5	6
—	—	—	GND	—	—	—	—	GND[2]	6	7
—	I/O28	I/O26	I/O46(A)	—	—	19	3	G1	7	8
I/O23 or A6	I/O27 or A6	I/O25 or A6	I/O45(A) or A6	13	2	20	4	H1	8	9
—	—	—	I/O44(B)	—	—	—	—	—	—	10
—	—	—	I/O43(A)	—	—	—	—	C2	9	11
I/O22	I/O26	I/O24	I/O42(A)	—	—	21	5	D2	10	12
I/O21 or A5	I/O25 or A5	I/O23 or A5	I/O41(A) or A5	14	3	22	6	E2	11	13
—	—	—	I/O40(B)	—	—	—	—	—	—	14
—	—	—	I/O39(A)	—	—	—	—	F2	12	15
I/O20	I/O24	I/O22	I/O38(A)	—	4	23	7	G2	13	16
I/O19 or A4	I/O23 or A4	I/O21 or A4	I/O37(A) or A4	15	5	24	8	H2	14	17
—	—	—	I/O36(B)	—	—	—	—	—	—	18
I/O18	I/O22	I/O20	I/O35(A)	—	—	25	9	D3	15	19
I/O17 or A3	I/O21 or A3	I/O19 or A3	I/O34(A) or A3	16	6	26	10	E3	16	20
I/O16	I/O20	I/O18	I/O33(A)	—	7	27	11	F3	17	21
—	—	—	I/O32(B)	—	—	—	—	—	18	22
I/O15 or A2	I/O19 or A2	I/O17 or A2	I/O31(A) or A2	17	8	28	12	G3	19	23
—	I/O18	I/O16	I/O30(A)	—	—	29	13	H3	20	24
GND	GND	GND	GND	18	9	30	14	GND[2]	21	25
VSS	VSS	VSS	VSS	19	10	31	15	GND[2]	22	26
I/O14 or A1	I/O17 or A1	I/O15 or A1	I/O29(A) or A1	20	11	32	16	F4	23	27
—	—	—	I/O28(B)	—	—	—	—	—	24	28
—	I/O16	—	I/O27(A)	—	—	—	17	G4	25	29
I/O13 or A0	I/O15 or A0	I/O14 or A0	I/O26(A) or A0	21	12	33	18	H4	26	30
I/O12 or D7	I/O14 or D7	I/O13 or D7	I/O25(A) or D7	22	13	34	19	H5	27	31
—	—	—	I/O24(B)	—	—	—	—	—	28	32
I/O11 or D6	I/O13 or D6	I/O12 or D6	I/O23(A) or D6	23	14	35	20	J4	29	33
I/O10 or D5	I/O12 or D5	I/O11 or D5	I/O22(A) or D5	24	15	36	21	K4	30	34
VDD	VDD	VDD	VDD	25	16	37	22	PWR[1]	31	35
VCC	VCC	VCC	VCC	26	17	38	23	PWR[1]	32	36
I/O9	I/O11	I/O10	I/O21(A)	—	—	39	24	J3	33	37
—	—	—	I/O20(B)	—	—	—	—	—	34	38
I/O8 or D4	I/O10 or D4	I/O9 or D4	I/O19(A) or D4	27	18	40	25	K3	35	39
I/O7	I/O9	I/O8	I/O18(A)	—	19	41	26	L3	36	40
—	—	—	I/O17(A)	—	—	—	—	M3	37	41
—	—	—	I/O16(B)	—	—	—	—	—	—	42
I/O6 or D3	I/O8 or D3	I/O7 or D3	I/O15(A) or D3	28	20	42	27	N3	38	43
—	I/07	I/O6	I/O14(A)	—	—	43	28	J2	39	44
—	—	—	I/O13(A)	—	—	—	—	K2	40	45
GND	GND	GND	GND	—	—	44	29	GND[2]	41	46
—	—	—	VSS	—	—	—	—	GND[2]	42	47
—	—	—	I/O12(B)	—	—	—	—	—	—	48
I/O5 or D2	I/O6 or D2	I/O5 or D2	I/O11(A) or D2	29	21	45	30	M2	43	49
I/O4	I/O5	I/O4	I/O10(A)	—	22	46	31	N2	44	50
—	—	—	I/O9(A)	—	—	—	—	P2	45	51
—	—	—	I/O8(B)	—	—	—	—	—	—	52
I/O3 or D1	I/O4 or D1	I/O3 or D1	I/O7(A) or D1	30	23	47	32	J1	46	53
I/O2	I/O3	I/O2	I/O6(A)	—	—	48	33	K1	47	54
—	—	—	I/O5(A)	—	—	—	—	L1	48	55
—	—	—	I/O4(B)	—	—	—	—	—	—	56
—	I/O2	—	I/O3(A)	—	—	—	34	M1	49	57
I/O1 or D0	I/O1 or D0	I/O1 or D0	I/O2(A) or D0	31	24	49	35	N1	50	58
—	—	—	I/O1(A)	—	—	—	—	P1	51	59
CCLK	CCLK	CCLK	CCLK	32	25	50	36	R1	52	60

Notes: 1. PWR = Pins connected to power plane = F1, E4/E5, L2, R4, K15, L12, E14, A12.
2. GND = Pins connected to ground plane = L4, M4, N9, N10, E12, D12, C7, C6.

Pinout Assignment (Continued)

Bottom Side (Left to Right)										
AT6002	AT6003	AT6005	AT6010	84 PLCC	100 VQFP	132 PQFP	144 TQFP	180 CPGA	208 PQFP	240 PQFP
CON	CON	CON	CON	33	26	51	37	M5	53	61
—	—	—	I/O204(A)	—	—	—	—	M6	54	62
I/O96 or CEN	I/O120 or CEN	I/O108 or CEN	I/O203(A) or CEN	34	27	52	38	M7	55	63
—	I/O119	—	I/O202(A)	—	—	—	39	R2	56	64
—	—	—	I/O201(B)	—	—	—	—	—	—	65
—	—	—	VCC	—	—	—	—	PWR[1]	57	66
—	—	—	I/O200(A)	—	—	—	—	R3	58	67
—	—	—	GND	—	—	—	—	GND[2]	59	68
—	I/O118	I/O107	I/O199(A)	—	—	53	40	R5	60	69
I/O95 or CSOUT	I/O117 or CSOUT	I/O106 or CSOUT	I/O198(A) or CSOUT	35	28	54	41	R6	61	70
—	—	—	I/O197(B)	—	—	—	—	—	—	71
—	—	—	I/O196(A)	—	—	—	—	R7	62	72
I/O94	I/O116	I/O105	I/O195(A)	—	—	55	42	P3	63	73
I/O93	I/O115	I/O104	I/O194(A)	36	29	56	43	P4	64	74
—	—	—	I/O193(B)	—	—	—	—	—	—	75
—	—	—	I/O192(A)	—	—	—	—	P5	65	76
I/O92	I/O114	I/O103	I/O191(A)	—	30	57	44	P6	66	77
I/O91 or CHECK	I/O113 or CHECK	I/O102 or CHECK	I/O190(A) or CHECK	37	31	58	45	P7	67	78
—	—	—	I/O189(B)	—	—	—	—	—	—	79
I/O90	I/O112	I/O101	I/O188(A)	—	—	59	46	N4	68	80
I/O89 or ERR	I/O111 or ERR	I/O100 or ERR	I/O187(A) or ERR	38	32	60	47	N5	69	81
I/O88	I/O110	I/O99	I/O186(A)	—	33	61	48	N6	70	82
—	—	—	I/O185(B)	—	—	—	—	—	71	83
I/O87	I/O109	I/O98	I/O184(A)	39	34	62	49	N7	72	84
	I/O108	I/O97	I/O183(A)			63	50	M8	73	85
GND	GND	GND	GND	40	35	64	51	GND[2]	74	86
I/O86	I/O107	I/O96	I/O182(A)	41	36	65	52	M9	75	87
—	—	—	I/O181(B)	—	—	—	—	—	76	88
—	I/O106	—	I/O180(A)	—	—	—	53	M10	77	89
I/O85	I/O105	I/O95	I/O179(A)	42	37	66	54	M11	78	90
CS	CS	CS	CS	43	38	67	55	L8	79	91
I/O84	I/O104	I/O94	I/O178(A)	44	39	68	56	M12	80	92
—	—	—	I/O177(B)	—	—	—	—	—	81	93
I/O83	I/O103	I/O93	I/O176(A)	45	40	69	57	N8	82	94
—	—	—	VDD	—	—	—	—	PWR[1]	83	95
VCC	VCC	VCC	VCC	46	41	70	58	PWR[1]	84	96
I/O82	I/O102	I/O92	I/O175(A)	47	42	71	59	N11	85	97
I/O81	I/O101	I/O91	I/O174(A)	—	—	72	60	N12	86	98
—	—	—	I/O173(B)	—	—	—	—	—	87	99
I/O80	I/O100	I/O90	I/O172(A)	48	43	73	61	N13	88	100
I/O79	I/O99	I/O89	I/O171(A)	—	44	74	62	P8	89	101
—	—	—	I/O170(A)	—	—	—	—	P9	90	102
—	—	—	I/O169(B)	—	—	—	—	—	—	103
I/O78	I/O98	I/O88	I/O168(A)	49	45	75	63	P10	91	104
—	I/O97	I/O87	I/O167(A)	—	—	76	64	P11	92	105
—	—	—	I/O166(A)	—	—	—	—	P12	93	106
GND	GND	GND	GND	—	—	77	65	GND[2]	94	107
—	—	—	I/O165(B)	—	—	—	—	—	—	108
I/O77	I/O96	I/O86	I/O164(A)	50	46	78	66	P13	95	109
I/O76	I/O95	I/O85	I/O163(A)	—	47	79	67	P14	96	110
—	—	—	I/O162(A)	—	—	—	—	R8	97	111
—	—	—	I/O161(B)	—	—	—	—	—	—	112
I/O75	I/O94	I/O84	I/O160(A)	51	48	80	68	R9	98	113
I/O74	I/O93	I/O83	I/O159(A)	—	—	81	69	R10	99	114
—	—	—	I/O158(A)	—	—	—	—	R11	100	115
—	—	—	I/O157(B)	—	—	—	—	—	—	116
—	I/O92	—	I/O156(A)	—	—	—	70	R12	101	117
I/O73	I/O91	I/O82	I/O155(A)	52	49	82	71	R13	102	118
—	—	—	I/O154(A)	—	—	—	—	R14	103	119
RESET	RESET	RESET	RESET	53	50	83	72	R15	104	120

Notes: 1. PWR = Pins connected to power plane = F1, E4/E5, L2, R4, K15, L12, E14, A12.
2. GND = Pins connected to ground plane = L4, M4, N9, N10, E12, D12, C7, C6.

Pinout Assignment (Continued)

Right Side (Bottom to Top)										
AT6002	AT6003	AT6005	AT6010	84 PLCC	100 VQFP	132 PQFP	144 TQFP	180 CPGA	208 PQFP	240 PQFP
—	—	—	I/O153(A)	—	—	—	—	P15	105	121
I/O72	I/O90	I/O81	I/O152(A)	54	51	84	73	N15	106	122
—	I/O89	I/O80	I/O151(A)	—	—	85[3]	74	M15	107	123
—	—	—	I/O150(B)	—	—	—	—	—	—	124
—	—	—	VCC	—	—	—	—	PWR[1]	108	125
—	—	—	I/O149(A)	—	—	—	—	L15	109	126
—	—	—	GND	—	—	—	—	GND[2]	110	127
—	I/O88	—	I/O148(A)	—	—	85[4]	75	J15	111	128
I/O71	I/O87	I/O79	I/O147(A)	55	52	86	76	H15	112	129
—	—	—	I/O146(B)	—	—	—	—	—	—	130
—	—	—	I/O145(A)	—	—	—	—	N14	113	131
I/O70	I/O86	I/O78	I/O144(A)	—	—	87	77	M14	114	132
I/O69	I/O85	I/O77	I/O143(A)	56	53	88	78	L14	115	133
—	—	—	I/O142(B)	—	—	—	—	—	—	134
—	—	—	I/O141(A)	—	—	—	—	K14	116	135
I/O68	I/O84	I/O76	I/O140(A)	—	54	89	79	J14	117	136
I/O67	I/O83	I/O75	I/O139(A)	57	55	90	80	H14	118	137
—	—	—	I/O138(B)	—	—	—	—	—	—	138
I/O66	I/O82	I/O74	I/O137(A)	—	—	91	81	M13	119	139
I/O65	I/O81	I/O73	I/O136(A)	58	56	92	82	L13	120	140
I/O64	I/O80	I/O72	I/O135(A)	—	57	93	83	K13	121	141
—	—	—	I/O134(B)	—	—	—	—	—	122	142
I/O63	I/O79	I/O71	I/O133(A)	59	58	94	84	J13	123	143
—	I/O78	I/O70	I/O132(A)	—	—	95	85	H13	124	144
GND	GND	GND	GND	60	59	96	86	GND[2]	125	145
VSS	VSS	VSS	VSS	61	60	97	87	GND[2]	126	146
I/O62	I/O77	I/O69	I/O131(A)	62	61	98	88	K12	127	147
—	—	—	I/O130(B)	—	—	—	—	—	128	148
—	I/O76	—	I/O129(A)	—	—	—	89	J12	129	149
I/O61	I/O75	I/O68	I/O128(A)	63	62	99	90	H12	130	150
I/O60	I/O74	I/O67	I/O127(A)	64	63	100	91	H11	131	151
—	—	—	I/O126(B)	—	—	—	—	—	132	152
I/O59	I/O73	I/O66	I/O125(A)	65	64	101	92	G12	133	153
I/O58	I/O72	I/O65	I/O124(A)	66	65	102	93	F12	134	154
VDD	VDD	VDD	VDD	67	66	103	94	PWR[1]	135	155
VCC	VCC	VCC	VCC	68	67	104	95	PWR[1]	136	156
I/O57	I/O71	I/O64	I/O123(A)	—	—	105	96	G13	137	157
—	—	—	I/O122(B)	—	—	—	—	—	138	158
I/O56	I/O70	I/O63	I/O121(A)	69	68	106	97	F13	139	159
I/O55	I/O69	I/O62	I/O120(A)	—	69	107	98	E13	140	160
—	—	—	I/O119(A)	—	—	—	—	D13	141	161
—	—	—	I/O118(B)	—	—		—	—	—	162
I/O54	I/O68	I/O61	I/O117(A)	70	70	108	99	C13	142	163
—	I/O67	I/O60	I/O116(A)	—	—	109	100	G14	143	164
—	—	—	I/O115(A)	—	—	—	—	F14	144	165
GND	GND	GND	GND	—	—	110	101	GND[2]	145	166
—	—	—	VSS	—	—	—	—	GND[2]	146	167
—	—	—	I/O114(B)	—	—	—	—	—	—	168
I/O53	I/O66	I/O59	I/O113(A)	71	71	111	102	D14	147	169
I/O52	I/O65	I/O58	I/O112(A)	—	72	112	103	C14	148	170
—	—	—	I/O111(A)	—	—	—	—	B14	149	171
—	—	—	I/O110(B)	—	—	—	—	—	—	172
I/O51	I/O64	I/O57	I/O109(A)	72	73	113	104	G15	150	173
I/O50	I/O63	I/O56	I/O108(A)	—	—	114	105	F15	151	174
—	—	—	I/O107(A)	—	—	—	—	E15	152	175
—	—	—	I/O106(B)	—	—	—	—	—	—	176
—	I/O62	—	I/O105(A)	—	—	—	106	D15	153	177
I/O49	I/O61	I/O55	I/O104(A)	73	74	115	107	C15	154	178
—	—	—	I/O103(A)	—	—	—	—	B15	155	179
M2	M2	M2	M2	74	75	116	108	A15	156	180

Notes: 1. PWR = Pins connected to power plane = F1, E4/E5, L2, R4, K15, L12, E14, A12.
2. GND = Pins connected to ground plane = L4, M4, N9, N10, E12, D12, C7, C6.
3. 85 = Pin 85 on AT6005.
4. 85 = pin 85 on AT6003 and AT6010.

Pinout Assignment (Continued)

Top Side (Right to Left)										
AT6002	AT6003	AT6005	AT6010	84 PLCC	100 VQFP	132 PQFP	144 TQFP	180 CPGA	208 PQFP	240 PQFP
M1	M1	M1	M1	75	76	117	109	D11	157	181
—	—	—	I/O102(A)	—	—	—	—	D10	158	182
I/O48	I/O60	I/O54	I/O101(A)	76	77	118	110	D9	159	183
—	I/O59	—	I/O100(A)	—	—	—	111	A14	160	184
—	—	—	I/O99(B)	—	—	—	—	—	—	185
—	—	—	VCC	—	—	—	—	PWR[1]	161	186
—	—	—	I/O98(A)	—	—	—	—	A13	162	187
—	—	—	GND	—	—	—	—	GND[2]	163	188
—	I/O58	I/O53	I/O97(A)	—	—	119	112	A11	164	189
I/O47	I/O57	I/O52	I/O96(A)	77	78	120	113	A10	165	190
—	—	—	I/O95(B)	—	—	—	—	—	—	191
—	—	—	I/O94(A)	—	—	—	—	A9	166	192
I/O46	I/O56	I/O51	I/O93(A)	—	—	121	114	B13	167	193
I/O45	I/O55	I/O50	I/O92(A)	78	79	122	115	B12	168	194
—	—	—	I/O91(B)	—	—	—	—	—	—	195
—	—	—	I/O90(A)	—	—	—	—	B11	169	196
I/O44	I/O54	I/O49	I/O89(A)	—	80	123	116	B10	170	197
I/O43	I/O53	I/O48	I/O88(A)	79	81	124	117	B9	171	198
—	—	—	I/O87(B)	—	—	—	—	—	—	199
I/O42	I/O52	I/O47	I/O86(A)	—	—	125	118	C12	172	200
I/O41	I/O51	I/O46	I/O85(A)	80	82	126	119	C11	173	201
I/O40	I/O50	I/O45	I/O84(A)	—	83	127	120	C10	174	202
—	—	—	I/O83(B)	—	—	—	—	—	175	203
I/O39	I/O49	I/O44	I/O82(A)	81	84	128	121	C9	176	204
—	I/O48	I/O43	I/O81(A)	—	—	129	122	D8	177	205
GND	GND	GND	GND	82	85	130	123	GND[2]	178	206
I/O38	I/O47	I/O42	I/O80(A)	83	86	131	124	D7	179	207
—	—	—	I/O79(B)	—	—	—	—	—	180	208
—	I/O46	—	I/O78(A)	—	—	—	125	D6	181	209
I/O37 or A16	I/O45 or A16	I/O41 or A16	I/O77(A) or A16	84	87	132	126	D5	182	210
CLOCK	CLOCK	CLOCK	CLOCK	1	88	1	127	E8	183	211
I/O36 or A15	I/O44 or A15	I/O40 or A15	I/O76(A) or A15	2	89	2	128	D4	184	212
—	—	—	I/O75(B)	—	—	—	—	—	185	213
I/O35 or A14	I/O43 or A14	I/O39 or A14	I/O74(A) or A14	3	90	3	129	C8	186	214
—	—	—	VDD	—	—	—	—	PWR[1]	187	215
VCC	VCC	VCC	VCC	4	91	4	130	PWR[1]	188	216
I/O34 or A13	I/O42 or A13	I/O38 or A13	I/O73(A) or A13	5	92	5	131	C5	189	217
I/O33	I/O41	I/O37	I/O72(A)	—	—	6	132	C4	190	218
—	—	—	I/O71(B)	—	—	—	—	—	191	219
I/O32 or A12	I/O40 or A12	I/O36 or A12	I/O70(A) or A12	6	93	7	133	C3	192	220
I/O31	I/O39	I/O35	I/O69(A)	—	94	8	134	B8	193	221
—	—	—	I/O68(A)	—	—	—	—	B7	194	222
—	—	—	I/O67(B)	—	—	—	—	—	—	223
I/O30 or A11	I/O38 or A11	I/O34 or A11	I/O66(A) or A11	7	95	9	135	B6	195	224
—	I/O37	I/O33	I/O65(A)	—	—	10	136	B5	196	225
—	—	—	I/O64(A)	—	—	—	—	B4	197	226
GND	GND	GND	GND	—	—	11	137	GND[2]	198	227
—	—	—	I/O63(B)	—	—	—	—	—	—	228
I/O29 or A10	I/O36 or A10	I/O32 or A10	I/O62(A) or A10	8	96	12	138	B3	199	229
I/O28	I/O35	I/O31	I/O61(A)	—	97	13	139	B2	200	230
—	—	—	I/O60(A)	—	—	—	—	A8	201	231
—	—	—	I/O59(B)	—	—	—	—	—	—	232
I/O27 or A9	I/O34 or A9	I/O30 or A9	I/O58(A) or A9	9	98	14	140	A7	202	233
I/O26	I/O33	I/O29	I/O57(A)	—	—	15	141	A6	203	234
—	—	—	I/O56(A)	—	—	—	—	A5	204	235
—	—	—	I/O55(B)	—	—	—	—	—	—	236
—	I/O32	—	I/O54(A)	—	—	—	142	A4	205	237
I/O25 or A8	I/O31 or A8	I/O28 or A8	I/O53(A) or A8	10	99	16	143	A3	206	238
—	—	—	I/O52(A)	—	—	—	—	A2	207	239
M0	M0	M0	M0	11	100	17	144	A1	208	240

Notes: 1. PWR = Pins connected to power plane = F1, E4/E5, L2, R4, K15, L12, E14, A12.
2. GND = Pins connected to ground plane = L4, M4, N9, N10, E12, D12, C7, C6.

A.C. Timing Characteristics

Delays are based on fixed load. Loads for each type of device are described in the notes. Delays are in nanoseconds. Worst case: Vcc = 4.75 V to 5.25 V. Temperature = 0°C to 70°C.

Cell Function	Parameter	From	To	Load	-2	-4	Units
Wire (4)	t_{PD} (max) (4)	A, B, L	A, B	1	1.2	1.8	ns
NAND	t_{PD} (max)	A, B, L	B	1	2.2	3.2	ns
XOR	t_{PD} (max)	A, B, L	A	1	2.4	4.0	ns
AND	t_{PD} (max)	A, B, L	B	1	2.2	3.2	ns
MUX	t_{PD} (max)	A, B	A	1	2.3	4.0	ns
		L	A	1	3.0	4.9	ns
D-Flip-Flop (5)	t_{setup} (min)	A, B, L	CLK		2.0	3.0	ns
D-Flip-Flop (5)	t_{hold} (min)	CLK	A, B, L		0.0	0.0	ns
D-Flip-Flop	t_{PD} (max)	CLK	A	1	2.0	3.0	ns
Bus Driver	t_{PD} (max)	A	L	2	2.6	4.0	ns
Repeater	t_{PD} (max)	L, E	E	3	1.6	2.3	ns
		L, E	L	2	2.1	3.0	ns
Column Clock	t_{PD} (max)	GCLK, A, ES	CLK	3	2.4	3.0	ns
Column Reset	t_{PD} (max)	GRES, A, EN	RES	3	2.4	3.0	ns
Clock Buffer (5)	t_{PD} (max)	CLOCK PIN	GCLK	4	2.0	2.9	ns
Reset Buffer (5)	t_{PD} (max)	RESET PIN	GRES	5	1.9	2.8	ns
TTL Input (1)	t_{PD} (max)	I/O	A	3	1.2	1.5	ns
CMOS Input (2)	t_{PD} (max)	I/O	A	3	1.4	2.3	ns
Fast Output (3)	t_{PD} (max)	A	I/O PIN	6	3.5	6.0	ns
Slow Output (3)	t_{PD} (max)	A	I/O PIN	6	8.0	12.0	ns
Output Disable (5)	t_{PXZ} (max)	L	I/O PIN	6	3.3	5.5	ns
Fast Enable (3, 5)	t_{PZX} (max)	L	I/O PIN	6	4.0	6.5	ns
Slow Enable (3, 5)	t_{PZX} (max)	L	I/O PIN	6	8.5	12.5	ns

Device	Cell Types	Outputs	Icc (max)
Cell (6)	Wire, XWire, Half-Adder, Flip-Flop	A, B	4.5 µA/MHz
Bus (6)	Wire, XWire, Half-Adder, Flip-Flop, Repeater	L	2.5 µA/MHz
Column Clock (6)	Column Clock Driver	CLK	40 µA/MHz

Notes:
1. TTL buffer delays are measured from a V_{IH} of 1.5 V at the pad to the internal V_{IH} at A. The input buffer load is constant.
2. CMOS buffer delays are measured from a V_{IH} of 1/2 V_{CC} at the pad to the internal V_{IH} at A. The input buffer load is constant.
3. Buffer delay is to a pad V_{IH} of 1.5 V with one output switching.
4. Max specifications are the average of max t_{PDLH} and t_{PDHL}
5. Parameter based on characterization and simulation; not tested in production.
6. Exact power calculation is available in an Atmel application note.

Load Definition:
1. Load of one A or B input
2. Load of one L input
3. Constant Load
4. Load of 28 Clock Columns
5. Load of 28 Reset Columns
6. Tester Load of 50 pF

Absolute Maximum Ratings*

Supply Voltage (V_{CC})	-0.5 V to +7.0 V
DC Input Voltage (V_{IN})	-0.5 V to VCC + 0.5 V
DC Output Voltage (V_{ON})	-0.5 V to VCC + 0.5 V
Storage Temperature Range (TSTG)	-65°C to +150°C
Power Dissipation (PD)	1500 mW
Lead Temperature (T_L) (Soldering, 10 sec.)	260°C
ESD (R_{ZAP}=1.5K, C_{ZAP}=100 pF)	2000 V

*NOTICE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

2

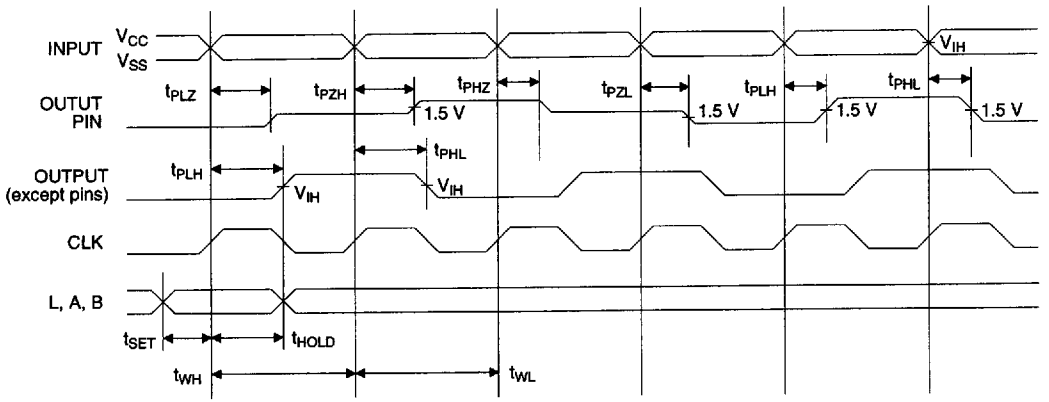
D.C. and A.C. Operating Range

		AT6002-2/4 AT6003-2/4 AT6005-2/4 AT6010-2/4 Commercial	AT6002-2/4 AT6003-2/4 AT6005-2/4 AT6010-2/4 Industrial	AT6002-4 AT6003-4 AT6005-4 AT6010-4 Military
Operating Temperature (Case)		0°C - 70°C	-40°C - 85°C	-55°C - 125°C
V_{CC} Power Supply		5 V ± 5%	5 V ± 10%	5 V ± 10%
Input Voltage Level (TTL)	High (V_{IHT})	2.0 V - V_{CC}	2.0 V - V_{CC}	2.0 V - V_{CC}
	Low (V_{ILT})	0 V - 0.8 V	0 V - 0.8 V	0 V - 0.8 V
Input Voltage Level (CMOS)	High (V_{IHC})	70% - 100% V_{CC}	70% - 100% V_{CC}	70% - 100% V_{CC}
	Low (V_{ILC})	0 - 30% V_{CC}	0 - 30% VCC	0 - 30% V_{CC}
Input Signal Transition Time	(T_{IN})	50 ns (max)	50 ns (max)	50 ns (max)

D.C. Characteristics

Symbol	Parameter	Conditions		Min	Max	Units
V_{IH}	High-Level Input Voltage	Commercial	CMOS	70% V_{CC}	V_{CC}	V
			TTL	2.0	V_{CC}	V
V_{IL}	Low-Level Input Voltage	Commercial	CMOS	0	20% V_{CC}	V
			TTL	0	0.8	V
V_{OH}	High-Level Output Voltage	Commercial	I_{OH} = -4 mA, V_{CC} min	3.9		V
			I_{OH} = -16 mA, V_{CC} min	3.0		V
V_{OL}	Low-Level Output Voltage	Commercial	I_{OL} = -4 mA, V_{CC} min		0.4	V
			I_{OL} = -16 mA, V_{CC} min		0.5	V
I_{OZH}	High-Level Tristate Output Leakage Current	V_O = V_{CC} (max)			10	µA
I_{OZL}	Low-Level Tristate	Without Pull-Up, V_O = V_{SS}		-10		µA
	Output Leakage Current	With Pull-Up, V_O = V_{SS}		-500		µA
I_{IH}	High-Level Input Current	VIN = V_{CC} (max)			10	µA
I_{IL}	Low-Level Input Current	Without Pull-Up, V_{IN} = V_{SS}		-10		µA
		With Pull-Up, V_{IN} = V_{SS}		-500		µA
I_{CC}	Power Consumption	Without Internal Oscillator (Standby)			500	µA
C_{IN}	Input Capacitance	All Pins			10	pF

Device Timing: During Operation



Ordering Information

Usable Gates	Speed Grade (ns)	Ordering Code	Package	Operation Range
2,000	2	AT6002-2AC AT6002A-2AC AT6002-2JC AT6002-2QC	100A 144A 84J 132Q	Commercial (0°C to 70°C)
2,000	4	AT6002-4AC AT6002A-4AC AT6002-4JC AT6002-4QC	100A 144A 84J 132Q	Commercial (0°C to 70°C)
		AT6002-4AI AT6002A-4AI AT6002-4JI AT6002-4QI	100A 144A 84J 132Q	Industrial (-40°C to 85°C)

Usable Gates	Speed Grade (ns)	Ordering Code	Package	Operation Range
3,000	2	AT6003-2AC AT6003A-2AC AT6003-2JC AT6003-2QC	100A 144A 84J 132Q	Commercial (0°C to 70°C)
3,000	4	AT6003-4AC AT6003A-4AC AT6003-4JC AT6003-4QC	100A 144A 84J 132Q	Commercial (0°C to 70°C)
		AT6003-4AI AT6003A-4AI AT6003-4JI AT6003-4QI	100A 144A 84J 132Q	Industrial (-40°C to 85°C)

Usable Gates	Speed Grade (ns)	Ordering Code	Package	Operation Range
5,000	2	AT6005-2AC AT6005A-2AC AT6005-2JC AT6005-2QC AT6005-2UC	100A 144A 84J 132Q 180U	Commercial (0°C to 70°C)
5,000	4	AT6005-4AC AT6005A-4AC AT6005-4JC AT6005-4QC AT6005-4UC	100A 144A 84J 132Q 180U	Commercial (0°C to 70°C)
		AT6005-4AI AT6005A-4AI AT6005-4JI AT6005-4QI AT6005-4UI	100A 144A 84J 132Q 180U	Industrial (-40°C to 85°C)

Ordering Information

Usable Gates	Speed Grade (ns)	Ordering Code	Package	Operation Range
10,000	2	AT6010A-2AC AT6010-2QC AT6010-2UC AT6010A-2QC AT6010H-2QC	144A 132Q 180U 208Q 240Q	Commercial (0°C to 70°C)
10,000	4	AT6010A-4AC AT6010-4QC AT6010-4UC AT6010A-4QC AT6010H-4QC	144A 132Q 180U 208Q 240Q	Commercial (0°C to 70°C)
		AT6010A-4AI AT6010A-4QI AT6010-4UI AT6010A-4QI AT6010H-4UI	144A 132Q 180U 208Q 240Q	Industrial (-40°C to 85°C)

Ordering Information

Package Type	
84J	84 Lead, Plastic J-Leaded Chip Carrier (PLCC)
100A	100 Lead, Very Thin (1.0 mm) Plastic Gull Wing Quad Flat Package (VQFP)
144A	144 Lead, Thin (1.4 mm) Plastic Gull Wing Quad Flat Package (TQFP)
180U	180 Pin, Ceramic Pin Grid Array (PGA)
132Q	132 Lead, Bumpered Plastic Gull Wing Quad Flat Package (BQFP)
208Q	208 Lead, Plastic Gull-Wing Quad Flat Package (PQFP)
240Q	240 Lead, Plastic Gull-Wing Quad Flat Package (PQFP)

Field Programmable Gate Array

Configuration Guide

AT6000 Series Configuration

Configuration is the process of loading a design into an AT6000 Series field programmable gate array (FPGA). AT6000 Series devices are SRAM-based and can be configured any number of times. The entire device or select portions of a design can be configured. Sections of the device can be configured while others continue to operate undisturbed.

Configuration data is transferred to the device in one of six modes. Full configuration takes only milliseconds. Partial configuration takes even less time and is a function of design density.

Configuration is controlled by dedicated configuration pins and dual-function pins that double as I/O pins when the device is operating. Three pins, M0, M1 and M2 determine the configuration mode (Table 1). The number of dual-function pins required for each mode varies (Table 2).

One of the modes is automatically initiated after power-up reboot; the others are initiated by the user. Configuration data can come from a variety of external logic sources, including a PC parallel port, microprocessor, EPROM or E^2PROM Serial Configuration Memory (AT17128).

The user determines the configuration mode for loading the bit pattern into the device. The Integrated Development System generates the SRAM bit pattern required to configure an AT6000 Series FPGA. Many factors can influence the user's choice of configuration mode, including device size, board space, required configuration speed, number of devices to be configured, and design size.

This document suggests guidelines for device configuration and describes each of the configuration modes in detail.

A basic understanding of the device architecture, as described in the AT6000 Series data sheet, is assumed.

Features

Variety of Formats

- PC Parallel Port
- Microprocessor
- Serial/Parallel EPROM
- Serial/Parallel E^2PROM

Configuration Windows

- Full or Partial Reconfiguration
- Bit-Stream Compression Algorithm

Reprogrammable

- Download Configuration any Number of Times
- Reconfigure In-System Down to Cell Level

Fast

- Full Configuration: 1-8 Milliseconds
- Partial Configuration: 0.2 µseconds/Cell

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Table 1. AT6000 Series Configuration Modes

Mode	Description	M2	M1	M0	Application
0	Configuration Reset	0	0	0	Clearing the Device
1	Address Count-Up, External CCLK	0	0	1	Fast Configuration; Parallel EPROM
2	Address Count-Down, External CCLK	0	1	0	Fast Configuration; Parallel EPROM
3	Bit-Sequential, External CCLK	0	1	1	Serial Communication Port to UART
4	Bit-Sequential, Internal CCLK	1	0	0	Serial EPROM; Auto Configuration
5	Address Count-Up, Internal CCLK	1	0	1	Parallel EPROM
6	Byte-Sequential, External CCLK	1	1	0	Parallel Port of Microprocessor

Configuration Modes

Powering up an AT6000 Series FPGA is a three-step process. When power is first applied, the device enters an initialization state that takes up to 16 milliseconds and resets the SRAM to all zeros. Cells in the array become cross wires with no A or B inputs selected, all bus drivers are switched off, repeaters are disabled, I/Os are set as TTL inputs with the pull-up enabled, column clocks are set to "0," and column resets are set to "1."

After initialization, the device enters the configuration state and writes to the memory bits that control cell functionality and interconnection.

Seven configuration modes are available:

Mode 0:Configuration Reset
Mode 1:Address Count-Up, External CCLK
Mode 2:Address Count-Down, External CCLK
Mode 3:Bit-Sequential, External CCLK
Mode 4:Bit Sequential, Internal CCLK
Mode 5:Address Count-Up, Internal CCLK
Mode 6:Byte-Sequential, External CCLK

Mode 0 is not a true configuration mode because it does not load a design into the FPGA. Instead, mode 0 initiates the reboot sequence and clears the device, preparing it for configuration or reconfiguration.

Modes 1, 2 and 5 generate external address outputs so the user can conveniently access sequential data from a standard parallel EPROM. The generated output addresses bear no relation to the internal addresses of the FPGA's configuration SRAM, they simply count up or down with each CCLK edge to create a sequential byte stream. Mode 6 is similar to modes 1, 2 and 5 but assumes a system-generated bit stream and does not generate external address outputs. Modes 3 and 4 use a serial bit stream received from the system, an industry-standard E^2PROM (AT17C65/128/256) or the download cable provided with the Integrated Development System. The data in each byte is serialized with the least-significant-bit supplied first. Mode 4 can be initiated automatically by the FPGA with the AT17C65/128/256 Serial Configuration Memory.

Modes 3 and 4 will typically be the most popular configuration modes because they require the fewest pins and receive data from small foot-print serial E^2PROMs that take up little board space.

Pins used for Configuration

AT6000 Series FPGAs have three kinds of pins: dedicated I/O pins, dedicated configuration pins, and dual-function pins which act as I/O during operation but are used for various control signals during configuration. (For more on device pins refer to the AT6000 Series data sheet.)

Dedicated Configuration Pins

There are six signals dedicated to programming: M0, M1, M2, CCLK, $\overline{\text{CON}}$ and $\overline{\text{CS}}$.

M0, M1, M2

The mode pins are inputs that determine the configuration mode to be used. Table 1 (this page) lists the states for each configuration mode. M0, M1 and M2 can be fixed in modes 1 through 6 and ignored. Mode 0, configuration reset, can be initiated by asynchronously driving M0, M1 and M2 low, then returning them to the proper mode selection value.

CCLK

CCLK is the configuration clock signal. It is an input or an output depending on the mode of operation. In modes 1, 2, 3 and 6 it is an input, in modes 4 and 5 it is an output with a typical frequency of 1 MHz. In all modes, the rising edge of the CCLK signal is used to sample inputs and change outputs.

$\overline{\text{CON}}$

CON is a bidirectional open-collector pin that provides the configuration control and status signal. Configuration starts on the first CCLK edge when $\overline{\text{CON}}$ is driven and held low. Configuration continues until $\overline{\text{CON}}$ is pulled high by a pull-up or by the configuration system. $\overline{\text{CON}}$ is driven low by the device until

Table 2. Dual-Function Pin Usage

N = Not used, R = Required, O = Optional

Mode	Minimum Dual-Function Pins	Optional Dual-Function Pins	A0-16 Outputs	D0 Input	D1-7 Inputs	$\overline{\text{CHECK}}$ Input	$\overline{\text{ERR}}$ Output	$\overline{\text{CSOUT}}$ Output
0	0	0	N	N	N	N	N	N
1	25	4	R	R	R	O	O	O
2	25	4	R	R	R	O	O	O
3	1	3	N	R	N	O	O	O
4	1	3	N	R	N	O	O	O
5	25	4	R	R	R	O	O	O
6	8	3	N	R	R	O	O	O

configuration is complete. The device moves to the operation state on the first CCLK edge after $\overline{\text{CON}}$ is high.

$\overline{\text{CS}}$

$\overline{\text{CS}}$ is the configuration chip select pin. $\overline{\text{CS}}$ must be low for configuration to occur. Pulling $\overline{\text{CS}}$ high during configuration does not stop the process, but the pin should be held low throughout configuration. $\overline{\text{CS}}$ can be used to cascade devices (see Figures 9 and 14) and create an addressed, multiple-device programming system (see Figure 15).

Dual-Function Pins

Dual-function pins are programming pins during configuration and I/O pins during operation. The number of dual-function pins used during configuration varies from mode to mode. Some dual-function pins act as configuration status pins and are optional regardless of mode. The optional pins are most useful when cascading devices to program multiple FPGAs from a single data source. Table 2 lists the dual-function pins used with each mode.

D0-D7

D0-D7 are data input pins. Parallel modes 1, 2, 5 and 6 use all eight data inputs, serial modes 3 and 4 use only one, D0.

$\overline{\text{CEN}}$ or I/O

During address count-up/down configuration, $\overline{\text{CEN}}$ is an output. $\overline{\text{CEN}}$ can be used as the output enable of a parallel EPROM. In this case, it should be configured as a constant high, and not used as a configurable I/O pin. For the AT6002, AT6003, and AT6005, $\overline{\text{CEN}}$ output is enabled after powerup and/or reboot. It switeches low one clock after CON is activated. It may become inactive one clock after the loading of the configuration control register during a configuration download, depending on the value of bit B7. $\overline{\text{CEN}}$ is active for modes 1,2,3,4,5, and 6. For the AT6010, $\overline{\text{CEN}}$ output is disabled after powerup and/or reboot. It may become active one clock after the loading of the configuration control register during a configuration download, depending on the value of B7. $\overline{\text{CEN}}$ is active for modes 1,2, and 5 only.

A0-A16

A0-A16 are address output signals, used by modes 1, 2 and 5, to drive an EPROM or other external addressed-memory device.

$\overline{\text{CSOUT}}$

CSOUT drives $\overline{\text{CS}}$ of the next device in a configuration chain.

$\overline{\text{CHECK}}$

$\overline{\text{CHECK}}$ is an input that enables an internal SRAM checking feature when used without B3 of the Configuration Control Register.

ERR

ERR is an output that switches low when an error is detected. It is used with the $\overline{\text{CHECK}}$ function, or when protocol errors occur during configuration. CHECK and $\overline{\text{ERR}}$ work together to perform simple and advanced diagnostic tests. For example, they can be used to verify the accuracy of a configuration run. With the $\overline{\text{CHECK}}$ pin low, download the configuration file a second time. The device systematically compares the data values in the configuration file with the data already programmed into the device's SRAM. If a mismatch is found, the $\overline{\text{ERR}}$ pin switches and remains low until the end of the configuration cycle.

Pin Status

The status of dual-function pins is determined by the device state. All I/Os are disabled during initialization. To move from the initialization state to configuration, the $\overline{\text{CON}}$ and $\overline{\text{CS}}$ pins are driven low. During configuration, the dual-function pins used by the selected mode are converted to inputs and outputs as required. To move from the configuration state to operation, the configuration file must be loaded completely and either $\overline{\text{CON}}$ or $\overline{\text{CS}}$ must be high. During operation, the I/O pins behave according to the specified design.

Control Register

The Integrated Development System generates the bit-stream file used to configure the FPGA. In addition to the actual data to be loaded into the SRAM, the bit stream loads a control register containing eight bits used to control various configuration sequence parameters (Figure 1).

Figure 1. Control Register

B7	B6	B5	B4	B3	B2	B1	B0

B0

B0 controls the value of the device's memory address counter after each configuration sequence. The default resets the value, so subsequent configuration sequences load the configuration file from the same address. In modes 1 and 5, the default address is 0000, in mode 2 it is 1FFFF. When B0 is set, the memory address counter retains its last value, so the user can store multiple designs sequentially in an External Memory Device.

B1

B1 controls loading of a jump address into the device's memory address counter. The default ignores any jump addresses. With B1 set, the memory address counter jumps to the specified address. Using B1, configuration files can be stored as a continuous stream or as a pointer-based list.

B2

B2 controls operation of the dual-function pin $\overline{\text{CSOUT}}$. When B2 is set, this pin is disabled. This is useful when a minimum pin-count configuration is desired.

B3

B3 controls the operation of the dual-function pins $\overline{\text{ERR}}$ and $\overline{\text{CHECK}}$. When B3 is set, both pins are disabled. This is useful when a minimum pin-count configuration is desired, or when design security is a concern.

B4

B4 controls the writing of configuration data after the initialization state. When B4 is set, configuration data can not be written into the device by subsequent configuration cycles. B4 can only be reset by rebooting the device.

B5 and B6

B5 and B6 control the operation of the global clock signal received through the CLOCK pin:

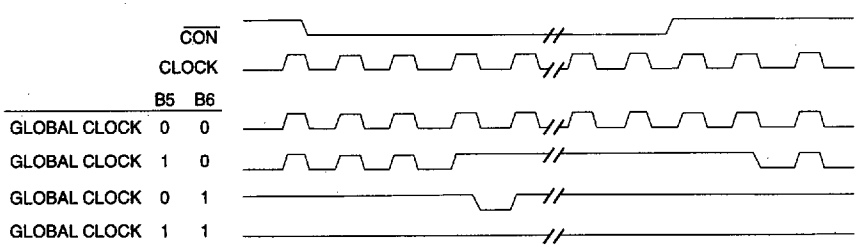
B5	B6	Global Clock Operation
0	0	Normal operation.
1	0	Stops after third rising edge of CLOCK after CON is low. Continues after second rising edge of CLOCK after CON is high.
0	1	Stops after fourth rising edge of CLOCK after CON is high. Each configuration cycle thereafter, it receives one pulse after the third rising edge of CLOCK after CON is low.
1	1	Stops at second rising edge of CLOCK after CON is high. Remains stopped regardless of CON.

Figure 2 shows the waveforms associated with each combination.

B7

B7 controls the $\overline{\text{CEN}}$ pin. When B7 is set, $\overline{\text{CEN}}$ is disabled.

Figure 2. Global Clock Signal During Operation



Configuration State Machine

Configuration is executed by a synchronous state machine that controls the flow of configuration data into the FPGA (Figure 3). The state machine is clocked by CCLK whether the signal is externally supplied or generated internally. On each CCLK cycle a different byte or bit of the configuration file is loaded into the state machine.

Data flow is controlled by the external input signals M0, M1, M2, $\overline{CON}$, $\overline{CS}$, $\overline{CHECK}$, D0-D7 and the values in the configuration control register. The state machine generates all the internal control signals as well as the A0-A16 output signals, $\overline{ERR}$ output, and $\overline{CSOUT}$ signal. Data is loaded into the device in a stream format and has no absolute address.

The process starts on power-up or when a mode 0 reset is applied. The reboot phase lasts for approximately 8000 up to approximately 16000 internal clock cycles while all the internal SRAM cells are written to a "0" value. During reboot the mode pins are sampled and the configuration-clock output starts.

Mode 4 supports automatic configuration. During reboot, the CCLK pin is enabled for output. After reboot, mode 4 releases the $\overline{CON}$ pin, allowing it to be pulled high, and then drives it low again to begin a configuration cycle automatically.

In the modes 1,2,3 and 6, CCLK remains an input but is ignored until the reboot process is complete. After reboot, the other modes release $\overline{CON}$ and allow it to float high. Control of the state machine is then transferred from the internal clock to the CCLK input signal. The device remains in idle until the $\overline{CON}$ pin is driven low.

Driving $\overline{CON}$ low puts the device in the preamble check loop, a synchronizing procedure for both parallel and serial configuration modes. Configuration is dependent on the sequence of data, and the preamble specifies the first byte of the data stream. In modes 3 and 4, the preamble also defines the byte boundary of serial data, which may be parallel before being processed by the state machine.

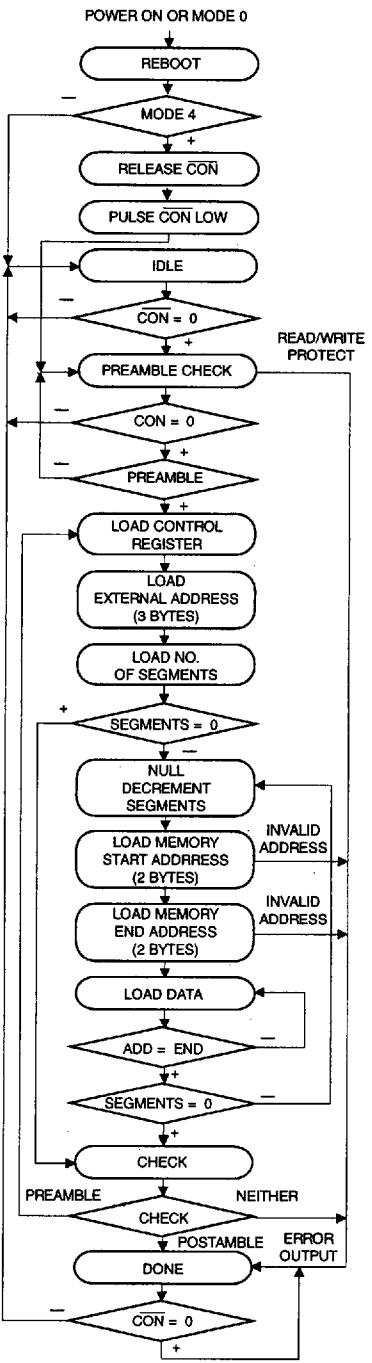
The first error test is done during the preamble check. If a read or write protect bit appears in the control register of the preamble, the $\overline{ERR}$ pin goes low and the device goes directly to the done state.

After the preamble check, the state machine loads the configuration control register and drives and holds the $\overline{CON}$ signal low until configuration is complete. Loading the configuration control register puts the next byte in the stream file into the control register, which controls features and variations in the configuration process.

The state machine then loads the next three bytes into a temporary register used to parallel-load the external address counter. This action is similar to a microprocessor "jump" command. The address bytes are loaded in all modes, but the jump can only be used by modes 1, 2 and 5.

The next byte in the stream file indicates the number of data strings, or segments. A single file can have 0 to 255 segments. The byte is loaded into a counter which is decremented at the end of each data string until it reaches zero and configuration is complete.

Figure 3. Configuration State Machine



If the register count is not zero, the state machine loads a null byte. If the B1 bit of the control register is equal to one the first time the state machine enters the null state, the external address is loaded. The byte loaded, while in the null state, is not used. If the segment count is zero, the state machine goes to the check state.

The data segment loop consists of the null byte, two bytes which load the internal pointer start address, two bytes which load the internal pointer end address, and enough data bytes to equal the difference between the end points. The state machine loops, loading data and incrementing the address counter, until the internal address pointer equals the end address pointer. Then it checks the segment counter. If more segments are to be loaded, the machine returns to the null state; and the data segment loop is executed again. If the segment counter is zero, the state machine goes to the check state. If an invalid value is encountered for the internal start or end address, the $\overline{ERR}$ signal switches low; and the state machine moves directly to the done state.

In the check state, the next byte in the stream file is examined. When a single device is being configured, this byte is a postamble, and the state machine moves to the done state. When devices are cascaded together for multiple configurations, this byte is a preamble for the next configuration file. The state machine transfers the data to the downstream device and monitors the downstream bit stream data to determine the next check for a preamble byte. If the state machine encounters a byte that isn't a preamble or a postamble, the $\overline{ERR}$ signal switches low; and the state machine enters the done state.

The done state releases the $\overline{CON}$ pin and loops until $\overline{CON}$ goes high and the device enters the idle state. In modes 1, 2, 5 and 6, the device enters the idle state three CCLK edges after $\overline{CON}$ is high. In modes 3 and 4, it takes twenty-four CCLK edges for the device to reach idle. The CCLK signal must therefore continue after the postamble until the device reaches the idle state.

Partial Configuration

Figure 4 gives the bit stream file used to configure a hypothetical device that has a 6 x 6 array of cells lined with four I/O on each side. Configuration begins with the bottom left cell, number 0, and ends with the upper right cell, number 35. Then the I/O cells are configured, beginning at number 36 and proceeding clockwise to number 51.

By placing windows in the bit stream file, it is possible to configure only a portion of the array. Figure 5 gives the bit stream file used to configure the lower right portion of the array and I/Os 45, 46 and 47— the program leaves darkened cells untouched.

On line six the program states that there are four segments of data to configure. The start address is the left-most cell in the bottom row to be configured, number 9, and the end address is the right-most cell in the row, number 11. Four bytes of data are used to load the cell between the two points, number 10. The next segment configures the row above. Notice that the cells between the first segment end address and the second segment start address are omitted. The data in these cells is left untouched— only the cell being programmed on a given clock cycle is changed. The other cells function as if in their normal operational mode. This means a portion of the array can be configured while the rest of the array remains operational.

Configuration Compression

A configuration compression algorithm, included in the Integrated Development System, uses windowing to compress the configuration file. On power-up, all cells in the FPGA are programmed to be logical zeros. Unused cells in a design remain zeros, so they do not need to be configured. The compression algorithm skips unused cells and can reduce file size by up tp 80%. This in turn reduces configuration time and memory storage requirements. It even makes designs less susceptible to reverse engineering, due to the random start and end array addresses in the compressed bit stream. For more information about the configuration compression algorithm, refer to the FPGA application notes.

Bit-Stream Sizes (bytes of data)

Mode(s)	Type [1, 2]	Beginning Sequence	6002	6003	6005	6010
1	P	Preamble	2677	4153	8077	16393
2	P	Preamble	2677	4153	8077	16393
3	S	Null Byte/Preamble	2678	4154	8078	16394
4	S	Null Byte/Preamble	2678	4154	8078	16394
5	P	Preamble	2677	4153	8077	16393
6	P	Preamble/Preamble	2678	4154	8078	16394

Notes: 1. P = Parallel.
2. S = Serial.

Figure 4. Full Configuration Example

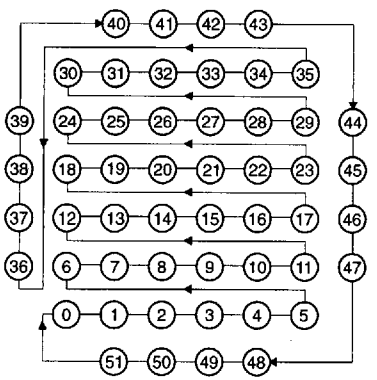
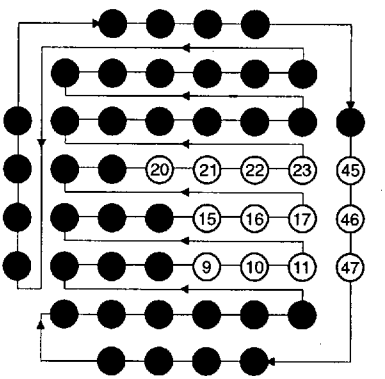


Figure 5. Partial Configuration Example



Full Configuration

```
10110010  ; preamble
00000000; control register
00000000; external address lsb
00000000;
00000000; external address msb
11111110; number of window segments
00000000; null
00000000; start address
00000000;
00000000; end address
00110011;
00000000; data
00000001
00000010
00000011
00000100
.
.
00110010
00110011
01001101; postamble
```

Partial Configuration

```
10110010  ; preamble
00000000; control register
00000000; external address lsb
00000000;
00000000; external address msb
11111011; number of window segments
00000000; null
00000000; start address segment 1
00001001;
00000000; end address
00010011;
00001001; data
00001010
00001011
00000000; null
00000000; start address segment 2
00001111;
00000000; end address
00010001;
00001111; data
00010001
00010001
.
.
00000000; null
00000000; start address segment 4
00101101;
00000000; end address
00101111;
00101101; data
00101110
00101111
01001101; postamble
```

Configuration Modes

This section gives setup requirements and usage guidelines for each configuration mode.

Mode 0: Configuration Reset

Configuration Data Source	Internal
Dedicated Configuration Pins Used	$\overline{CON}$, $\overline{CS}$, M0, M1, M2, CCLK
Dual-Function Pins Used	None
Optional Dual-Function Pins	None

Mode 0 initiates the reboot sequence— it is equivalent to turning power to the device off and on again. Mode 0 overrides any other configuration sequences and cannot be stopped. In AT6000 devices, mode 0 is enabled by asserting $\overline{CS}$, $\overline{CON}$, M0, M1 and M2 low during the rising edge of CCLK. Reboot starts when the mode pins are released from mode 0 to any other mode. Because of this, the device should not be powered up in mode 0. One clock after entering mode 0, $\overline{CSOUT}$ tristates. Users who cascade devices and intend to use the mode 0 reboot function should insert logic to guarantee that the $\overline{CS}$ signal sent to the downstream cascaded device is driven low.

Mode 1: Address Count-Up, External CCLK

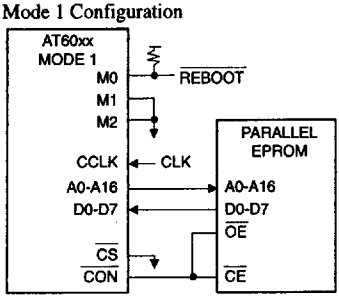
Configuration Data Source	Parallel EPROM
Dedicated Configuration Pins Used	$\overline{CON}$, $\overline{CS}$, M0, M1, M2, CCLK
Dual-Function Pins Used	D0-D7, A0-A16
Optional Dual-Function Pins	$\overline{ERR}$, $\overline{CHECK}$, $\overline{CSOUT}$, $\overline{CEN}$

Mode 1 (Figure 6) does not automatically generate a $\overline{CON}$ signal after the power-up boot sequence. The user supplies a configuration clock to CCLK. Configuration is initiated by driving $\overline{CON}$ low.

If the FPGA is sharing a large EPROM with a microprocessor, the addresses used must start from the opposite end of the EPROM address map so that configuration does not interfere with the microprocessor, and vice versa. In mode 1, the external address counter starts at 00000 and counts up (see mode 2 description).

Using a maximum clock rate of 10 MHz, mode 1 can configure a single device in under 1 millisecond. Cascading devices limits the parallel data rate to 800 kHz.

Figure 6. Mode 1 Configuration



Mode 2: Address Count-Down, External CCLK

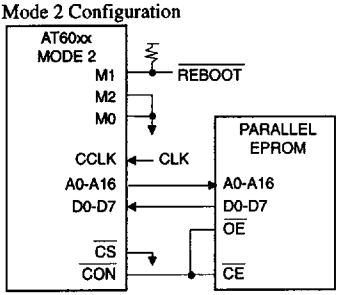
Configuration Data Source	Parallel EPROM
Dedicated Configuration Pins Used	$\overline{CON}$, $\overline{CS}$, M0, M1, M2, CCLK
Dual-Function Pins Used	D0-D7, A0-A16
Optional Dual-Function Pins	$\overline{ERR}$, $\overline{CHECK}$, $\overline{CSOUT}$, $\overline{CEN}$

Mode 2 (Figure 7) does not automatically generate a $\overline{CON}$ signal after the power-up boot sequence. The user supplies a configuration clock to CCLK. Configuration is initiated by driving $\overline{CON}$ low.

A typical microprocessor uses the highest or lowest address to load its own reboot address vector. If the FPGA is sharing a large EPROM with a microprocessor, the addresses used must start from the opposite end of the EPROM address map so that configuration does not interfere with the microprocessor, and vice versa. In mode 2, the external address counter starts at 1FFFF and counts down (see mode 1 description).

Using a maximum clock rate of 10 MHz, mode 2 can configure a single device in under one millisecond. Cascading devices limits the parallel data rate to 800 kHz.

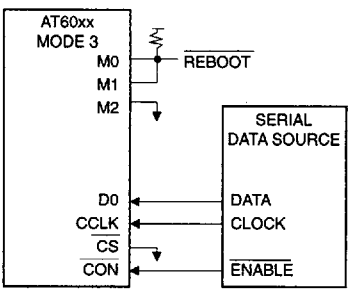
Figure 7. Mode 2 Configuration



Mode 3: Bit-Sequential, External CCLK

Configuration Data Source	Serial EPROM, Serial Comm. Port, UART, Download Cable
Dedicated Configuration Pins Used	$\overline{CON}$, $\overline{CS}$, M0, M1, M2, CCLK
Dual-Function Pins Used	D0
Optional Dual-Function Pins	$\overline{ERR}$, $\overline{CHECK}$, $\overline{CSOUT}$

Figure 8. Mode 3 Configuration



Mode 3 (Figure 8) does not automatically generate a $\overline{CON}$ signal after the power-up boot sequence. The user must supply a configuration clock to CCLK. Configuration is initiated by driving $\overline{CON}$ low.

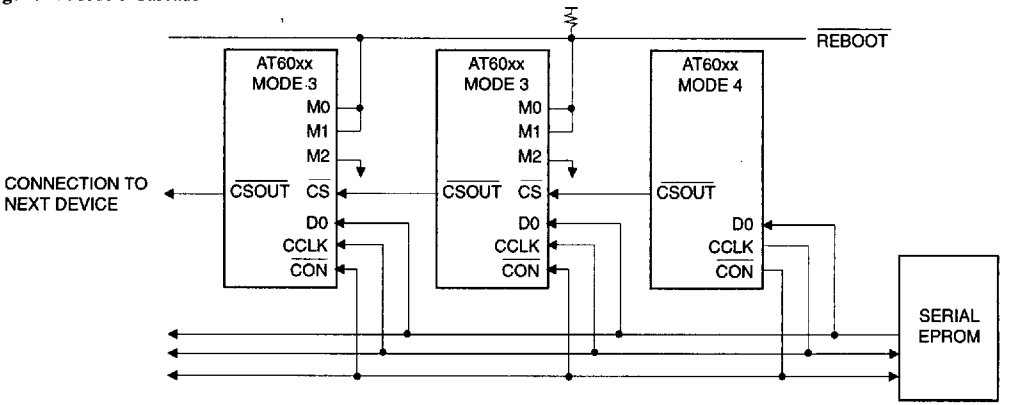
As long as data setup and hold requirements are satisfied, CCLK pulses can have arbitrary periods. This is helpful when using asynchronous communication ports or UARTs for configuration. If CCLK is stopped entirely between configurations, allow 24 preceding and trailing clock pulses with respect to $\overline{CON}$ going low or high (refer to the AC timing table in the AT6000 Series data sheet).

Depending on the speed of the user-supplied clock, mode 3 configuration can take as little as 8 milliseconds.

Mode 3 can be used to configure multiple devices cascaded together (Figure 9). The first device in the cascade chain must use either Mode 3 or Mode 4. If the configuration file contains a second preamble instead of a postamble (see the configuration-file format section), then the first device in the chain drives $\overline{CSOUT}$ low enabling the next device in the chain to receive configuration data from the serial data source. Configuration for downstream devices proceeds in a similar manner with "chip select" ($\overline{CS}$) propagating through the chain.

Mode 3 is used when configuring with the download cable provided in the Integrated Development System.

Figure 9. Mode 3 Cascade



Mode 4: Bit-Sequential, Internal CCLK E²PROM (AT17XXX)

Configuration Data Source	Serial E²PROM
Dedicated Configuration Pins Used	$\overline{CON}$, $\overline{CS}$, M0, M1, M2, CCLK
Dual-Function Pins Used	D0
Optional Dual-Function Pins	$\overline{ERR}$, $\overline{CHECK}$, $\overline{CSOUT}$

Mode 4 (Figure 10) asserts the $\overline{CON}$ pin low during the power-up boot sequence. $\overline{CON}$ is released for one CCLK period after initialization to reset the serial E²PROM. $\overline{CON}$ is then automatically re-asserted low and an internal oscillator toggles CCLK. This causes the E²PROM to begin downloading configuration data. One bit of data is loaded from the D0 pin on each rising edge of CCLK until configuration is complete. $\overline{CON}$ is then released, indicating the device is ready to use. Configuration time varies depending on the speed of the internal oscillator, but typically takes about 8 milliseconds.

The power supply ramp-up rate is critical in mode 4. The device generates a reset pulse 8 milliseconds after the supply voltage crosses the V_{TRIP} level (Figure 11). The supply voltage must be at the minimum for the serial E²PROM before the FPGA generates its reset pulse. Otherwise, the E²PROM's operation may be sporadic.

Mode 5: Address Count-Up, Internal CCLK

Configuration Data Source	Parallel EPROM
Dedicated Configuration Pins Used	$\overline{CON}$, $\overline{CS}$, M0, M1, M2, CCLK
Dual-Function Pins Used	D0-D7, A0-A16
Optional Dual-Function Pins	$\overline{ERR}$, $\overline{CHECK}$, $\overline{CSOUT}$, CEN

Mode 5 (Figure 12) does not automatically generate a $\overline{CON}$ signal after the power-up boot sequence. Configuration is initiated by driving $\overline{CON}$ low. An internal oscillator toggles CCLK. This causes the FPGA to generate addresses A0-A16, beginning at 0, to read a configuration file from a parallel EPROM. One byte of configuration data is loaded from the D0-D7 pins on each rising edge of CCLK until configuration is complete. $\overline{CON}$ is then released, indicating the device is ready to use. Configuration time varies depending on the speed of the oscillator, but typically takes 8 milliseconds for the AT6005, and 16 milliseconds for the AT6002/3/10.

Only 13 address bits are required to fully program a single device; the four extra addresses allow multiple device configuration and let the device share memory space with other components of a system.

Figure 10. Mode 4 Configuration

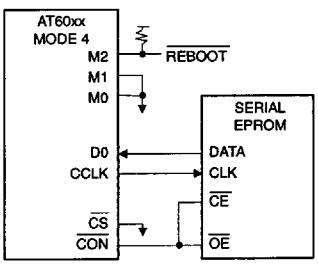


Figure 12. Mode 5 Configuration

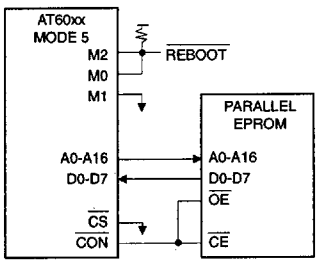
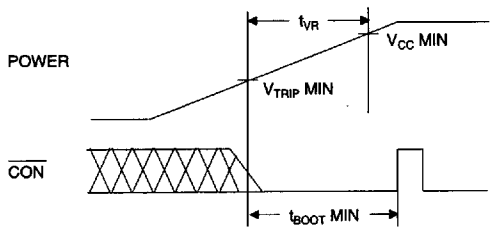


Figure 11. Power Supply Ramp-Up (Mode 4)



V_{CC} min	Minimum voltage for E²PROM operation
V_{TRIP} min	Minimum FPGA supply voltage to initiate reboot
t_{BOOT} min	Minimum reboot cycle time
t_{VR}	Minimum rise time of power supply from V_{TRIP} to V_{CC} min.

Mode 6: Byte-Sequential, External CCLK

Configuration Data Source	Parallel port of microprocessor
Dedicated Configuration Pins Used	$\overline{CON}$, $\overline{CS}$, M0, M1, M2, CCLK
Dual-Function Pins Used	D0-D7
Optional Dual-Function Pins	$\overline{ERR}$, $\overline{CHECK}$, $\overline{CSOUT}$

Figure 13. Mode 6 Configuration

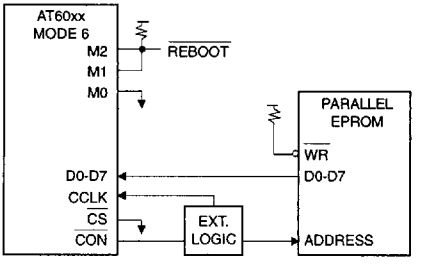


Figure 14. Mode 6 Cascade

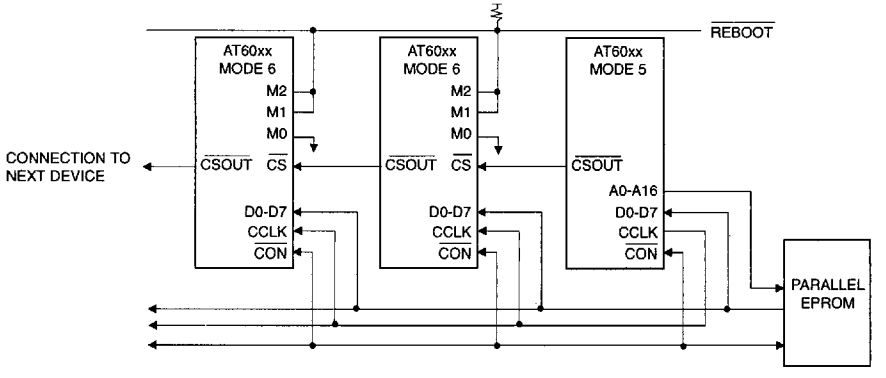
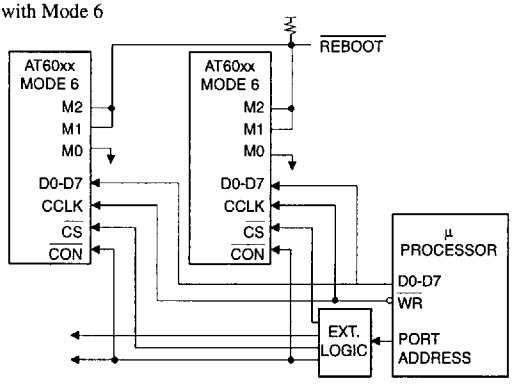


Figure 15. Parallel Configuration with Mode 6



Configuration Timing Parameters

These AC parameters are based on the timing diagrams that follow.

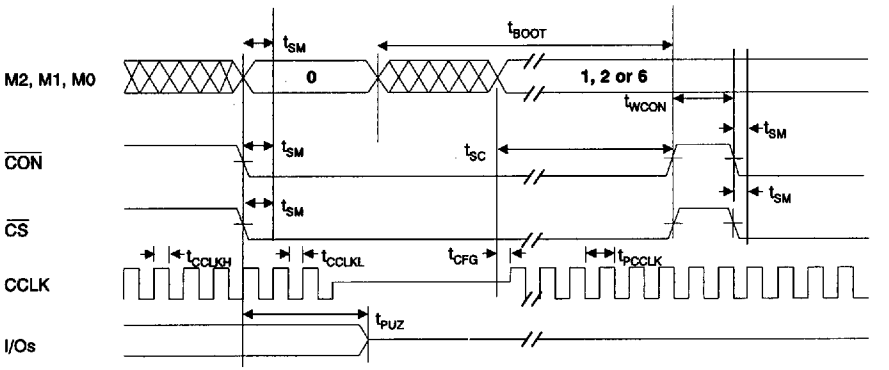
Parameter	Description		Min	Typ	Max	Units
t_{BOOT}	Delay from release of mode 0 or Power on (V_{CC} > Vsth min) to $\overline{CON}$ released.	AT6002/3: modes 1,2,3,5,6	1.3	2.7	5.4	ms
		AT6002/3/10: mode 4	8.1	16.3	32.6	ms
		AT6005: modes 1,2,3,4,5,6	4.4	8.8	17.6	ms
		AT6010: modes 1,2,3,5,6	0.05	0.1	0.2	ms
t_{WCON}	$\overline{CON}$ and $\overline{CS}$ high pulse width. Measured in CCLK clock cycles in modes 1, 2, 3 and 6.		2			cyc
t_{PCON}	$\overline{CON}$ high pulse width. Measured in CCLK clock cycles in modes 4 and 5.		2		2	cyc
t_{PUZ}	Delay from power-up or entry into mode 0 to user I/Os being tri-stated.			2000	4000	ns
t_{DERR}	Delay time from CCLK to change in $\overline{ERR}$. $\overline{ERR}$ will typically be high, and only go low if there is an error during confiugration or a mismatch during the check function.				30	ns
t_{SM}	Setup time from M0, M1, M2, $\overline{CS}$ and $\overline{CON}$ to rising edge of CCLK to initiate configuration or reboot.		30			ns
t_{HMP}	Hold time for $\overline{CS}$ and $\overline{CON}$ from rising edge of CCLK with preamble data present. Valid in modes 1, 2, 5 and 6.		2			cyc
t_{HMS}	Hold time for $\overline{CS}$ and $\overline{CON}$ from rising edge of CCLK with the least-significant-bit of the preamble present. Valid in modes 3 and 4.		17			cyc
t_{HCD}	Hold time for configuration data with respect to rising edge of CCLK.		5			ns
t_{SCD}	Setup time for configuration data with respect to rising edge of CCLK.		10			ns
t_{CFG}	Delay from rising edge of CCLK to change in I/O pin direction, as required when moving between the configuration and operation states.				50	ns
t_{DA}	Delay from CCLK rising edge to external address change.				35	ns
t_{CONH}	Delay from rising edge of CCLK to $\overline{CON}$ release. Delay measured with 2.7k pull-up resistor on $\overline{CON}$.				35	ns
t_{SC}	Setup time for M0, M1, M2 and CCLK to $\overline{CON}$ high.		10			cyc
V_{TRIP}	Supply voltage at which FPGA initiates reboot.		2.8		4.75	V
t_{CS}	Delay time from falling edge of CCLK to change in $\overline{CSOUT}$.				30	ns

Table 3. CCLK Parameters

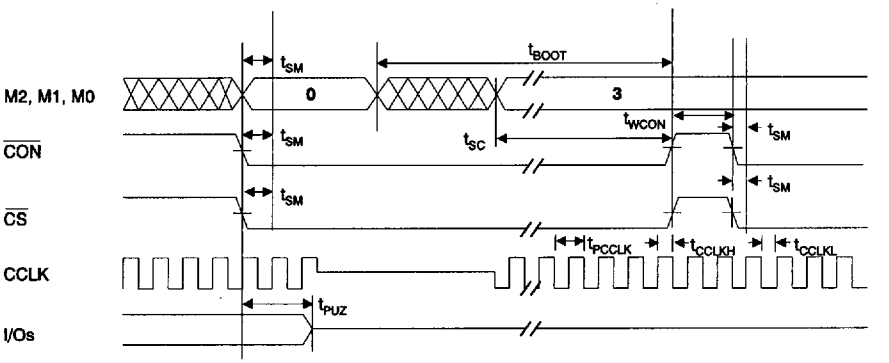
Mode(s)	Condition	t_{CCLKL} Min	t_{CCLKH} Min	t_{PCCLK} Min	t_{PCCLK} Typ	t_{PCCLK} Max
1, 2, 6	Without Cascade, without $\overline{\text{CHECK}}$	40 ns	40 ns	80 ns		
1, 2, 6	With Cascade, without $\overline{\text{CHECK}}$	150 ns	150 ns	1.25 µs		
1, 2, 6	Without Cascade, with $\overline{\text{CHECK}}$	200 ns	200 ns	500 ns		
1, 2, 6	With Cascade, with $\overline{\text{CHECK}}$	200 ns	200 ns	1.25 µs		
4, 5	CCLK is Output	240 ns	240 ns	500 ns	800 ns	1200 ns
3	Without $\overline{\text{CHECK}}$	40 ns	40 ns	80 ns		
3	With $\overline{\text{CHECK}}$	200 ns	200 ns	500 ns		

Reboot Cycle

Modes 1, 2 and 6

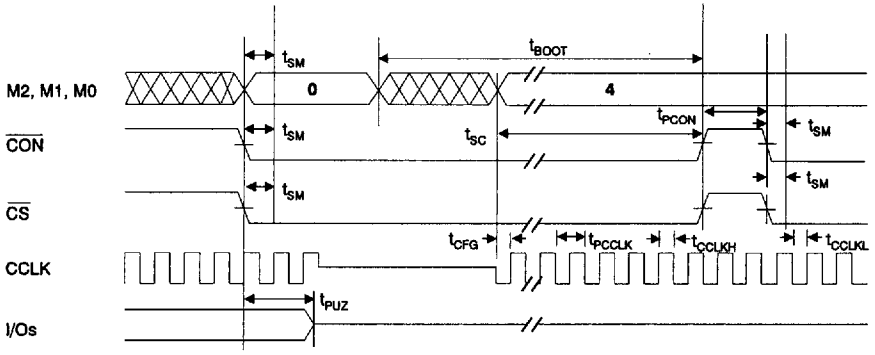


Mode 3

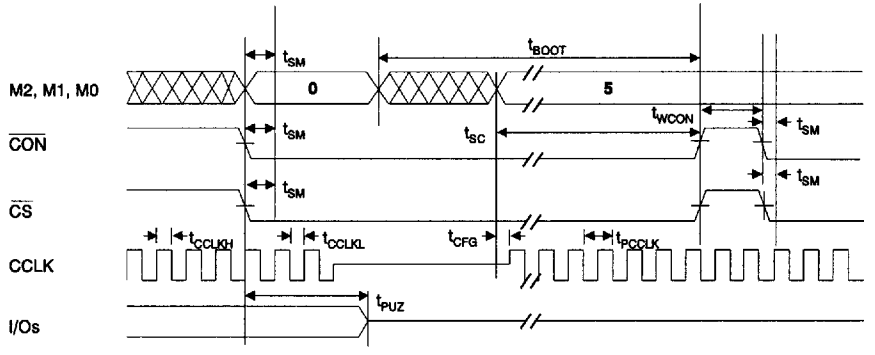


Reboot Cycle (Continued)

Mode 4

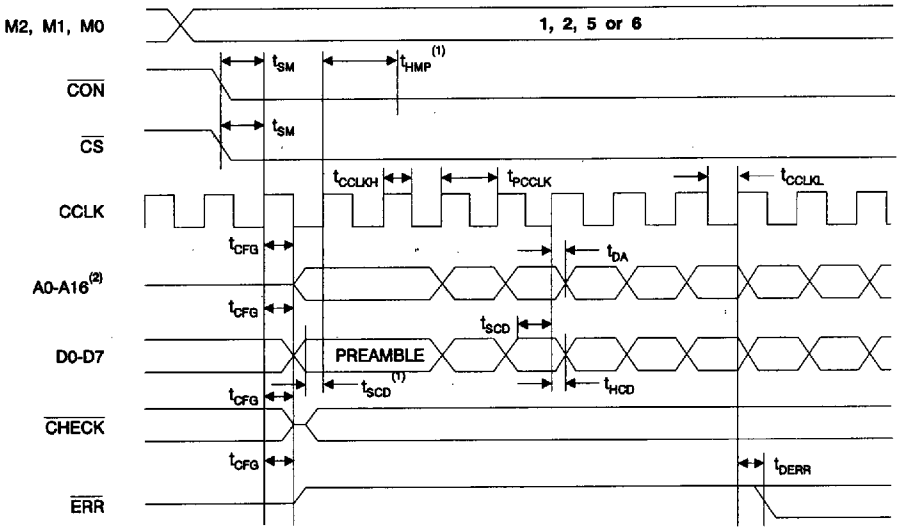


Mode 5



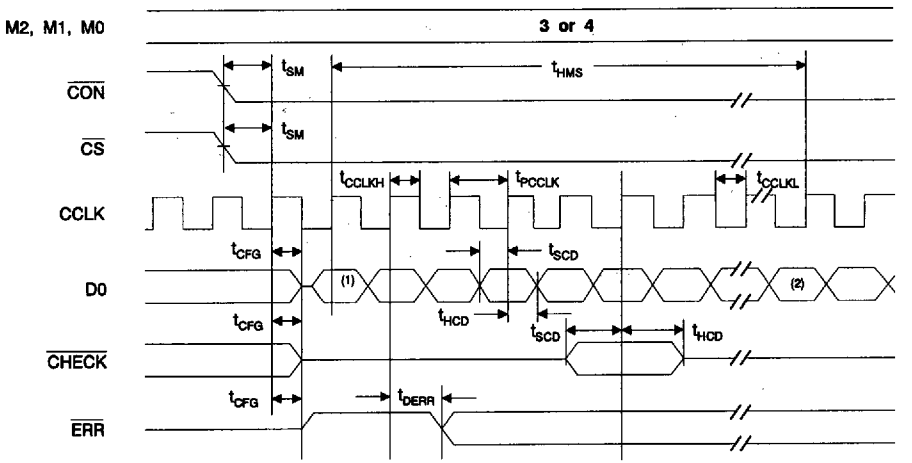
Beginning of Configuration

Modes 1, 2, 5 and 6



Notes: 1. Measured with respect to the edge of CCLK, which clocks in the preamble.
2. A0-A16 not used in mode 6.

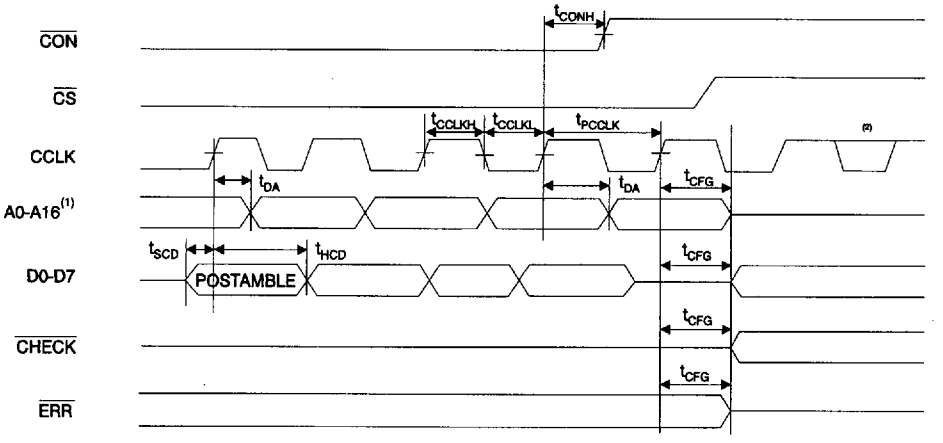
Modes 3 and 4



Note: 1. Preamble LSB.
2. Preamble MSB.

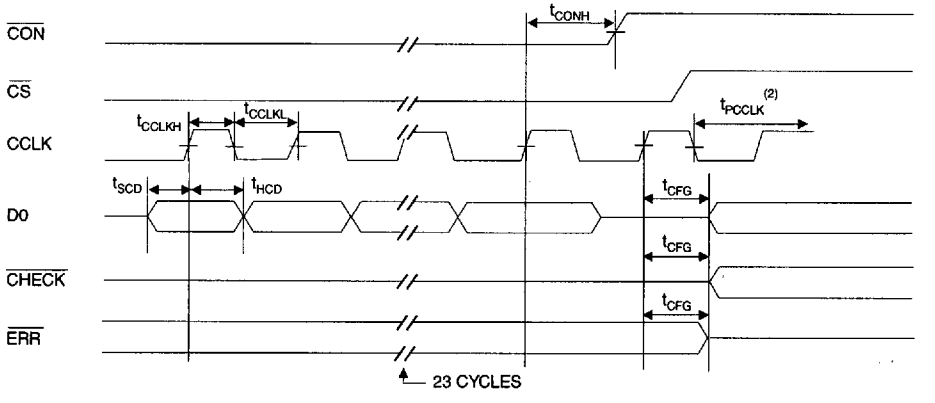
End of Configuration without Cascading

Modes 1, 2, 5 and 6



Note: 1. A0-A16 not used in mode 6.
2. CCLK remains high in mode 5.

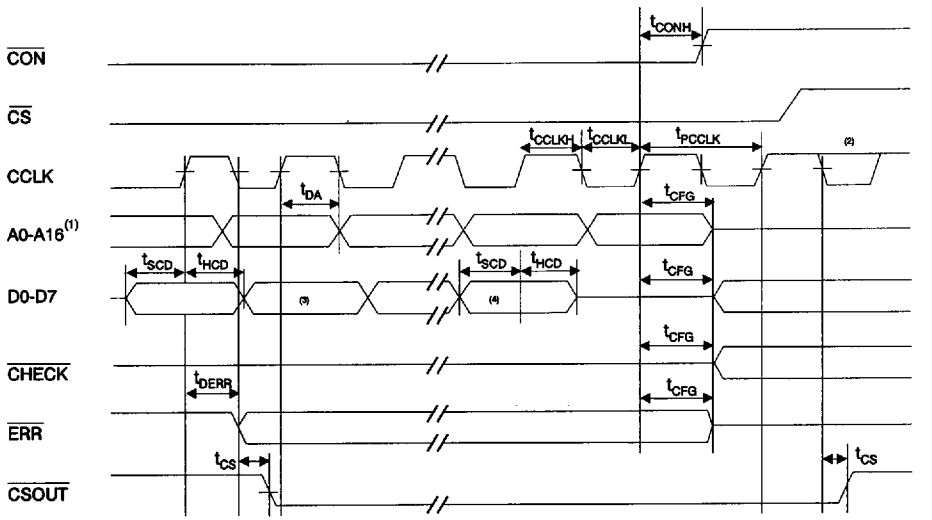
Modes 3 and 4



Note: 1. Postamble LSB.
2. CCLK remains high in mode 4.

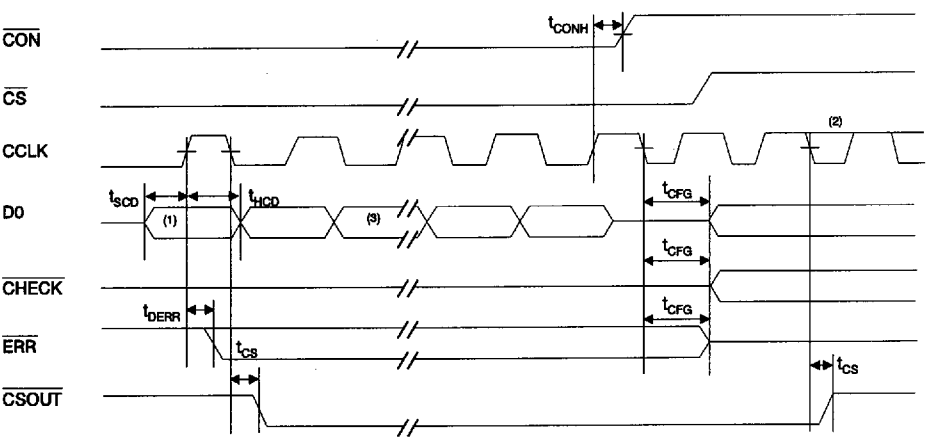
End of Configuration with Cascading

Modes 1, 2, 5 and 6



Note: 1. A0-A16 not used in mode 6.
2. CCLK remains high in mode 5.
3. End address of final window.
4. Postamble of final chip in cascade chain.

Modes 3 and 4



Note: 1. Preamble LSB.
2. CCLK remains high in mode 4.
3. Postamble of final chip in cascade chain.