REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add "Y" package and updated boilerplate.	96-04-12	M. A. Frye
B	Updated boilerplate. Changes to $t_{pd(O-PB)}$ and $t_{pd(E-PE)}$. - glg	97-12-04	Raymond Monnin

REV	B	B	B	B	B	B	B													
SHEET	35	36	37	38	39	40	41													
REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34

REV STATUS OF SHEETS																		
	REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14			

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
Gary L. Gross

CHECKED BY
Jeff Bowling

APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
95-11-03

REVISION LEVEL
B

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216

MICROCIRCUIT, MEMORY, DIGITAL, CMOS
64 X 36 X 2 CLOCKED FIFO, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-95609**

SHEET 1 OF 41

DSCC FORM 2233
APR 97

5962-E059-98

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

9004708 0033095 771

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V) , and nontraditional performance environment (device class N). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN. For device class N, the user is cautioned to assure that the device is appropriate for the application environment.

1.2 PIN. The PIN shall be as shown in the following example:

5962	-	95609	01	Q	X	X
* * *	* * *		* * *	* * *	* * *	* * *
Federal stock class designator	RHA designator (see 1.2.1)		Device type (see 1.2.2)	Device class designator (see 1.2.3)	Case outline (see 1.2.4)	Lead finish (see 1.2.5)
\		/				
	V					
	Drawing number					

1.2.1 RHA designator. Device classes N, Q, and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	ABT3614	64 X 36 X 2 clocked FIFO

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
N	Certification and qualification to MIL-PRF-38535 with a non-traditional performance environment 1/
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	120	Plastic quad flat package
Y	See figure 1	132	Ceramic quad flat package

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes N, Q, and V or MIL-PRF-38535, appendix A for device class M.

1.2.5.1 Lead finish D. Lead finish D shall be designated by a single letter as follows:

Finish letter	Process
D	Palladium

1/ Any device outside the traditional performance environment; i.e., (Plastic Encapsulated Microcircuit).

1.3 Absolute maximum ratings. 2/ 3/ 4/

Supply voltage range (V_{CC})	-0.5 V dc to +7.0 V dc
DC input voltage range (I/O ports) (V_{IN})	-0.5 V dc to V_{CC} + 0.5 V dc 5/
DC output voltage range (V_{OUT})	-0.5 V dc to V_{CC} + 0.5 V dc 5/
DC output current (I_O) (per output)(V_O = 0.0 V to V_{CC})	±50 mA
DC input clamp current (I_{IK}) (V_{IN} < 0.0 V or V_{IN} > V_{CC})	±20 mA
DC output clamp current (I_{OK}) (V_{OUT} < 0.0 V or V_{OUT} > V_{CC})	±50 mA
Storage temperature range (T_{STG})	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (Θ_{JC})	3.3°C/W
Junction temperature (T_J)	+175°C
Maximum power dissipation (P_D) at T_A = +55°C in still air	1.8 W 6/
V_{CC} current (I_{VCC})	±400 mA
Ground current (I_{GND})	±400 mA

1.4 Recommended operating conditions. 3/ 4/

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Maximum low level input voltage (V_{IL})	+0.8 V
Minimum high level input voltage (V_{IH})	+2.0 V
Maximum high level output current (I_{OH})	-4.0 mA
Maximum low level output current (I_{OL})	+8.0 mA
Case operating temperature range (T_C)	-55°C to +125°C

1.5 Digital logic testing for device classes N, Q, and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	XX percent 7/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).

2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
3/ Unless otherwise noted, all voltages are referenced to GND.
4/ The limits for the parameters specified herein shall apply over the full specified V_{CC} range and case temperature range of -55°C to +125°C.
5/ The input negative voltage rating may be exceeded provided that the input clamp current rating is observed.
6/ The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
7/ Values will be added when they become available.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes N, Q, and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes N, Q, and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 3.

3.2.4 Block or logic diagram(s). The block or logic diagram(s) shall be as specified on figure 4.

3.2.5 Test circuit and switching waveforms. The test circuit and switching waveforms shall be as specified on figure 5.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes N, Q, and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes N, Q, and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes N, Q, and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes N, Q, and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Test conditions 1/ $-55°C \le T_C \le +125°C$, $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified		Device types	Group A subgroups 2/	Limits 3/ Min	Limits 3/ Max	Unit
High level output voltage	V_{OH}	For all inputs affecting output under test, V_{IN} = 2.0 V or 0.8 V, I_{OH} = -4.0 mA, V_{CC} = 4.5 V		01	1, 2, 3	2.4		V
Low level output voltage	V_{OL}	For all inputs affecting output under test, V_{IN} = 2.0 V or 0.8 V, I_{OL} = 8 mA, V_{CC} = 4.5 V		01	1, 2, 3		0.5	V
Input current	I_I 4/	For input under test, $V_I = V_{CC}$ or GND, V_{CC} = 5.5 V		01	1, 2, 3		±50	µA
Three-state output leakage current high	I_{OZH} 5/	$V_{OUT} = V_{CC}$, V_{CC} = 5.5 V		01	1, 2, 3		50	µA
Three-state output leakage current low	I_{OZL} 5/	V_{OUT} = GND, V_{CC} = 5.5 V		01	1, 2, 3		-50	µA
Quiescent supply current, outputs high	I_{CC}	For all inputs, Output = port B, I_{OUT} = 0 A, V_{CC} = 5.5 V, $V_{IN} = V_{CC}$ -0.2 V or GND	Outputs high	01	1, 2, 3		30	mA
			Outputs low				130	
			Outputs disabled				30	
Input capacitance	C_{IN}	T_C = +25°C, V_{BIAS} = 0 V, V_{CC} = 5.0 V, See 4.4.1e	Control inputs	01	4		6	pF
I/O capacitance	$C_{I/O}$		A or B ports		4		9	
Functional tests	6/	V_{IH} = 2.0 V, V_{IL} = 0.8 V, verify output V_O, V_{CC} = 4.5 V and 5.5 V, 4.4.1c		01	7, 8A, 8B	L	H	
Clock frequency CLKA or CLKB	f_{clock}	C_L = 20 pF minimum, V_{CC} = 4.5 V and 5.5 V, see figures 5 and 6 as applicable		01	9, 10, 11		50	MHz
Clock cycle time CLKA or CLKB	t_c			01	9, 10, 11	20		ns
Pulse duration, CLKA and CLKB high or low	t_w			01	9, 10, 11	8		
Setup time, A0-A35 before CLKA↑, and B0-B35 before CLKB↑	$t_{su(D)}$			01	9, 10, 11	5		
Setup time, CSA, ENA and MBA before CLKA↑; CSB, and ENB before CLKB↑	$t_{su(EN)}$			01	9, 10, 11	5		
Setup time, W/RA to CLKA↑, and W/RB to CLKB↑	$t_{su(W)}$			01	9, 10, 11	10		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	Device types	Group A subgroups 2/	Limits 3/		Unit
					Min	Max	
Setup time, SIZ0, SIZ1, and BE before CLKB↑	$t_{su(SZ)}$	C_L = 20 pF minimum, V_{CC} = 4.5 V and 5.5 V, See figures 5 and 6 as applicable	01	9, 10, 11	5		ns
Setup time, $\overline{RST}$ low before CLKA↑ or CLKB↑	$t_{su(RS)}$ 7/		01	9, 10, 11	6		
Setup time, FS0 and FS1 before $\overline{RST}$ high	$t_{su(FS)}$		01	9, 10, 11	6		
Setup time, SW0 and SW1 before CLKB↑	$t_{su(SW)}$		01	9, 10, 11	7		
Setup time, ODD/EVEN and PGA before CLKA↑; ODD/EVEN and PGB before CLKB↑	$t_{su(PG)}$ 8/		01	9, 10, 11	6		
Hold time, A0-A35 after CLKA↑ and B0-B35 after CLKB↑	$t_{h(D)}$		01	9, 10, 11	1		
Hold time, $\overline{CSA}$, W/$\overline{RA}$, ENA and MBA after CLKA↑ and $\overline{CSB}$, W/$\overline{RB}$, and ENB after CLKB↑	$t_{h(EN)}$		01	9, 10, 11	1		
Hold time, SIZ0, SIZ1, and BE after CLKB↑	$t_{h(SZ)}$		01	9, 10, 11	2		
Hold time, SW0 and SW1 after CLKB↑	$t_{h(SW)}$		01	9, 10, 11	7		
Hold time, ODD/EVEN and PGA after CLKA↑; ODD/EVEN and PGB after CLKB↑	$t_{h(PG)}$ 8/		01	9, 10, 11	0		
Hold time, $\overline{RST}$ low after CLKA↑ or CLKB↑	$t_{h(RS)}$ 7/		01	9, 10, 11	6		
Hold time, FS0 and FS1 after $\overline{RST}$ high	$t_{h(FS)}$		01	9, 10, 11	4		
Skew time, between CLKA↑ and CLKB↑ for EFA, EFB, FFA, AND FFB	$t_{sk(1)}$ 9/		01	9, 10, 11	8		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	Device types	Group A subgroups 2/	Limits 3/		Unit
					Min	Max	
Skew time, between CLKA↑ and CLKB↑ for AEA, AEB, AFA, and AFB	$t_{sk(2)}$ 9/	C_L = 20 pF minimum, V_{CC} = 4.5 V and 5.5 V, See figures 5 and 6 as applicable	01	9, 10, 11	16		ns
Access time, CLKA↑ to A0-A35 and CLKB↑ to B0-B35	t_a		01	9, 10, 11	2	12	
Propagation delay time, CLKA↑ to FFA and CLKB↑ to FFB	$t_{pd(C-FF)}$		01	9, 10, 11	2	12	
Propagation delay time, CLKA↑ to EFA and CLKB↑ to EFB	$t_{pd(C-EF)}$		01	9, 10, 11	2	12	
Propagation delay time, CLKA↑ to AEA and CLKB↑ to AEB	$t_{pd(C-AE)}$		01	9, 10, 11	2	12	
Propagation delay time, CLKA↑ to AFA and CLKB↑ to AFB	$t_{pd(C-AF)}$		01	9, 10, 11	2	12	
Propagation delay time, CLKA↑ to $\overline{MBF1}$ low or $\overline{MBF2}$ high and CLKB↑ to $\overline{MBF2}$ low or $\overline{MBF1}$ high	$t_{pd(C-MF)}$		01	9, 10, 11	1	12	
Propagation delay time, CLKA↑ to B0-B35↑ 10/ and CLKB↑ to A0-A35 11/	$t_{pd(C-MR)}$		01	9, 10, 11	3	13	
Propagation delay time, MBA to AO-A35 valid and SIZ0, SIZ1 to B0-B35 valid	$t_{pd(M-DV)}$		01	9, 10, 11	1	11.5	
Propagation delay time, CLKB↑ to PEFB 12/	$t_{pd(C-PE)}$		01	9, 10, 11	2	12	
Propagation delay time, A0-A35 valid to PEFA valid; B0-B35 valid to PEFB valid	$t_{pd(D-PE)}$		01	9, 10, 11	3	12.5	
Propagation delay time, ODD/EVEN to PEFA and PEFB	$t_{pd(O-PE)}$		01	9, 10, 11	3	12	
Propagation delay time, ODD/EVEN to parity bits (A8,A17,A26,A35) and (B8,B17,B26,B35)	$t_{pd(O-PB)}$		01	9, 10, 11	2	14	

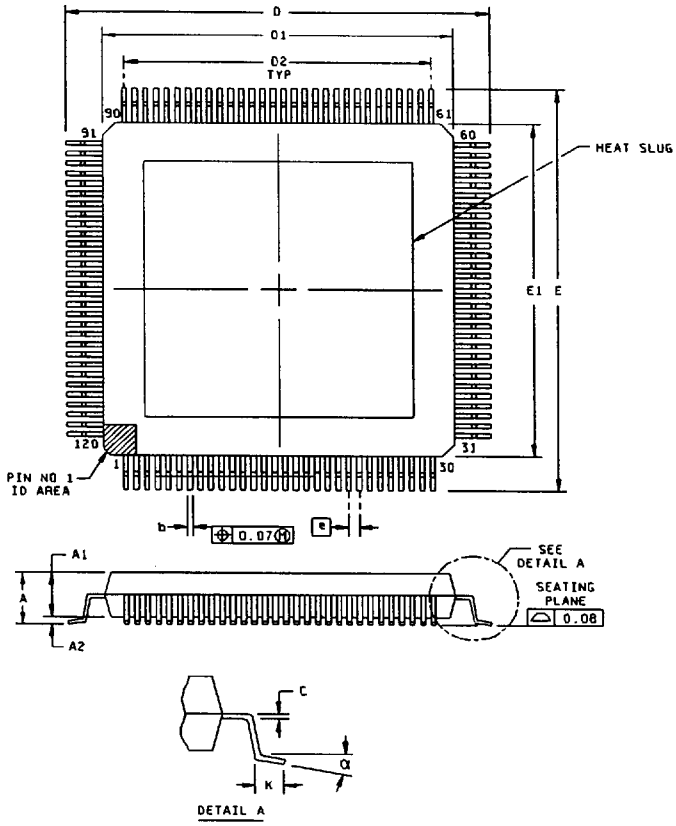
See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	Device types	Group A subgroups 2/	Limits 3/		Unit
					Min	Max	
Propagation delay time, $\overline{CSA}$, W/$\overline{RA}$, ENA, MBA or PGA to PEFA $\overline{CSB}$, W/$\overline{RB}$, ENB, SIZ1, SIZ0, or PGB to PEFB	$t_{pd(E-PE)}$	C_L = 20 pF minimum, V_{CC} = 4.5 V and 5.5 V, See figures 5 and 6 as applicable	01	9, 10, 11	1	23	ns
Propagation delay time, $\overline{CSA}$, W/$\overline{RA}$, ENA, MBA or PGA to parity bits (A8,A17, A26,A35); $\overline{CSB}$, W/$\overline{RB}$, ENB, SIZ1, SIZ0, or PGB to parity bits (B8,B17,B26,B35)	$t_{pd(E-PB)}$ 13/		01	9, 10, 11	3	19	
Propagation delay time, RST to ($\overline{MBF1}$, $\overline{MBF2}$) high	$t_{pd(R-F)}$		01	9, 10, 11	1	20	
Enable time, $\overline{CSA}$ and W/$\overline{RA}$ low to A0-A35 active and CSB low and W/$\overline{RB}$ high to B0-B35 active	t_{en}		01	9, 10, 11	2	12	
Disable time, $\overline{CSA}$ or W/$\overline{RA}$ high to A0-A35 at high impedance and CSB high or W/$\overline{RB}$ low to B0-B35 at high impedance	t_{dis}		01	9, 10, 11	1	9	

1/ Each input/output, as applicable, shall be tested at the specified temperature, for the specified limits, to the tests in table I herein. Output terminals not designated shall be high level logic, low level logic, or open, except for all I_{CC} tests, where the output terminals shall be open. When performing these tests, the current meter shall be placed in the circuit such that all current flows through the meter. For input terminals not designated, V_{IN} = GND or $V_{IN} \ge 3.0$ V.
2/ For device class N, all limits for subgroups 1, 3, 7, 8B, 9 and 11 are guaranteed but not production tested. These limits are characterized at qualification. Production testing is performed at max. operating temperature.
3/ For negative and positive voltage and current values, the sign designates the potential difference in reference to GND and the direction of current flow, respectively, and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein.
4/ For I/O ports, the limit includes I_I leakage current from the input circuitry.
5/ For I/O ports, the limit includes I_{OZH} or I_{OZL} leakage current from the output circuitry. This test is guaranteed when the control inputs affecting the output under test are at 2.0 V or 0.8 V.
6/ Tests shall be performed in sequence, attributes data only. Functional tests shall include the truth table and other logic patterns used for fault detection. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 3 herein. Functional tests shall be performed in sequence as approved by the qualifying activity on qualified devices. After incorporating allowable tolerances per MIL-STD-883, V_{IL} = 0.4 V and V_{IH} = 2.4 V. For outputs, L ≤ 0.8 V, H ≥ 2.0 V.
7/ Requirements to count the clock edge as one of at least four needed to reset the FIFO.
8/ Only applies for a clock edge that does a FIFO read.
9/ Skew time is not a timing constraint for proper device operation and is only included to illustrate the timing relationship between CLKA cycle and CLKB cycle. This parameter is guaranteed, but not tested.
10/ Writing data to the mail1 register when the B0-B35 outputs are active and SIZ1, SIZ0 are high.
11/ Writing data to the mail2 register when the A0-A35 outputs are active and MBA is high.
12/ Only applies when a new port-B bus size is implemented by the rising CLKB edge.
13/ Only applies when reading data from a mail register.

Case outline X (see notes 1, 2, 3 and 4)

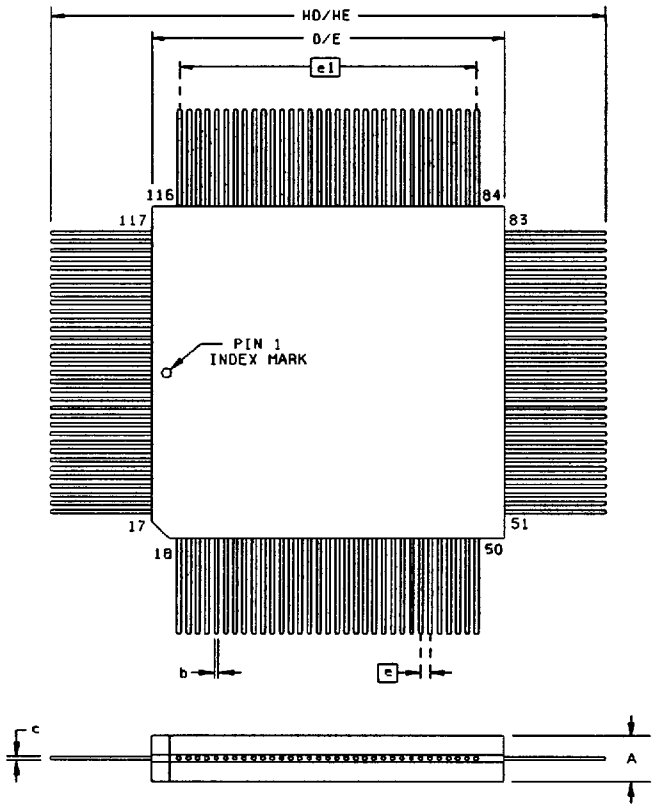


*Symbol	*Millimeters		*	*Symbol	*Millimeters		*
*	* Min	* Max	*	*	* Min	* Max	*
* A	* —	* 1.60	*	*D1/E1	*13.80	*14.20	*
* A1	* 1.35	* 1.45	*	* D2	* 11.60 Nom.		*
* A2	* 0.05	* —	*	*e	* 0.40 BSC		*
* b	* 0.13	* 0.25	*	*K	* 0.45	* 0.75	*
* c	* 0.13 Nom.		*	*α	* 0°	* 7°	*
* D/E	*15.80	*16.20	*	*	*	*	*

Notes:
1. All linear dimensions are in millimeters.
2. Body dimensions do not include mold flash or protrusion. Allowable protrusion is 0.25 mm maximum per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07mm for 0.4mm pitch packages.
4. Thermally enhanced molded plastic package with a heat slug (HSL).

FIGURE 1. Case outline.

Case outline Y (see notes 1, 2, and 3)



Symbol	Inches		Millimeters		Symbol	Inches		Millimeters	
	Min	Max	Min	Max		Min	Max	Min	Max
A	0.110	0.150	2.79	3.81	HD/HE	1.460	1.540	37.08	39.12
b	0.008	0.014	0.20	0.36	e	0.025		0.635	
c	0.004	0.008	0.10	0.20	e1	0.800		20.32	
D/E	0.935	0.965	23.75	24.51	N	132			

Notes:
1. Although dimensions are in inches, the US government preferred system of measurement is the metric SI system. However, since this item was originally designed using inch-pound units of measurement, in the event of conflict between the two, the inch-pound units shall take precedence. Metric equivalents are for general information only.
2. Terminal one shall be identified by a mechanical index in the lead or body, or a mark on the top surface.
3. Terminal identification numbers need not appear on the package.

FIGURE 1. Case outline - Continued.

Device type	01						
Case outline	X						
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	A23	31	$\overline{AFA}$	61	AFB	91	B23
2	A22	32	FFA	62	AEB	92	B24
3	A21	33	CSA	63	EFB	93	B25
4	GND	34	ENA	64	B0	94	B26
5	A20	35	CLKA	65	B1	95	V_{CC}
6	A19	36	W/RA	66	B2	96	B27
7	A18	37	V_{CC}	67	GND	97	B28
8	A17	38	PGA	68	B3	98	B29
9	A16	39	PEFA	69	B4	99	GND
10	A15	40	MBF2	70	B5	100	B30
11	A14	41	MBA	71	B6	101	B31
12	A13	42	FS1	72	V_{CC}	102	B32
13	A12	43	FS0	73	B7	103	B33
14	A11	44	ODD/EVEN	74	B8	104	B34
15	A10	45	RST	75	B9	105	B35
16	GND	46	GND	76	GND	106	GND
17	A9	47	BE	77	B10	107	A35
18	A8	48	SW1	78	B11	108	A34
19	A7	49	SW0	79	B12	109	A33
20	V_{CC}	50	SIZ1	80	B13	110	A32
21	A6	51	SIZ0	81	B14	111	A31
22	A5	52	MBF1	82	B15	112	A30
23	A4	53	PEFB	83	B16	113	GND
24	A3	54	PGB	84	B17	114	A29
25	GND	55	V_{CC}	85	B18	115	A28
26	A2			86	B19	116	A27
27	A1	56	W/RB	87	B20	117	V_{CC}
28	A0	57	CLKB	88	GND	118	A26
29	$\overline{EFA}$	58	ENB	89	B21	119	A25
30	$\overline{AEA}$	59	CSB	90	B22	120	A24
		60	FFB				

FIGURE 2. Terminal connections.

Device type	01						
Case outline	Y						
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	GND	34	A10	67	GND	100	B10
2	RST	35	A11	68	B35	101	GND
3	ODD/EVEN	36	V_{CC}	69	B34	102	B9
4	FS0	37	A12	70	B33	103	B8
5	FS1	38	A13	71	GND	104	B7
6	MBA	39	A14	72	B32	105	V_{CC}
7	MBF2	40	GND	73	B31	106	B6
8	GND	41	A15	74	B30	107	B5
9	PEFA	42	A16	75	V_{CC}	108	B4
10	PGA	43	A17	76	B29	109	B3
11	V_{CC}	44	A18	77	B28	110	GND
		45	A19	78	B27	111	B2
12	W/RA	46	A20	79	GND	112	B1
13	CLKA	47	GND	80	B26	113	B0
14	ENA	48	A21	81	B25	114	EFB
15	CSA	49	A22	82	B24	115	AEB
16	FFA	50	A23	83	V_{CC}	116	GND
17	$\overline{AFA}$	51	V_{CC}	84	B23	117	AFB
18	GND	52	A24	85	B22	118	FFB
19	$\overline{AEA}$	53	A25	86	B21	119	CSB
20	$\overline{EFA}$	54	A26	87	GND	120	ENB
21	A0	55	GND	88	B20	121	CLKB
22	A1	56	A27	89	B19	122	W/RB
23	A2	57	A28	90	B18	123	V_{CC}
24	GND	58	A29	91	B17	124	PGB
25	A3	59	V_{CC}	92	B16	125	PEFB
26	A4	60	A30	93	B15	126	GND
27	A5	61	A31	94	GND	127	MBF1
28	A6	62	A32	95	B14	128	SIZ0
29	V_{CC}	63	GND	96	B13	129	SIZ1
30	A7	64	A33	97	B12	130	SW0
31	A8	65	A34	98	V_{CC}	131	SW1
32	A9	66	A35	99	B11	132	BE
33	GND						

FIGURE 2. Terminal connections - Continued.

Flag Programming

FS1	FS0	$\overline{RST}$	ALMOST-FULL AND ALMOST-EMPTY FLAG OFFSET REGISTER (X)
H	H	↑	16
H	L	↑	12
L	H	↑	8
L	L	↑	4

Port-A Enable Function

$\overline{CSA}$	W/$\overline{RA}$	ENA	MBA	CLKA	A0-A35 OUTPUTS	PORT FUNCTION
H	X	X	X	X	In high-impedance state	None
L	H	L	X	X	In high-impedance state	None
L	H	H	L	↑	In high-impedance state	FIFO1 write
L	H	H	H	↑	In high-impedance state	Mail1 write
L	L	L	L	X	Active, FIFO2 output register	None
L	L	H	L	↑	Active, FIFO2 output register	FIFO2 read
L	L	L	H	X	Active, mail2 register	None
L	L	H	H	↑	Active, mail2 register	Mail2 read (set $\overline{MBF2}$ high)

Port-B Enable Function

$\overline{CSB}$	W/$\overline{RB}$	ENB	SIZ1, SIZ0	CLK B	B0-B35 OUTPUTS	PORT FUNCTION
H	X	X	X	X	In high-impedance state	None
L	H	L	X	X	In high-impedance state	None
L	H	H	One, both low	↑	In high-impedance state	FIFO2 write
L	H	H	Both high	↑	In high-impedance state	Mail2 write
L	L	L	One, both low	X	Active, FIFO1 output register	None
L	L	H	One, both low	↑	Active, FIFO1 output register	FIFO1 read
L	L	L	Both high	X	Active, mail1 register	None
L	L	H	Both high	↑	Active, mail1 register	Mail1 read (set $\overline{MBF1}$ high)

FIFO1 and FIFO2 flag operation

NUMBER OF 36-BIT WORDS IN FIFO1 AND FIFO2 1/	FIFO1				FIFO2			
	SYNCHRONIZED TO CLKB		SYNCHRONIZED TO CLKA		SYNCHRONIZED TO CLKA		SYNCHRONIZED TO CLKAB	
	$\overline{EF}$B	$\overline{AE}$B	$\overline{AF}$A	$\overline{EF}$A	$\overline{EF}$A	$\overline{AE}$A	$\overline{AF}$B	$\overline{EF}$B
0	L	L	H	H	L	L	H	H
1 to X	H	L	H	H	H	L	H	H
(X+1) to [64-(X+1)]	H	H	H	H	H	H	H	H
(64-X) to 63	H	H	L	H	H	H	L	H
64	H	H	L	L	H	H	L	L

1/ X is the value in the almost-empty flag and the almost-full flag offset register.

FIGURE 3. Truth tables.

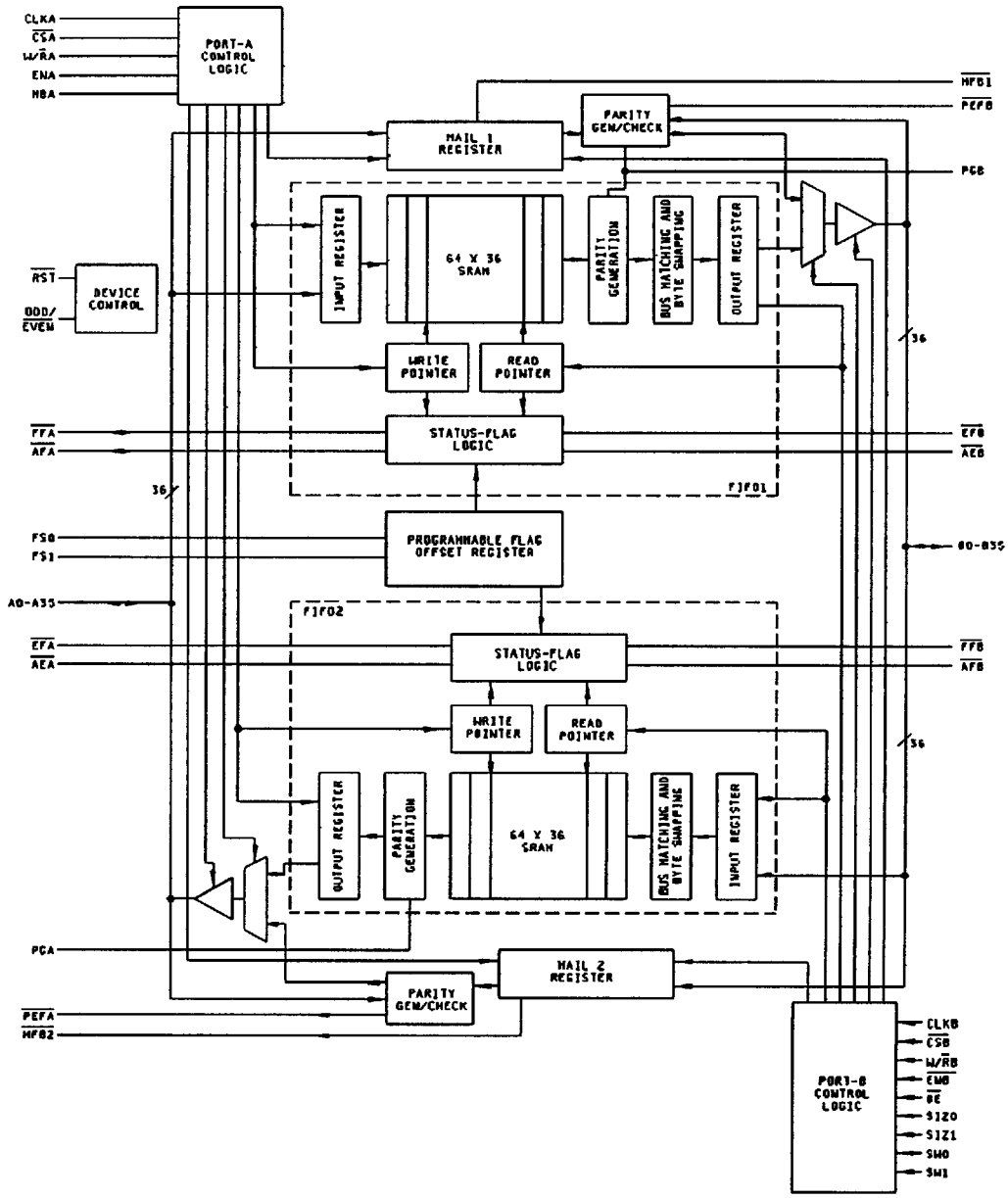
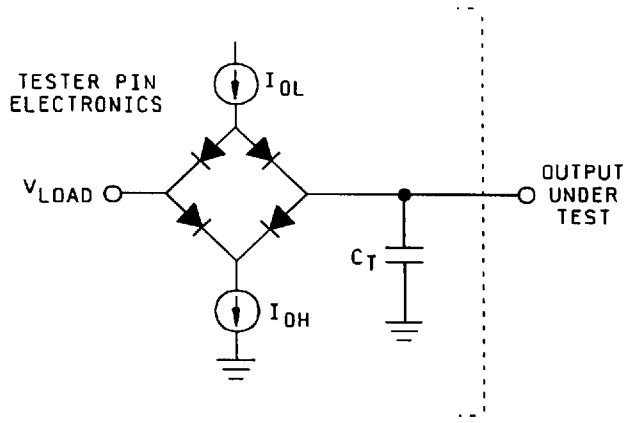
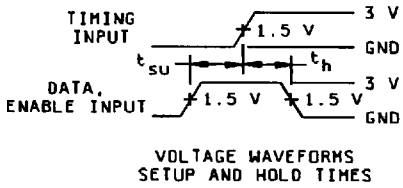


FIGURE 4. Block diagram.

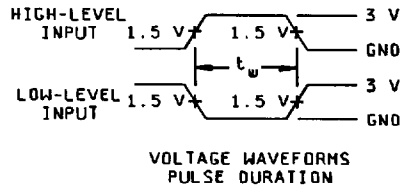
STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-95609
		REVISION LEVEL B	SHEET 14



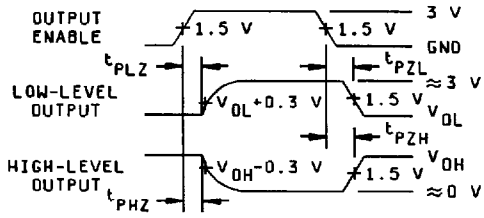
NOTE: I_{OL} = 8 mA (all outputs), I_{OH} = -4 mA (all outputs), and V_{LOAD} = 20 pF minimum load circuit capacitance.



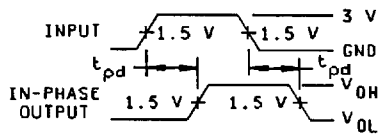
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

FIGURE 5. Test load circuit and voltage timing waveforms.

DEVICE RESET LOADING THE X REGISTER WITH THE VALUE OF EIGHT

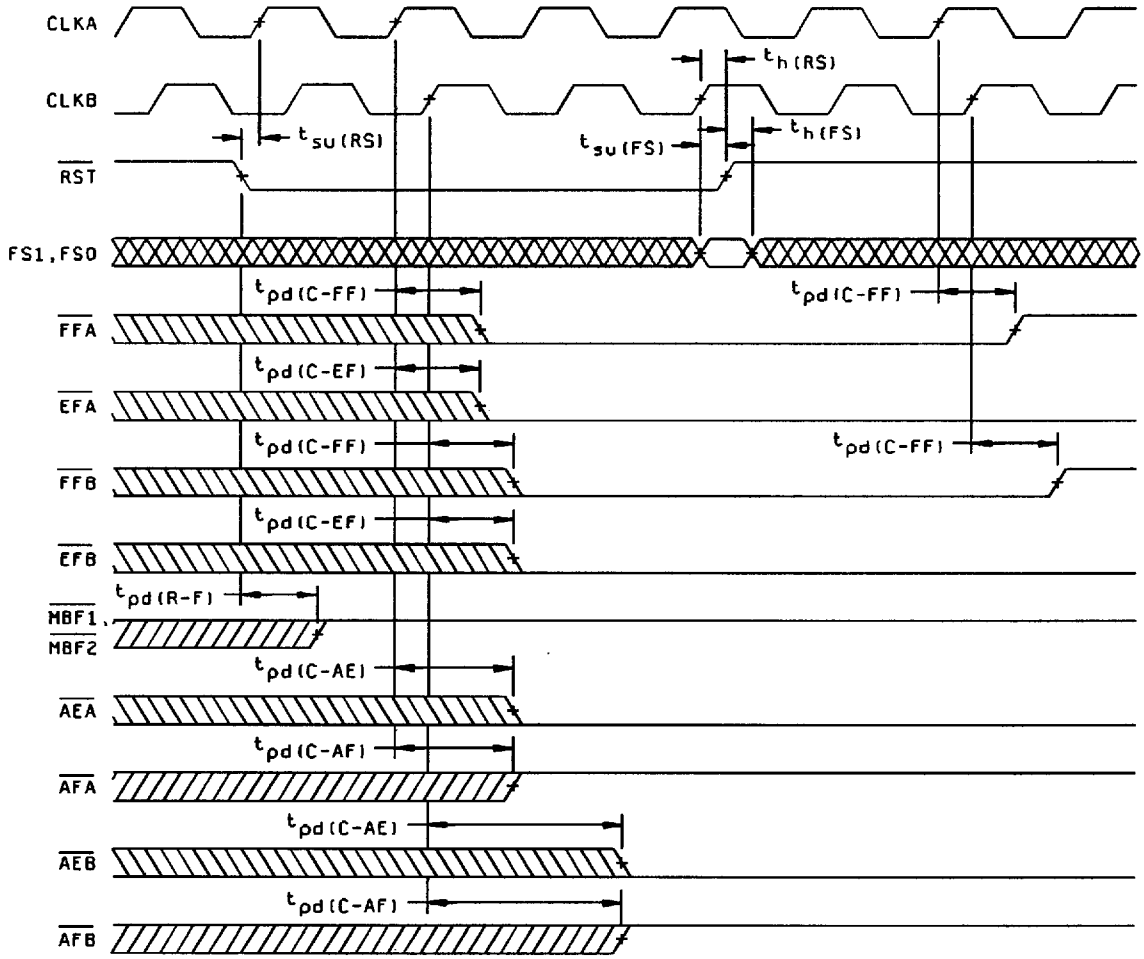
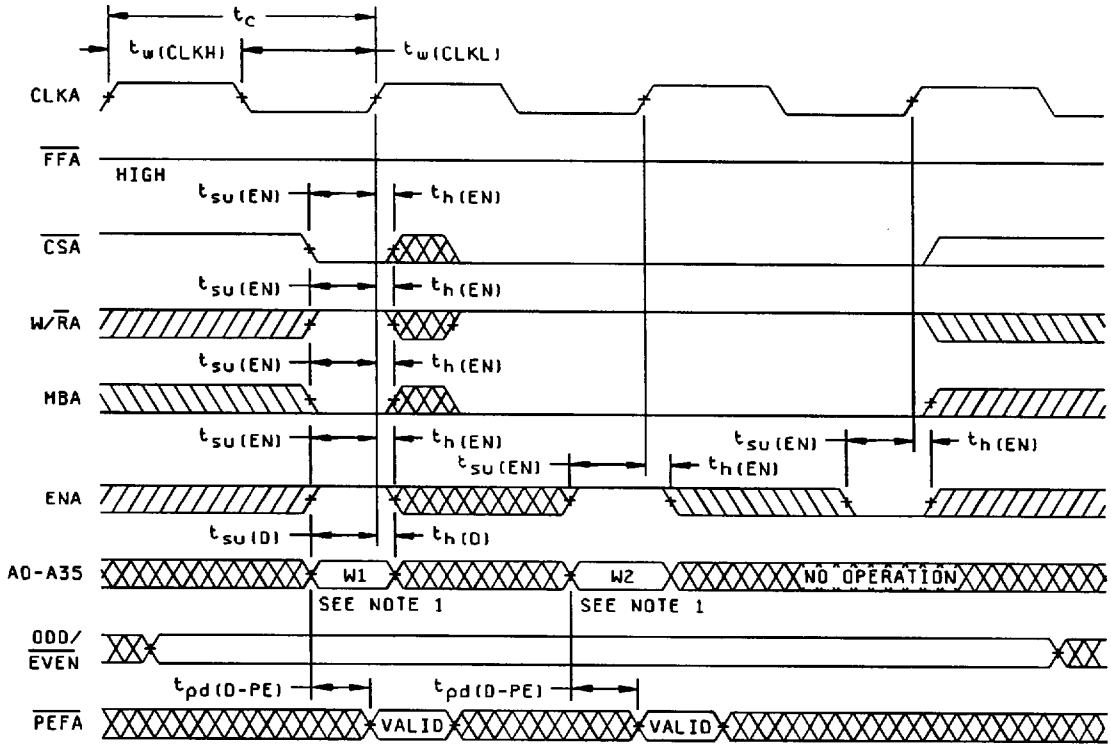


FIGURE 6. Timing waveforms - Continued.

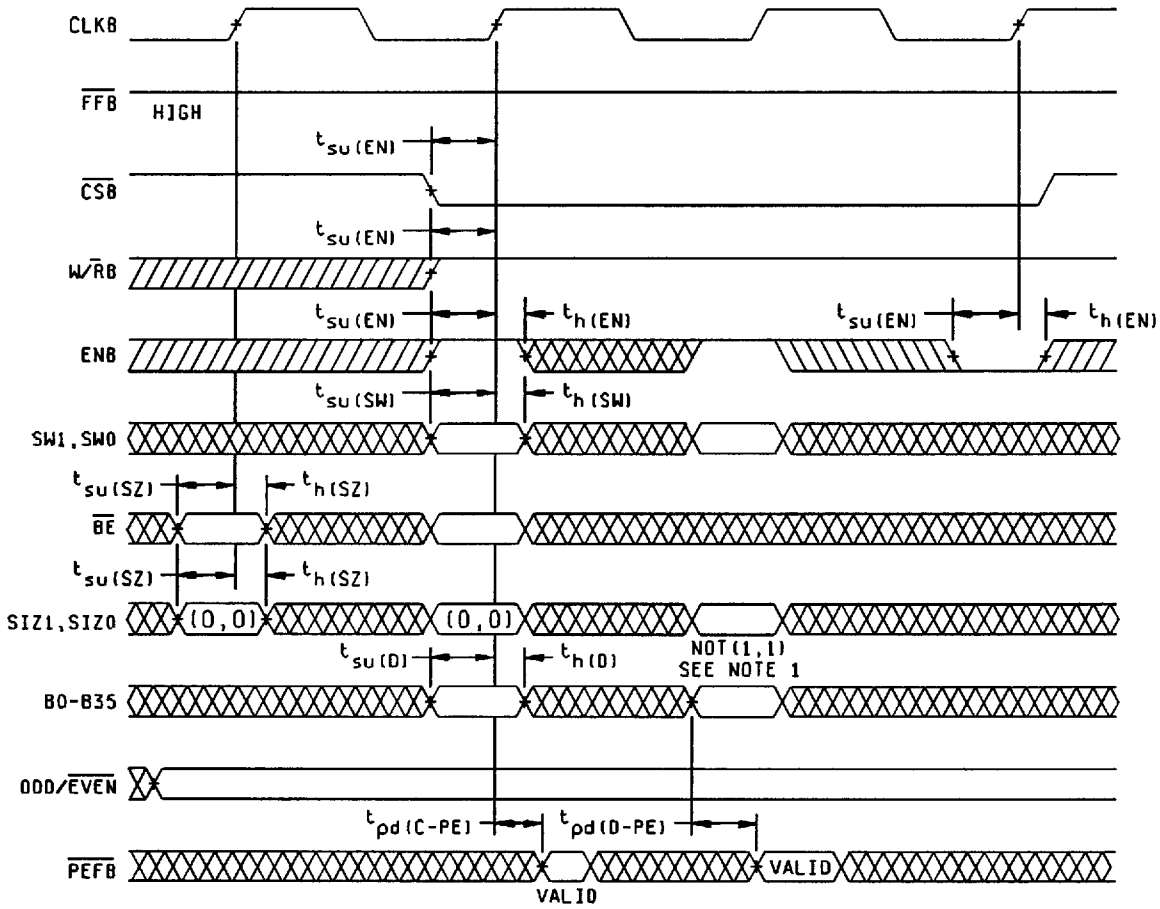
PORT-A WRITE CYCLE TIMING FOR FIFO1



NOTE: 1. Written to FIFO1.

FIGURE 6. Timing waveforms - Continued.

PORT-B LONG-WORD WRITE CYCLE TIMING FOR FIFO2 AND DATA SWAP TABLE FOR LONG-WORD WRITES TO FIFO2

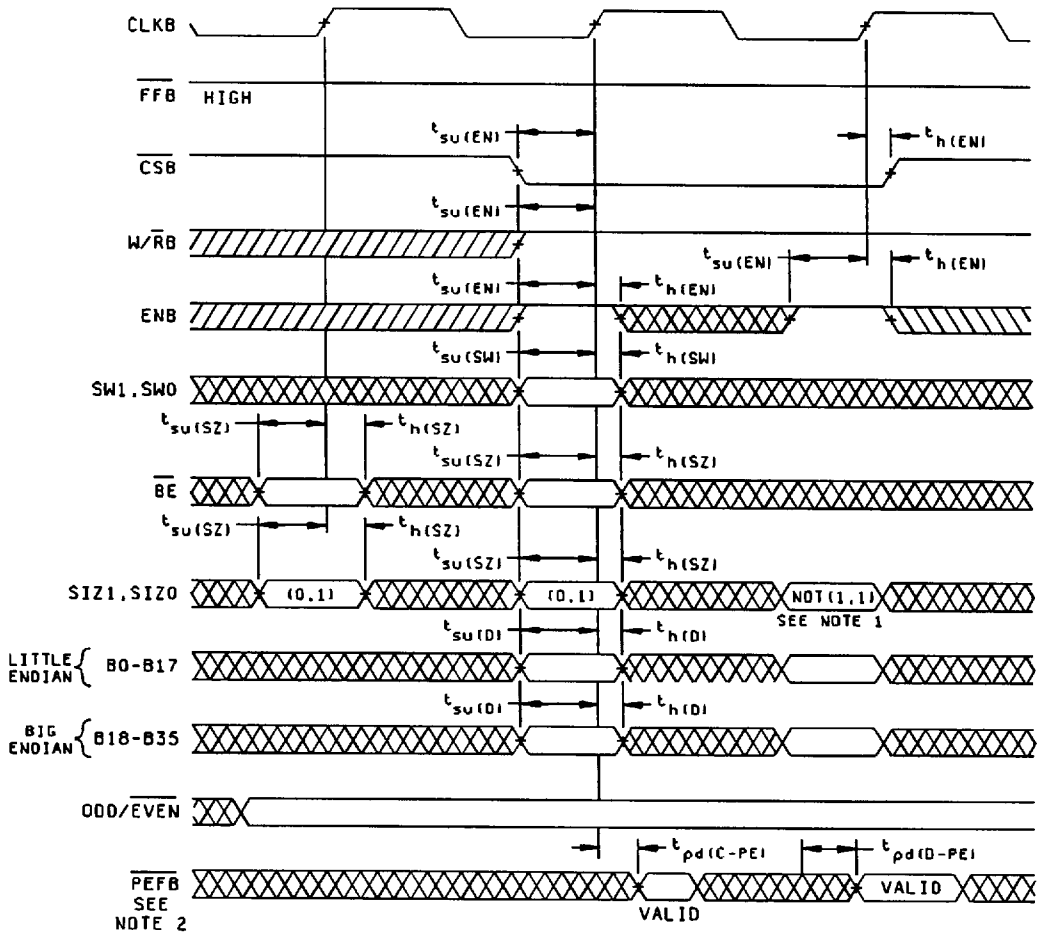


NOTE: 1. SIZ0 = H and SIZ1 = H writes data to the mail2 register.

SWAP MODE		DATA WRITTEN TO FIFO2				DATA READ FROM FIFO2			
SW1	SW0	B35-B27	B26-B18	B17-B9	B8-B0	A35-A27	A26-A18	A17-A9	A8-A0
L	L	A	B	C	D	A	B	C	D
L	H	D	C	B	A	A	B	C	D
H	L	C	D	A	B	A	B	C	D
H	H	B	A	D	C	A	B	C	D

FIGURE 6. Timing waveforms - Continued.

PORT-B WORD WRITE CYCLE TIMING FOR FIFO2 AND DATA SWAP TABLE FOR WORD WRITES TO FIFO2

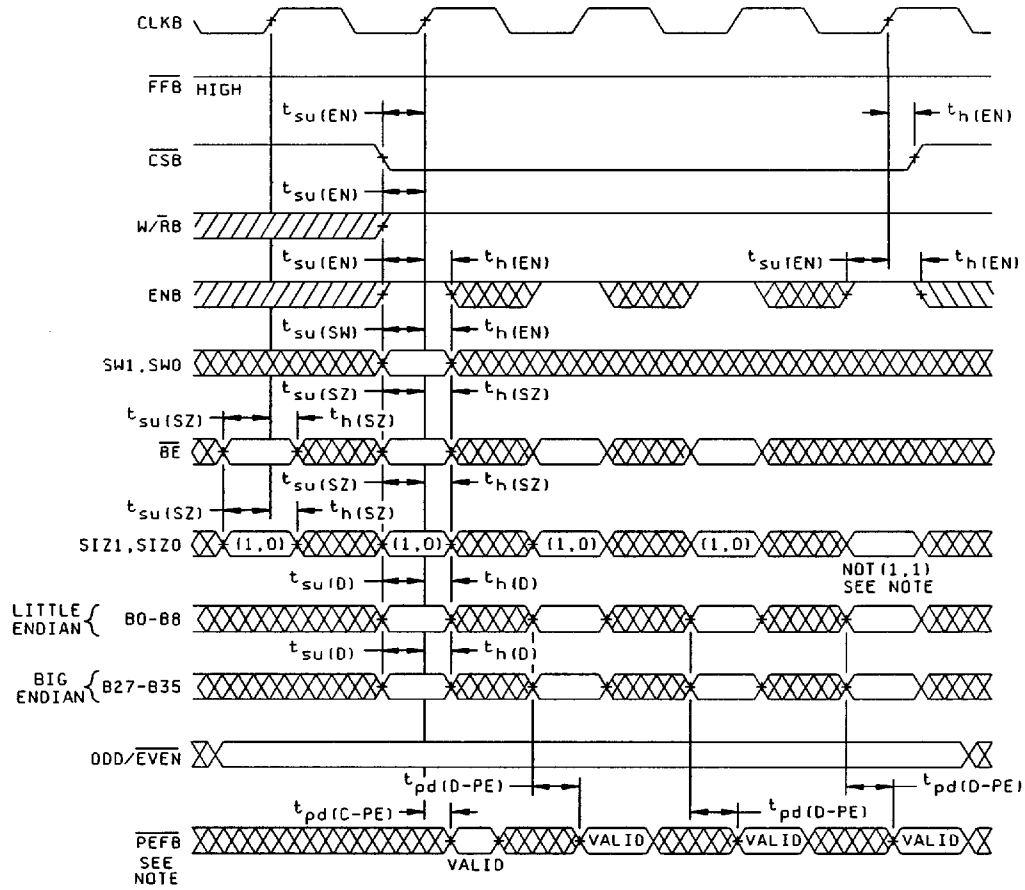


NOTES: 1. SIZ0 = H and SIZ1 = H writes data to the mail2 register.
2. PEFB indicates parity error for the following bytes: B35-B27 and B26-B18 for big-endian bus, and B17-B9 and B8-B0 for little-endian bus.

SWAP MODE		WRITE NO.	DATA WRITTEN TO FIFO2				DATA READ FROM FIFO2			
			BIG ENDIAN		LITTLE ENDIAN					
SW1	SW0		B35-B27	B26-B18	B17-B9	B8-B0	A35-A27	A26-A18	A17-A9	A8-A0
L	L	1	A	B	C	D	A	B	C	D
		2	C	D	A	B				
L	H	1	D	C	B	A	A	B	C	D
		2	B	A	D	C				
H	L	1	C	D	A	B	A	B	C	D
		2	A	B	C	D				
H	H	1	B	A	D	C	A	B	C	D
		2	D	C	B	A				

FIGURE 6. Timing waveforms - Continued.

PORT-B BYTE WRITE CYCLE TIMING FOR FIFO2 AND DATA SWAP TABLE FOR BYTE WRITES TO FIFO2

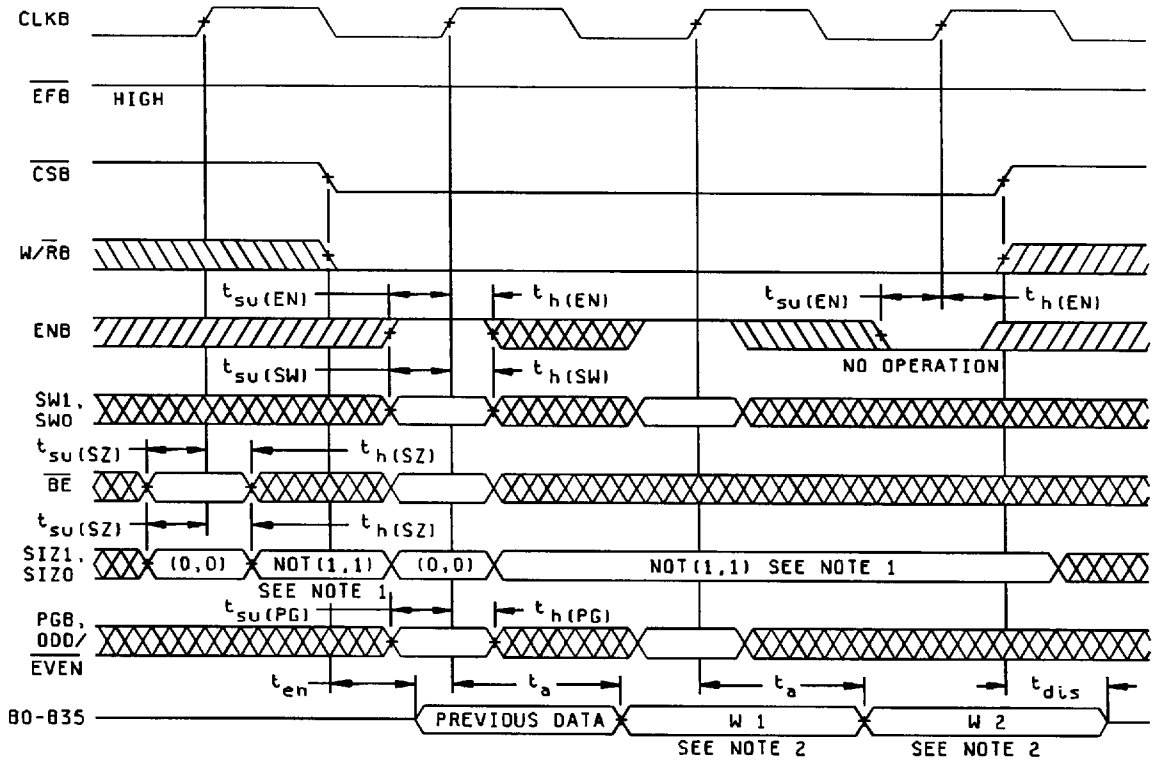


NOTE: See notes from sheet 18.

SWAP MODE		WRITE NO.	DATA WRITTEN TO FIFO2		DATA READ FROM FIFO2			
			BIG ENDIAN	LITTLE ENDIAN				
SW1	SW0		B35-B27	B8-B0	A35-A27	A26-A18	A17-A9	A8-A0
L	L	1	A	D	A	B	C	D
		2	B	C				
		3	C	B				
		4	D	A				
L	H	1	D	A	A	B	C	D
		2	C	B				
		3	B	C				
		4	A	D				
H	L	1	C	B	A	B	C	D
		2	D	A				
		3	A	D				
		4	B	C				
H	H	1	B	C	A	B	C	D
		2	A	D				
		3	D	A				
		4	C	B				

FIGURE 6. Timing waveforms - Continued.

PORT-B LONG-WORD READ CYCLE TIMING FOR FIFO1 AND DATA SWAP TABLE FOR LONG-WORD READS FROM FIFO1

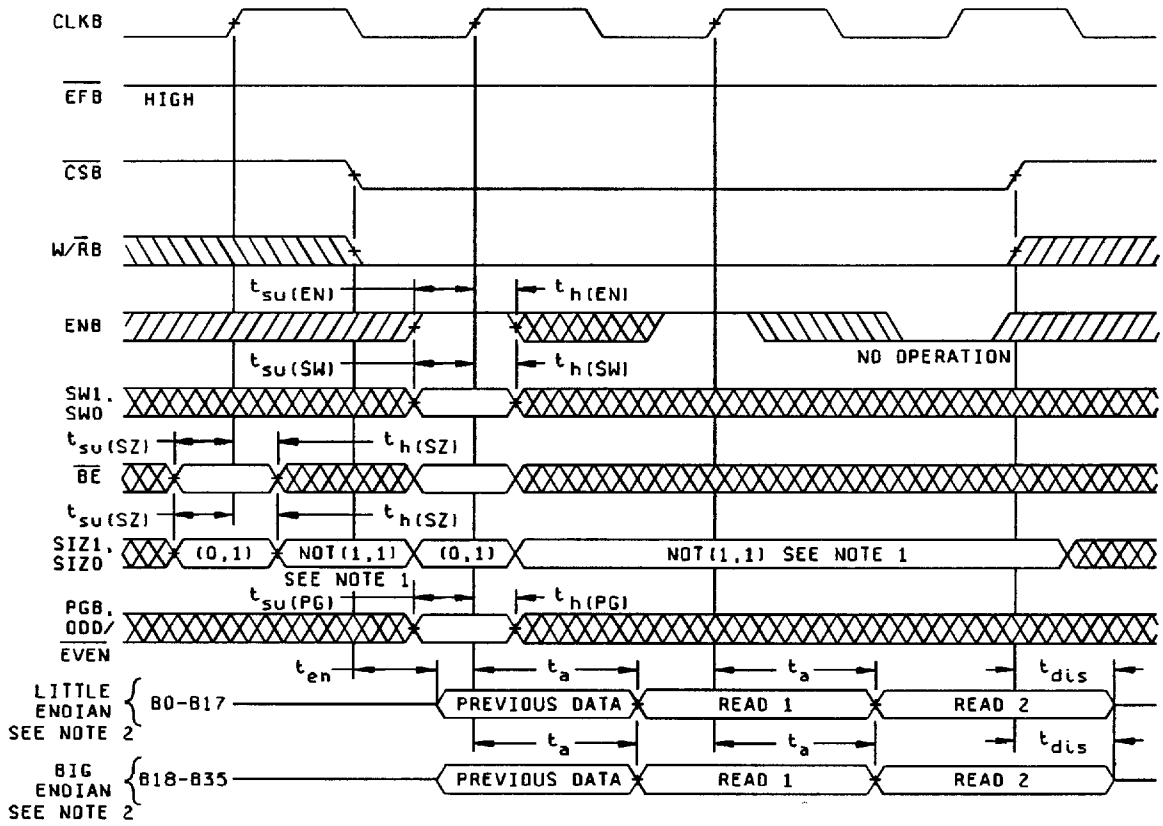


NOTES: 1. SIZ0 = H and SIZ1 = H selects the mail1 register for output on B0-B35.
2. Data read from FIFO1.

DATA WRITTEN TO FIFO1				SWAP MODE		DATA READ FROM FIFO1			
A35-A27	A26-A18	A17-A9	A8-A0	SW1	SW0	B35-B27	B26-B18	B17-B9	B8-B0
A	B	C	D	L	L	A	B	C	D
A	B	C	D	L	H	D	C	B	A
A	B	C	D	H	L	C	D	A	B
A	B	C	D	H	H	B	A	D	C

FIGURE 6. Timing waveforms - Continued.

PORT-B WORD READ CYCLE TIMING FOR FIFO1 AND DATA SWAP TABLE FOR WORD READS FROM FIFO1

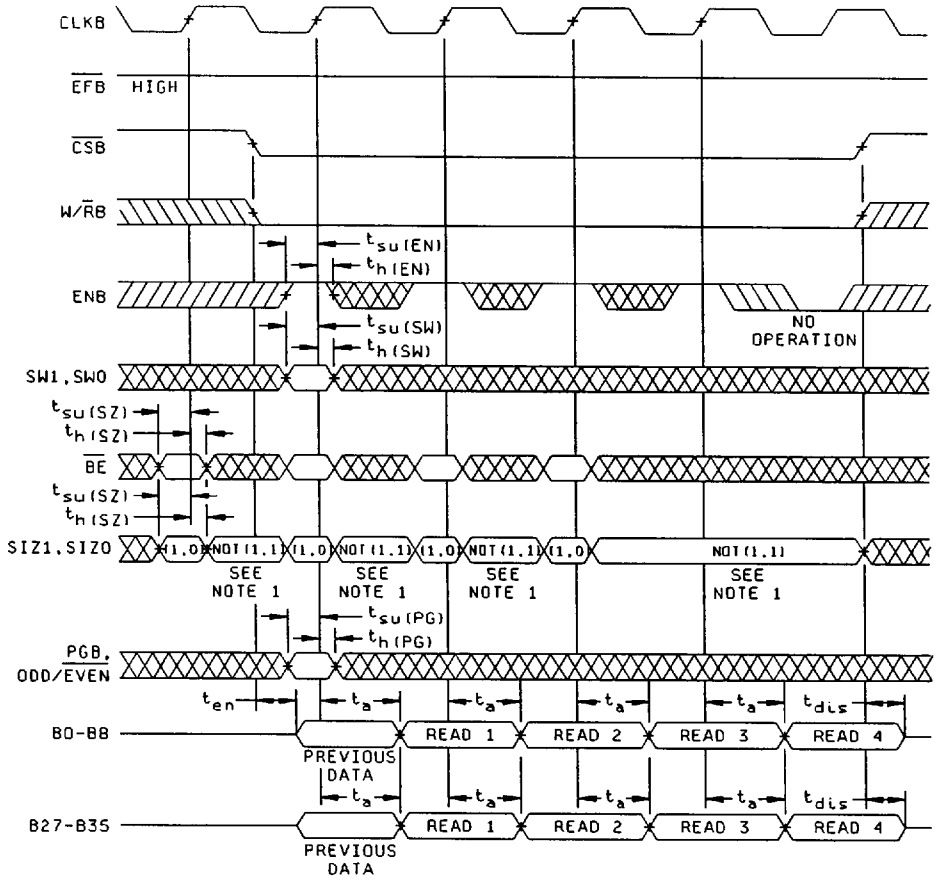


NOTES: 1. SIZ0 = H and SIZ1 = H selects the mail1 register for output on B0-B35.
2. Unused word B0-B17 or B18-B35 holds last FIFO1 output register data for word-size reads.

DATA WRITTEN TO FIFO1				SWAP MODE		READ NO.	DATA READ FROM FIFO1			
							BIG ENDIAN		LITTLE ENDIAN	
A35-A27	A26-A18	A17-A9	A8-A0	SW1	SW0		B35-B27	B26-B18	B17-B9	B8-B0
A	B	C	D	L	L	1	A	B	C	D
						2	C	D	A	B
A	B	C	D	L	H	1	D	C	B	A
						2	B	A	D	C
A	B	C	D	H	L	1	C	D	A	B
						2	A	B	C	D
A	B	C	D	H	H	1	B	A	D	C
						2	D	C	B	A

FIGURE 6. Timing waveforms - Continued.

PORT-B BYTE READ CYCLE TIMING FOR FIFO1 AND DATA SWAP TABLE FOR BYTE READS FROM FIFO1

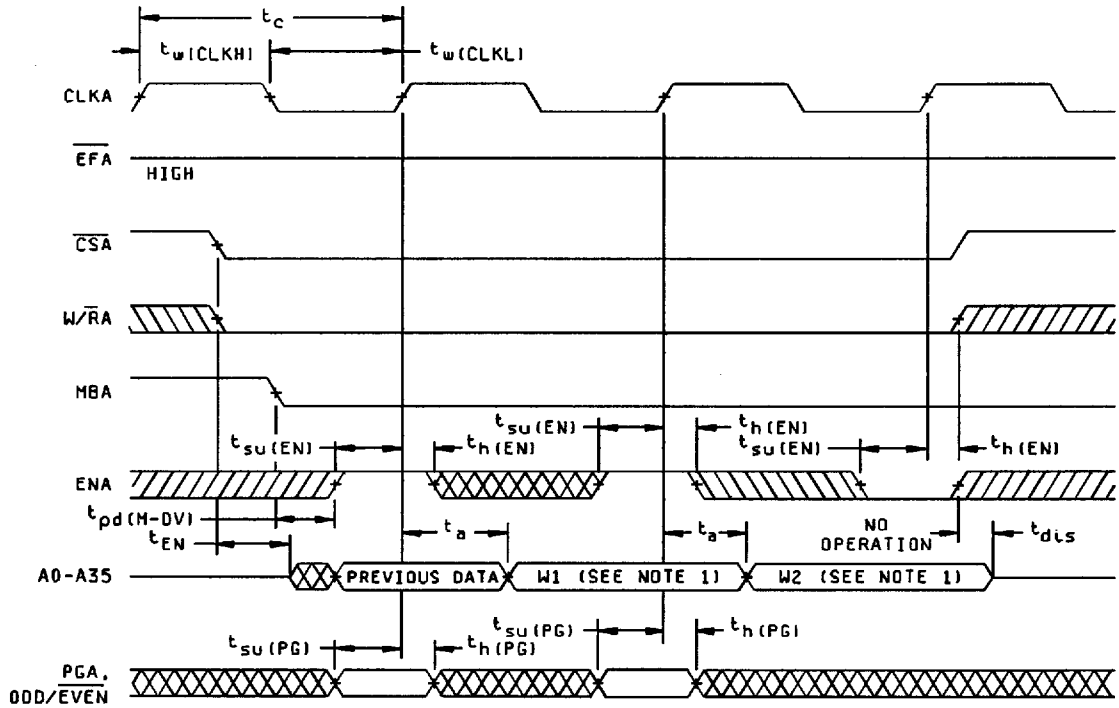


NOTES: 1. SIZ0 = H and SIZ1 = H selects the mail1 register for output on B0-B35.
2. Unused bytes hold last FIFO1 output register data for byte-size reads.

DATA WRITTEN TO FIFO1				SWAP MODE		READ NO.	DATA READ FROM FIFO1	
							BIG ENDIAN	LITTLE ENDIAN
A35-A27	A26-A18	A17-A9	A8-A0	SW1	SW0		B35-B27	B8-B0
A	B	C	D	L	L	1	A	D
						2	B	C
						3	C	B
						4	D	A
A	B	C	D	L	H	1	D	A
						2	C	B
						3	B	C
						4	A	D
A	B	C	D	H	L	1	C	B
						2	D	A
						3	A	D
						4	B	C
A	B	C	D	H	H	1	B	C
						2	A	D
						3	D	A
						4	C	B

FIGURE 6. Timing waveforms - Continued.

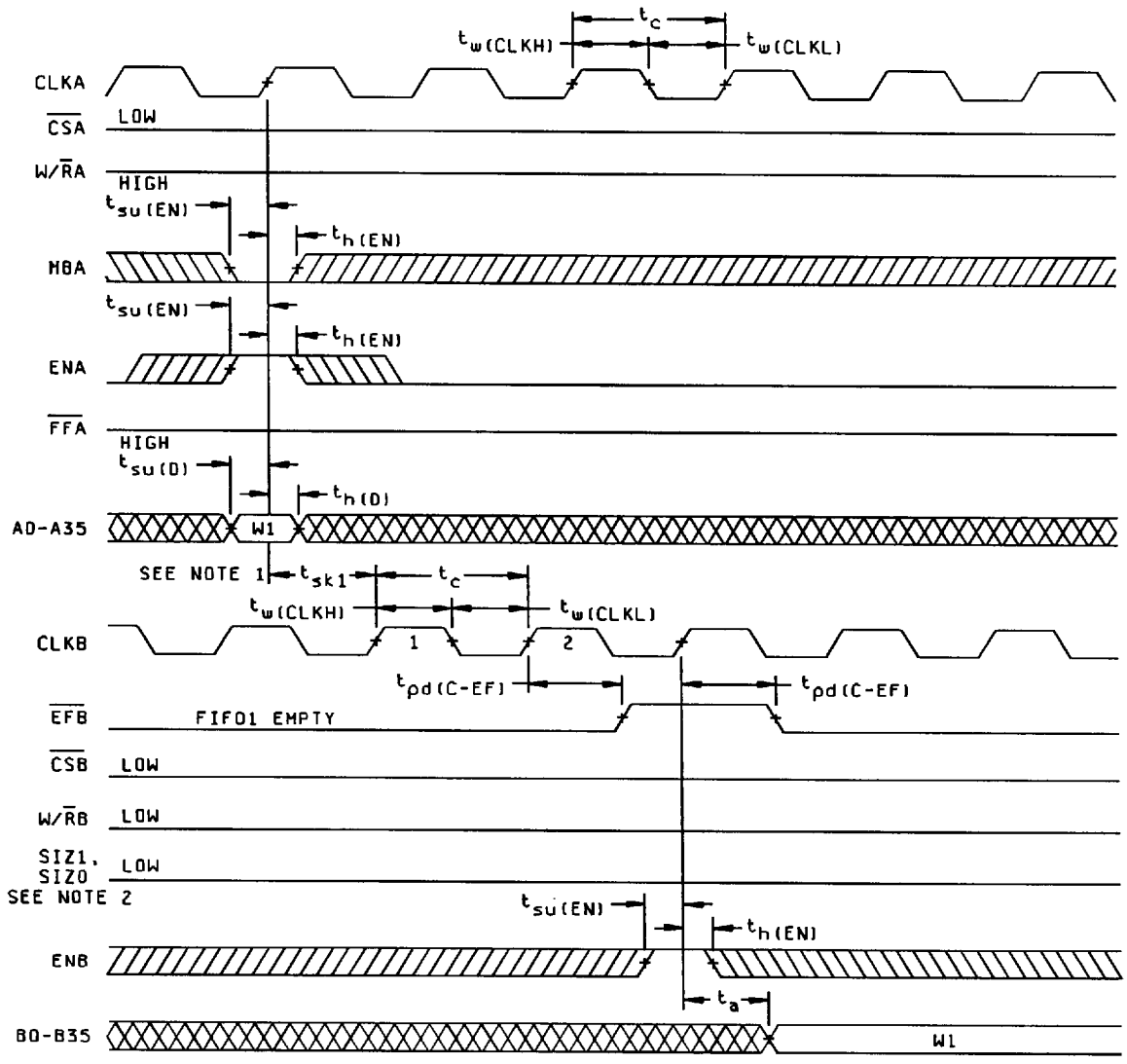
PORT-A READ CYCLE TIMING FOR FIFO2



NOTE: 1. Read from FIFO2.

FIGURE 6. Timing waveforms - Continued.

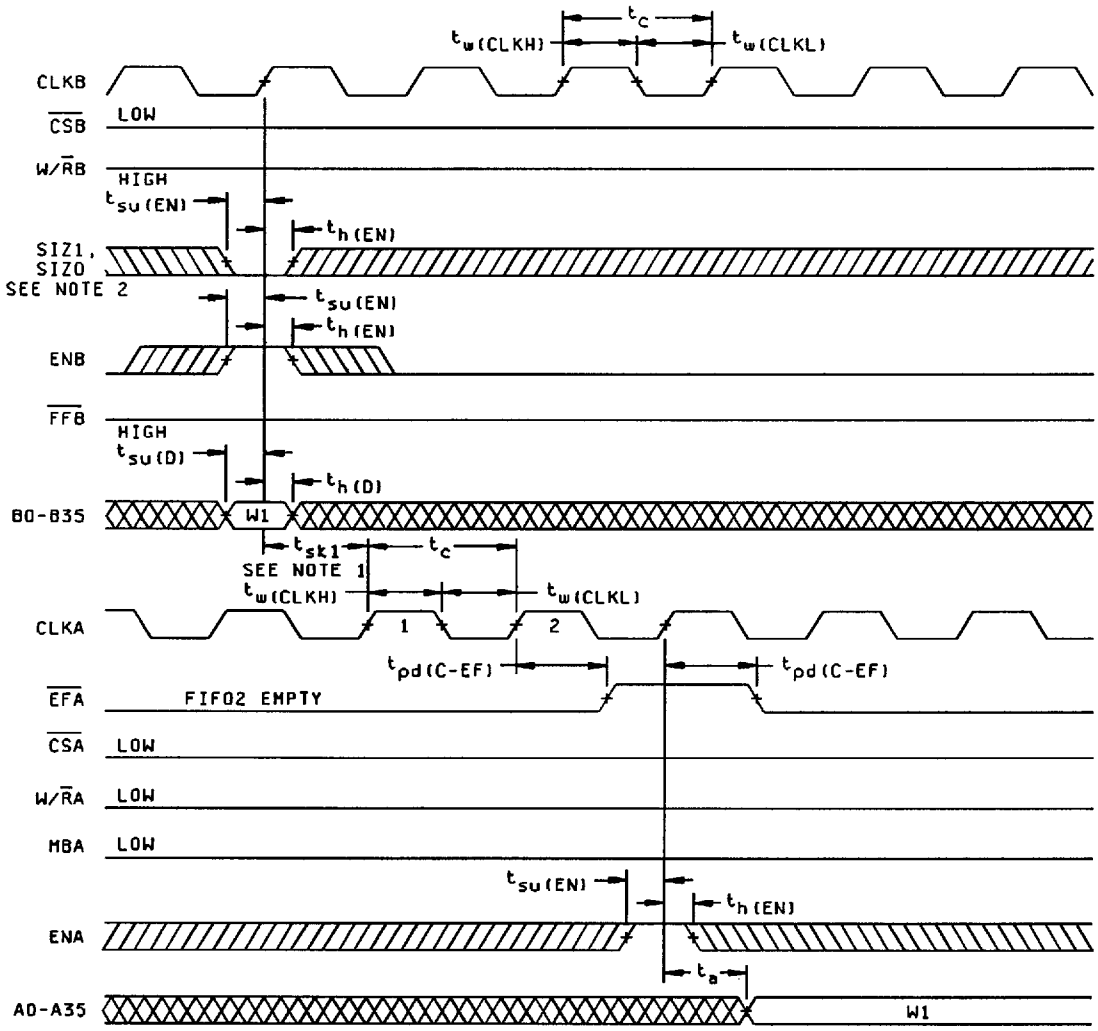
EFB FLAG TIMING AND FIRST DATA READ WHEN FIFO1 IS EMPTY



NOTES: 1. t_{sk1} is the minimum time between a rising CLKA edge and a rising CLKB edge for EFB to transition high in the next CLKB cycle. If the time between CLKA edge and rising CLKB edge is less than t_{sk1}, then the transition of EFB high may occur one CLKB cycle later than shown.
2. Port-B size of long word is selected for FIFO1 read by SIZ1 = L, SIZ0 = L. If port-B size is word or byte, EFB is set low by the last word or byte read from FIFO1, respectively.

FIGURE 6. Timing waveforms - Continued.

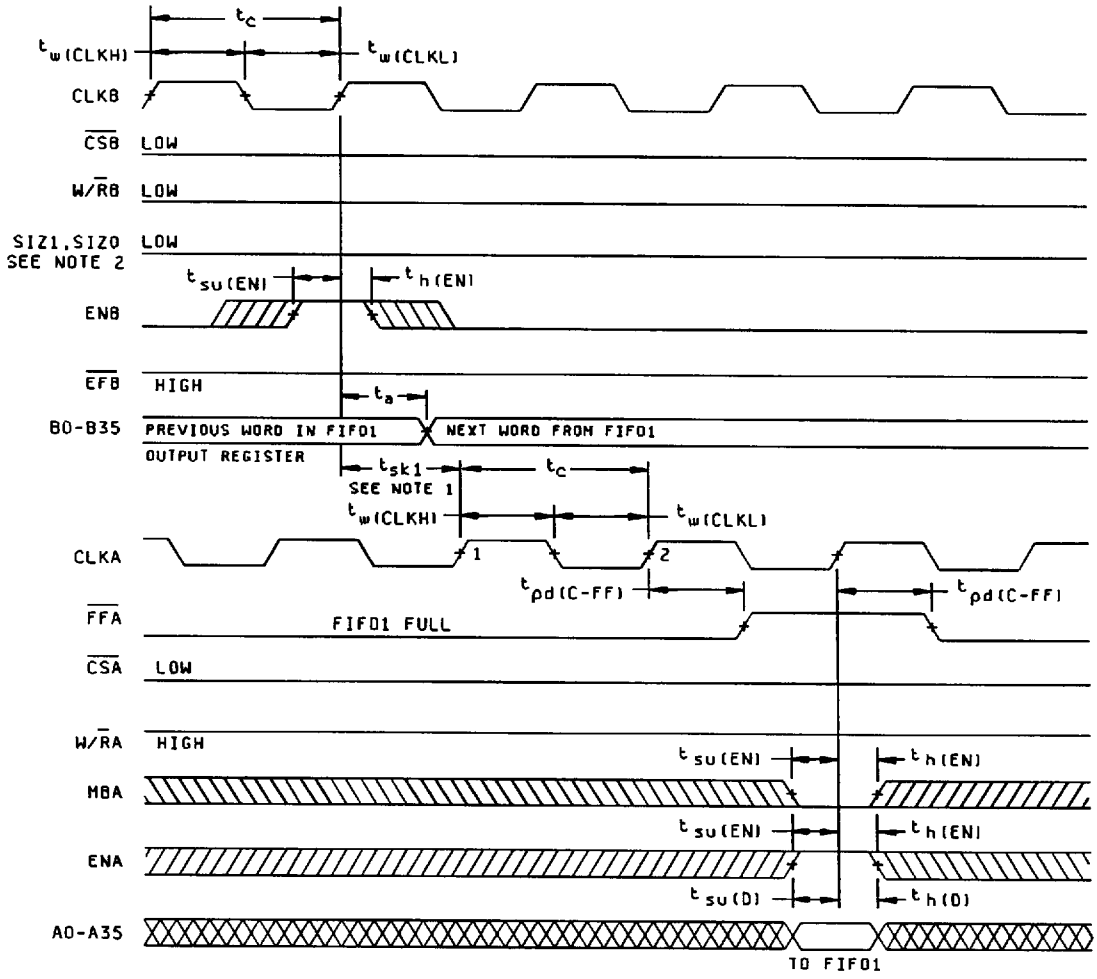
EFA FLAG TIMING AND FIRST DATA READ WHEN FIFO2 IS EMPTY



NOTES: 1. t_{sk1} is the minimum time between a rising CLKB edge and a rising CLKA edge for EFA to transition high in the next CLKA cycle. If the time between the rising CLKA edge is less than t_{sk1}, then the transition of EFA high may occur one CLKA cycle later than shown.
2. Port-B size of long word is selected for FIFO2 write by SIZ1 = L, SIZ0 = L. If port-B size is word or byte, t_{sk1} is referenced to the rising CLKB edge that writes the last word or byte of the long word, respectively.

FIGURE 6. Timing waveforms - Continued.

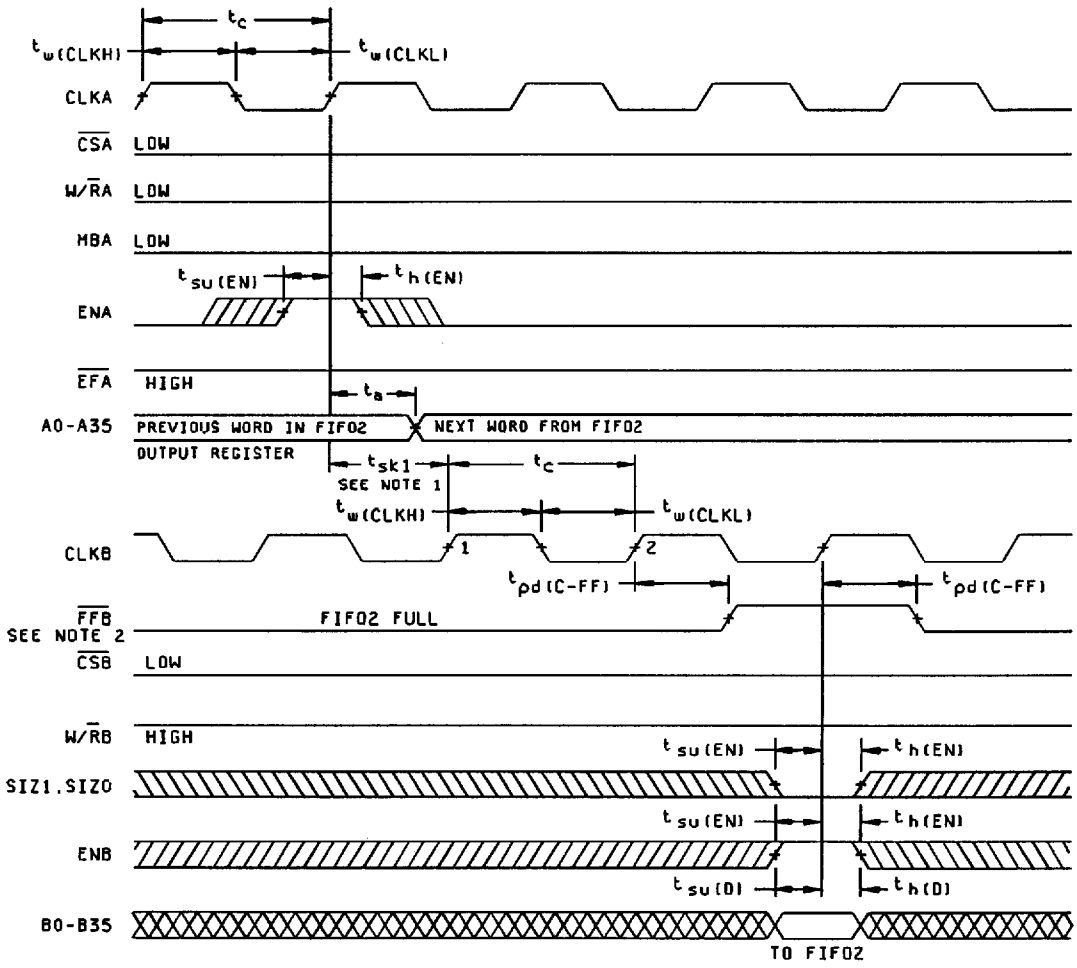
FFA FLAG TIMING AND FIRST AVAILABLE WRITE WHEN FIFO1 IS FULL



NOTES: 1. t_{sk1} is the minimum time between a rising CLKB edge and a rising CLKA edge for FFA to transition high in the next CLKA cycle. If the time between the rising CLKB edge and the rising CLKA edge is less than t_{sk1}, then FFA may transition high one CLKA cycle later than shown.
2. Port-B size of long word is selected for FIFO1 read by SIZ1 = L, SIZ0 = L. If port-B size is word or byte, t_{sk1} is referenced from the rising CLKB edge that reads the last word or byte of the long word, respectively.

FIGURE 6. Timing waveforms - Continued.

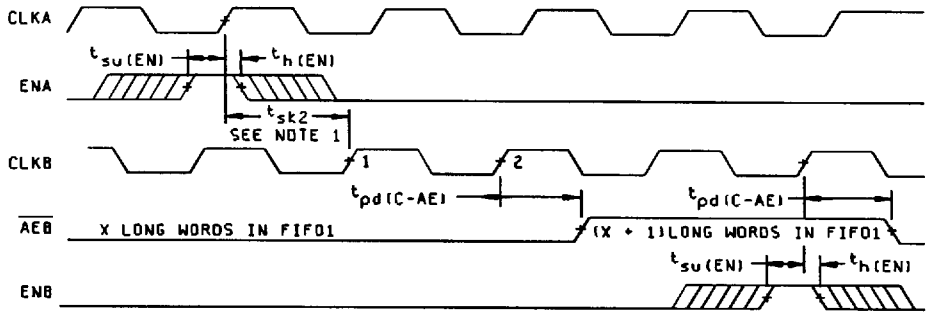
FFB FLAG TIMING AND FIRST AVAILABLE WRITE WHEN FIFO2 IS FULL



NOTES: 1. t_{sk1} is the minimum time between a rising CLKA edge and a rising CLKB edge for FFB to transition high in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{sk1}, then FFB may transition high one CLKB cycle later than shown.
2. Port-B size of long word is selected for FIFO1 read by SIZ1 = L, SIZ0 = L. If port-B size is word or byte, FFB is set low by the last word or byte of the long word, respectively.

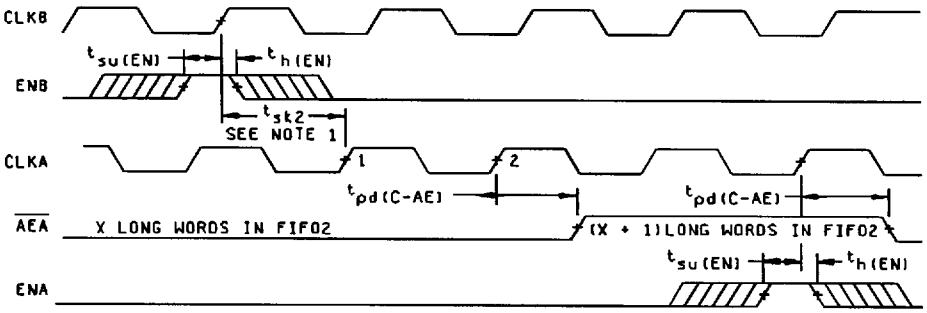
FIGURE 6. Timing waveforms - Continued.

TIMING FOR $\overline{AEB}$ WHEN FIFO1 IS ALMOST EMPTY



NOTES: 1. t_{sk2} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{AEB}$ to transition high in the next CLKB cycle. If the time between CLKA edge and rising CLKB edge is less than t_{sk2}, then $\overline{AEB}$ may transition high one CLKB cycle later than shown.
2. FIFO1 write (CSA = L, W/RA = H, MBA = L), FIFO1 read (CSB = L, W/RB = L, MBB = L).
3. Port-B size of long word is selected for FIFO1 read by SIZ1 = L, SIZ0 = L. If port-B size is word or byte, $\overline{AEB}$ is set low by the first word or byte read of the long word, respectively.

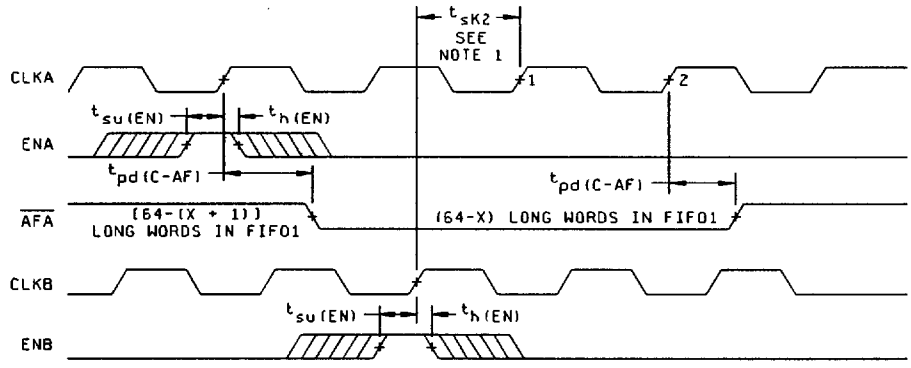
TIMING FOR $\overline{AEA}$ WHEN FIFO2 IS ALMOST EMPTY



NOTES: 1. t_{sk2} is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{AEA}$ to transition high in the next CLKA cycle. If the time between CLKB edge and rising CLKA edge is less than t_{sk2}, then $\overline{AEA}$ may transition high one CLKA cycle later than shown.
2. FIFO2 write (CSB = L, W/RB = H, MBB = L), FIFO2 read (CSA = L, W/RA = L, MBA = L).
3. Port-B size of long word is selected for FIFO2 write by SIZ1 = L, SIZ0 = L. If port-B size is word or byte, t_{sk2} is referenced from the rising CLKB edge that writes the last word or byte of the long word respectively.

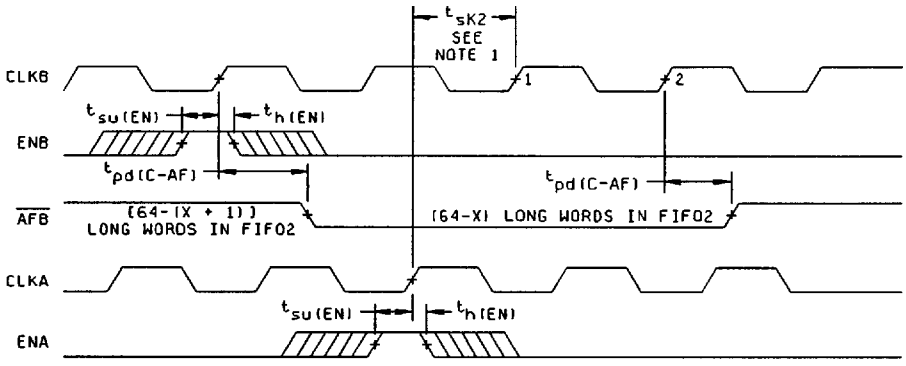
FIGURE 6. Timing waveforms - Continued.

TIMING FOR AFA WHEN FIFO1 IS ALMOST FULL



NOTES: 1. t_{sk2} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{AFA}$ to transition high in the next CLKA cycle. If the time between CLKA edge and rising CLKB edge is less than t_{sk2}, then $\overline{AFA}$ may transition high one CLKB cycle later than shown.
2. FIFO1 write (CSA = L, W/RA = H, MBA = L), FIFO1 read (CSB = L, W/RB = L, MBB = L).
3. Port-B size of long word is selected for FIFO1 read by SIZ1 = L, SIZ0 = L. If port-B size is word or byte, t_{sk2} is referenced from first word or byte read of the long word, respectively.

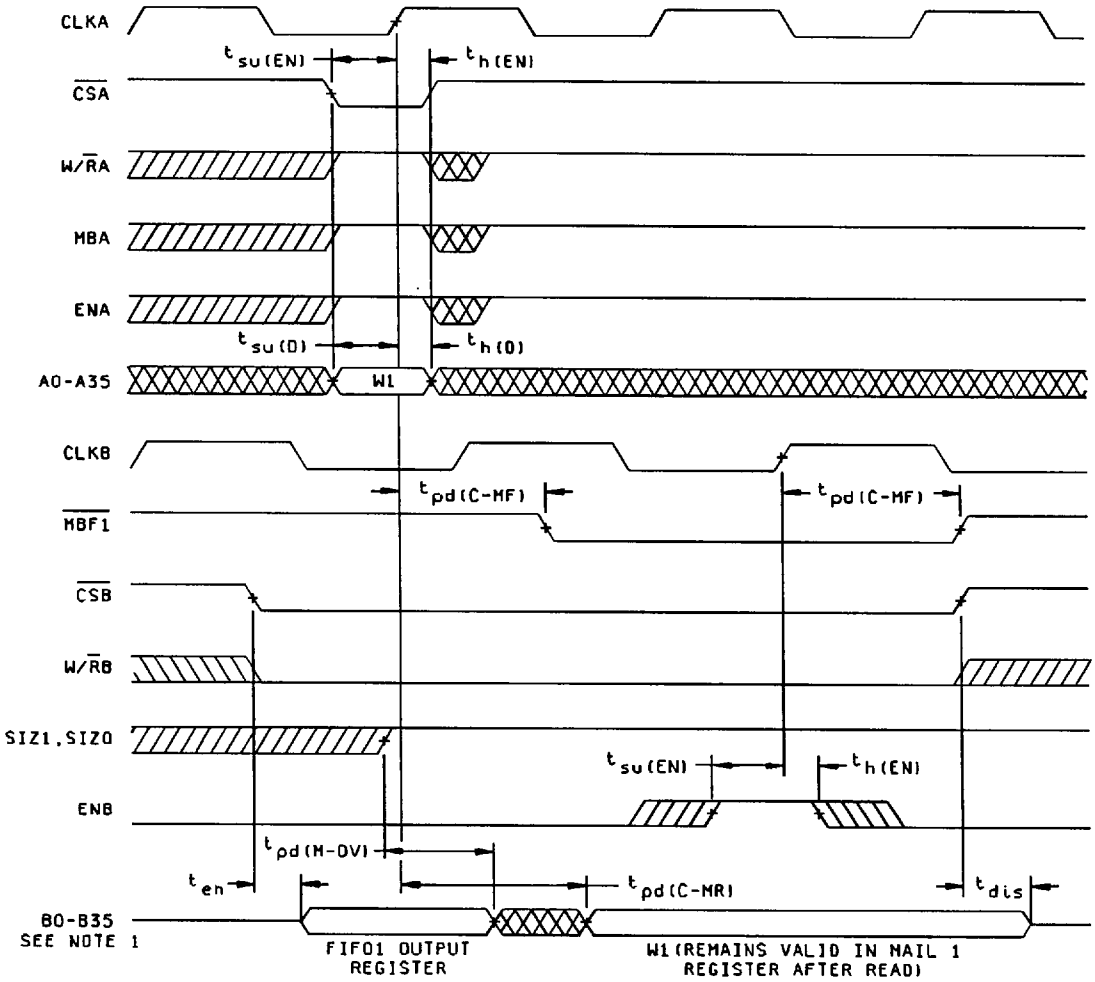
TIMING FOR AFB WHEN FIFO2 IS ALMOST FULL



NOTES: 1. t_{sk2} is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{AFB}$ to transition high in the next CLKB cycle. If the time between CLKB edge and rising CLKA edge is less than t_{sk2}, then $\overline{AFB}$ may transition high one CLKA cycle later than shown.
2. FIFO2 write (CSB = L, W/RB = H, MBB = L), FIFO2 read (CSA = L, W/RA = L, MBA = L).
3. Port-B size of long word is selected for FIFO2 write by SIZ1 = L, SIZ0 = L. If port-B size is word or byte, $\overline{AFB}$ is set low by the last word or byte read of the long word, respectively.

FIGURE 6. Timing waveforms - Continued.

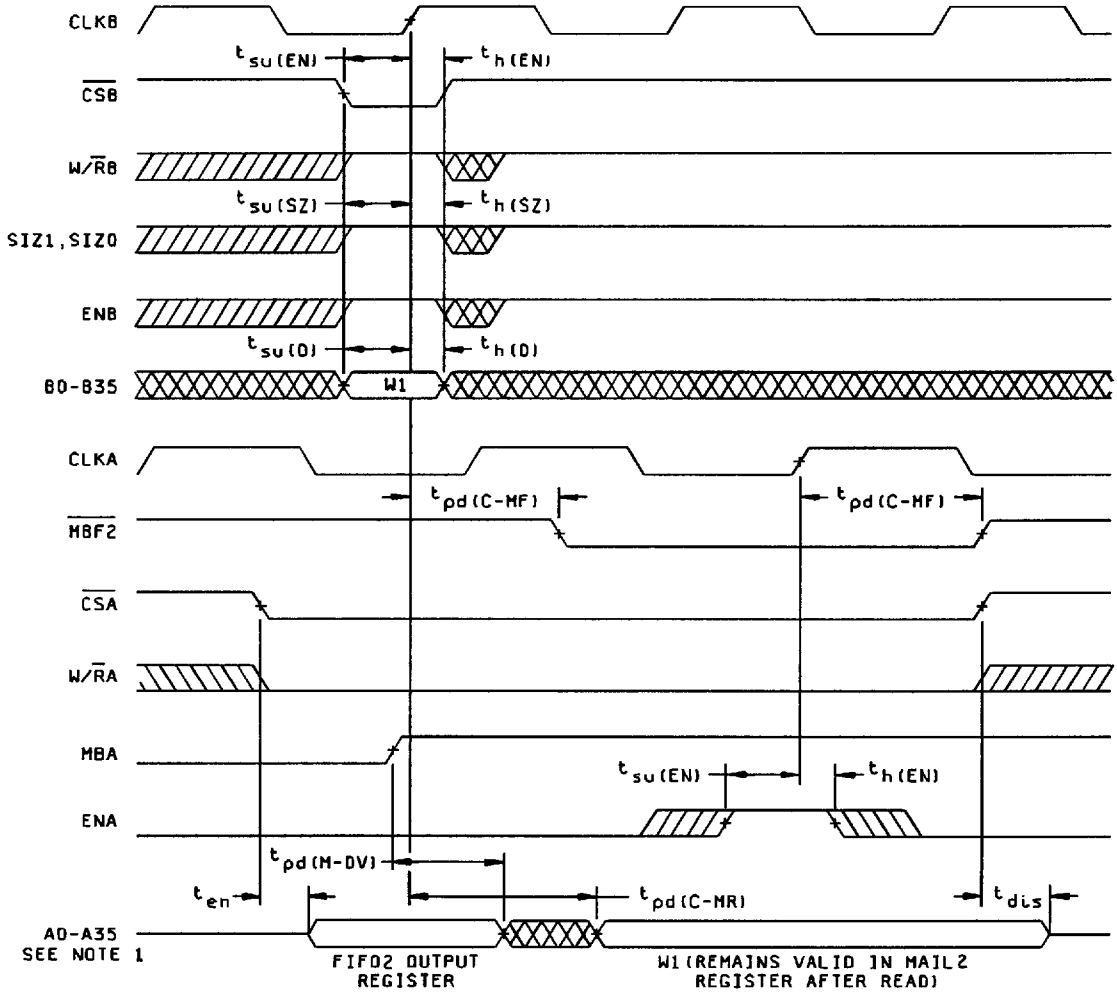
TIMING FOR MAIL1 REGISTER AND MBF1 FLAG



NOTE: 1. Port-B parity generaton off (PGB = L)

FIGURE 6. Timing waveforms - Continued.

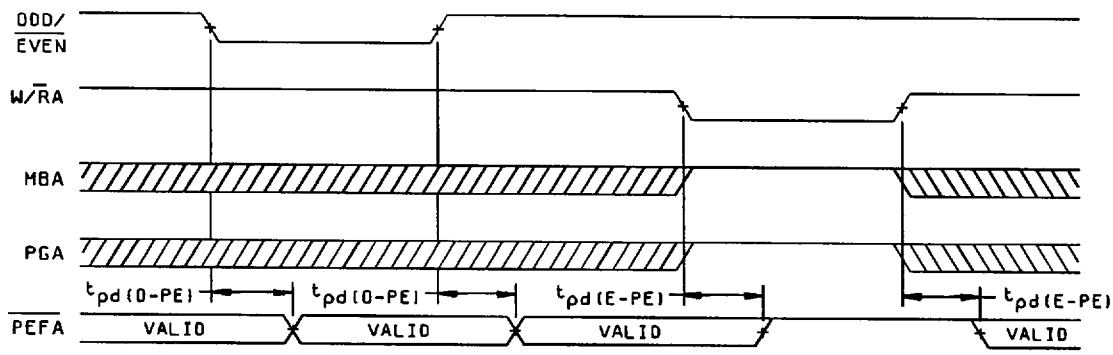
TIMING FOR MAIL2 REGISTER AND MBF2 FLAG



NOTE: 1. Port-A parity generation off (PGA = L).

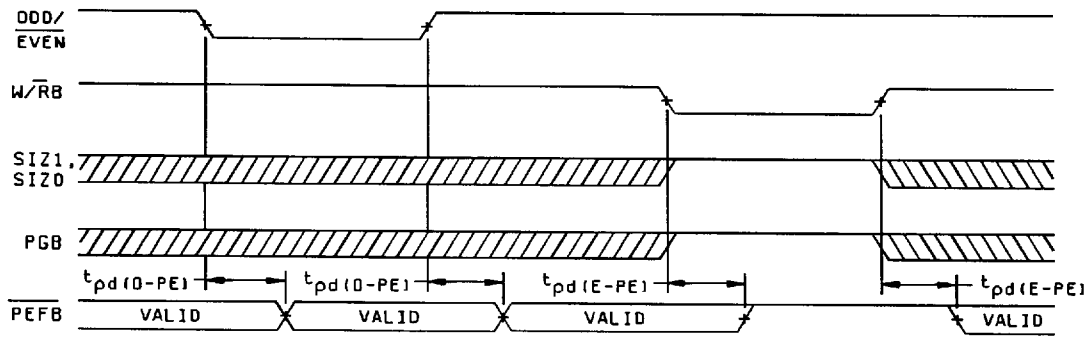
FIGURE 6. Timing waveforms - Continued.

ODD/EVEN, W/RA, MBA, AND PGA TO PEFA TIMING



NOTE: 1. ENA is high and CSA is low.

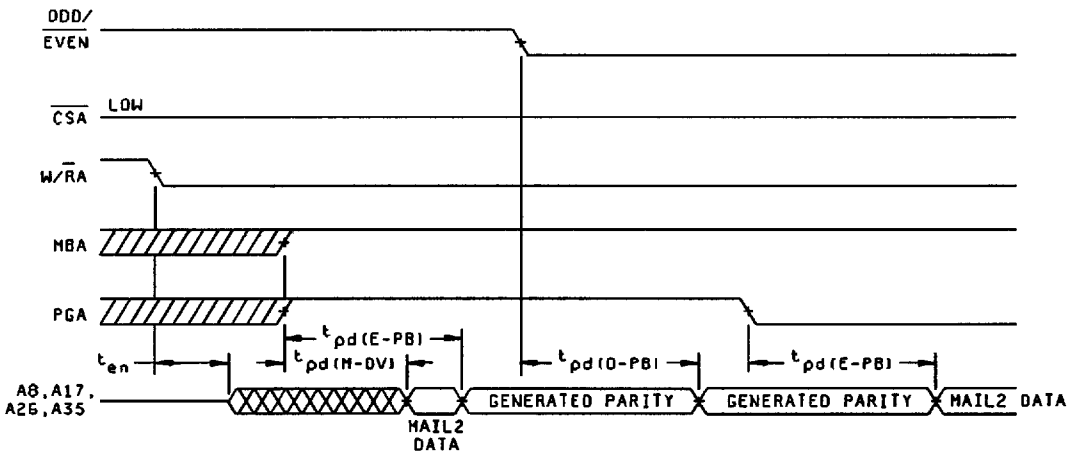
ODD/EVEN, W/RB, SIZ1, SIZ0, AND PGB TO PEFB TIMING



NOTE: 1. ENB is high and CSB is low.

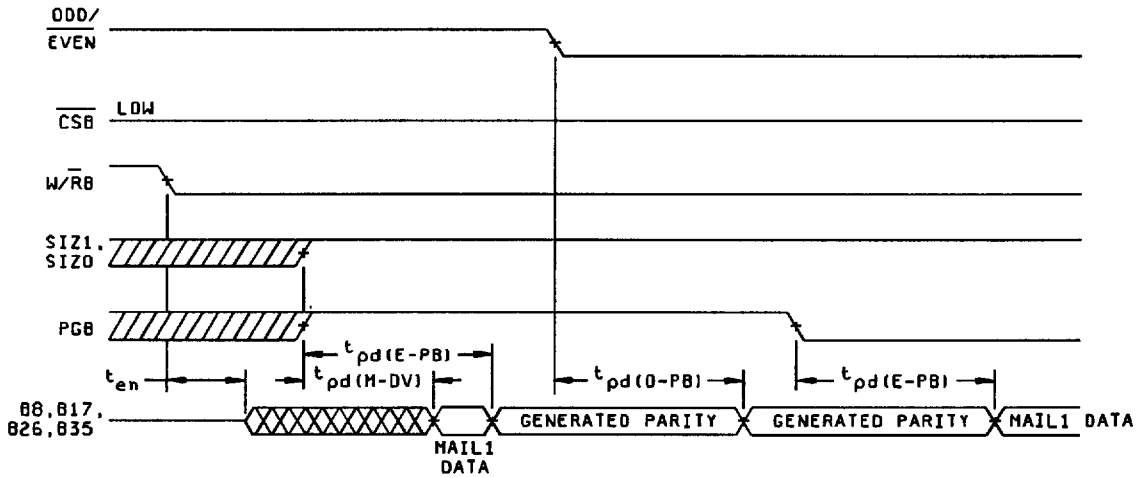
FIGURE 6. Timing waveforms - Continued.

PARITY GENERATION TIMING WHEN READING FROM THE MAIL2 REGISTER



NOTE: 1. ENA is high.

PARITY GENERATION TIMING WHEN READING FROM THE MAIL1 REGISTER



NOTE: 1. ENB is high.

FIGURE 6. Timing waveforms - Continued.

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (in accordance with MIL-STD-883, TM 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)		
		Device class M	Device class N	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)				1,7,9
2	Static burn-in I and II (method 1015)	Not required		Not required	Required
3	Same as line 1				1*,7* Δ
4	Dynamic burn-in (method 1015)	Required		Required	Required
5	Same as line 1				1*,7* Δ
6	Final electrical parameters	1*,2,3,7*, 8A,8B,9,10, 11	2,8A,10	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9, 10,11
7	Group A test requirements	1,2,3,4**,7, 8A,8B,9,10, 11	2,8A,10	1,2,3,4**,7, 8A,8B,9,10, 11	1,2,3,4**,7, 8A,8B,9,10, 11
8	Group C end-point electrical parameters	2,3,7, 8A,8B		1,2,3,7, 8A,8B	1,2,3,7, 8A,8B,9, 10,11 Δ
9	Group D end-point electrical parameters	2,3, 8A,8B		2,3, 8A,8B	2,3, 8A,8B
10	Group E end-point electrical parameters	1,7,9		1,7,9	1,7,9

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall verify the truth table.
4/ * indicates PDA applies to subgroup 1 and 7.
5/ ** see 4.4.1e.
6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).
7/ See 4.4.1d.

TABLE IIB. Delta limits at +25°C.

Parameter 1/	Device types
	All
I_I	±10%
I_{OZH}, I_{OZL}	±10%

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 105 (see MIL-PRF-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes N, Q, and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes N, Q, and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Delete the sequence specified as initial (preburn-in) electrical parameters through interim (postburn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.

b. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(1) Dynamic burn-in for device class M (method 1015 of MIL-STD-883, test condition D; for circuit, see 4.2.1b herein).

c. Interim and final electrical parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes N, Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-PRF-38535.

4.3 Qualification inspection for device classes N, Q, and V. Qualification inspection for device classes N, Q, and V shall be in accordance with MIL-PRF-38535 and the device manufacturer's QM plan. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes N, Q, and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes N, Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M, procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes N, Q and V, the procedures and circuits shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC Standard number 17 may be used for reference.

e. Subgroup 4 (C_{IN} and $C_{I/O}$ measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 15 devices with no failures, and all input and output terminals tested.

(1) The following shall apply to device class N only. Sample size is five devices with no failures. For C_{IN} and $C_{I/O}$, a device manufacturer may qualify devices by functional groups. A specific functional group shall be composed of function types, that by design, will yield the same capacitance values when tested in accordance with table I herein. The device manufacturer shall set a functional group limit for the C_{IN} and $C_{I/O}$ tests. The device manufacturer may then test one device function from a functional group to the limits and conditions specified herein. All other device functions in that particular functional group shall be guaranteed, if not tested, to the limits and conditions specified in table I herein. The device manufacturer shall submit to DSCC-VA the device functions listed in each functional group and the test results for each device tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes N, Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-PRF-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes N, Q, and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.5 Delta measurements for device class V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes N, Q, and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-EC, telephone (614) 692-0525.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-5000.

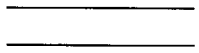
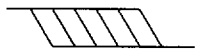
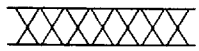
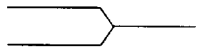
6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535, MIL-HDBK-1331, and as follows.

Pin name	I/O	Description
A0-A35	I/O	Port-A data. 36-bit bidirectional data port for side A.
$\overline{AEA}$	O	Port-A almost empty flag. Programmable flag synchronized to CLKA. It is low when the number of 36-bit words in FIFO2 is less than or equal to the value in the offset register (X).
$\overline{AEB}$	O	Port-B almost empty flag. Programmable flag synchronized to CLKB. It is low when the number of 36-bit words in FIFO1 is less than or equal to the value in the offset register (X).
$\overline{AFA}$	O	Port-A almost-full flag. Programmable flag synchronized to CLKA. It is low when the number of 36-bit locations in FIFO1 is less than or equal to the value in the offset register (X).
$\overline{AFB}$	O	Port-B almost-full flag. Programmable flag synchronized to CLKB. It is low when the number of 36-bit locations in FIFO2 is less than or equal to the value in the offset register (X).
B0-B35	I/O	Port-B data. 36-bit bidirectional data port for side B.
BE	I	Big-endian select. Selects the bytes on port B used during byte or word data transfer. A low on BE selects the most significant bytes on B0-B35 for use, and a high selects the least significant bytes.
CLKA	I	Port-A clock. CLKA is a continuous clock that synchronizes all data transfers through port A and can be asynchronous or coincident to CLKB. EFB, FFB, AFB, and AEB, are synchronous to the low-to-high transition of CLKA.
CLKB	I	Port-B clock. CLKB is a continuous clock that synchronizes all data transfers through port B and can be asynchronous or coincident to CLKA. Port-B byte swapping and data port sizing operations are also synchronous to the low-to-high transition of CLKB. EFA, FFA, AFA, and AEA, are synchronous to the low-to-high transition of CLKB.
$\overline{CSA}$	I	Port-A chip select. $\overline{CSA}$ must be low to enable a low-to-high transition of CLKA to read or write data on port A. The A0-A35 outputs are in the high-impedance state when $\overline{CSA}$ is high.
$\overline{CSB}$	I	Port-B chip select. $\overline{CSB}$ must be low to enable a low-to-high transition of CLKB to read or write data on port B. The B0-B35 outputs are in the high-impedance state when $\overline{CSB}$ is high.
EFA	O	Port-A empty flag. EFA is synchronized to the low-to-high transition of CLKA. When EFA is low, FIFO2 is empty and reads from its memory are disabled. Data can be read from FIFO2 to the output register when EFA is high. EFA is forced low when the device is reset and is set high by the second low-to-high transition of CLKA after data is loaded into empty FIFO2 memory.
EFB	O	Port-B empty flag. EFB is synchronized to the low-to-high transition of CLKB. When EFB is low, FIFO1 is empty and reads from its memory are disabled. Data can be read from FIFO2 to the output register when EFB is high. EFB is forced low when the device is reset and is set high by the second low-to-high transition of CLKB after data is loaded into empty FIFO1 memory.
ENA	I	Port-A enable. ENA must be high to enable a low-to-high transition of CLKA to read or write data on port A.
ENB	I	Port-B enable. ENB must be high to enable a low-to-high transition of CLKB to read or write data on port B.
FFA	O	Port-A full flag. FFA is synchronized to the low-to-high transition of CLKA. When FFA is low, FIFO1 is full and writes to its memory are disabled. FFA is forced low when the device is reset and is set high by the second low-to-high transition of CLKA after reset.
FFB	O	Port-B full flag. FFB is synchronized to the low-to-high transition of CLKB. When FFB is low, FIFO2 is full and writes to its memory are disabled. FFB is forced low when the device is reset and is set high by the second low-to-high transition of CLKB after reset.
FS1,FS0	I	Flag offset selects. The low-to-high transition of RST latches the values of FS0 and FS1, which selects one of four preset values for the almost-empty flag and the almost-full flag offset.

Pin name	I/O	Description
MBA	I	Port-A mailbox select. A high level on MBA chooses a mailbox register for a port-A read or write operation. When the A0-A35 outputs are active, a high level on MBA selects data from the mail2 register for output and low level selects FIFO2 output register data for output.
$\overline{MBF1}$	O	Mail1 register flag. $\overline{MBF1}$ is set low by the low-to-high transition of CLKA that writes data to the mail1 register. Writes to the mail1 register are inhibited while $\overline{MBF1}$ is low. $\overline{MBF1}$ is set high by a low-to-high transition of CLKB when a port-B read is selected and both SIZ1 and SIZ0 are set high. $\overline{MBF1}$ is set high by a reset.
$\overline{MBF2}$	O	Mail2 register flag. $\overline{MBF2}$ is set low by the low-to-high transition of CLKB that writes data to the mail2 register. Writes to the mail2 register are inhibited while $\overline{MBF2}$ is low. $\overline{MBF2}$ is set high by a low-to-high transition of CLKA when a port-A read is selected and MBA is high. $\overline{MBF2}$ is set high by a reset.
ODD/EVEN	I	Odd/even parity select. Odd parity is checked on each port when ODD/EVEN is high, and even parity is checked when ODD/EVEN is low. ODD/EVEN also the type of parity generated for each port if parity generation is enabled for a read operation.
PEFA	O	Port-A parity error flag. When any byte applied to terminals A0-A35 fails parity, PEFA is low. Bytes are organized as A0-A8, A9-A17, A18-A26, and A27-A35, with the most significant bit of each byte serving as the parity bit. The type of parity checked is determined by the state of the ODD/EVEN input. The parity trees used to check the A0-A35 inputs are shared by the mail2 register to generate parity if parity generation is selected by PGA. Therefore, if a mail2 read with parity generation is setup by having W/RA low, MBA high, and PGA high, the PEFA flag is forced high regardless of the state of the A0-A35 inputs.
PEFB	O	Port-B parity error flag. When any byte applied to terminals B0-B35 fails parity, PEFB is low. Bytes are organized as B0-B8, B9-B17, B18-B26, and B27-B35, with the most significant bit of each byte serving as the parity bit. A byte is valid when it is used by the bus size selected for port B. The type of parity checked is determined by the state of the ODD/EVEN input. The parity trees used to check the B0-B35 inputs are shared by the mail1 register to generate parity if parity generation is selected by PGB. Therefore, if a mail1 read with parity generation is setup by having W/RB low, SIZ1, SIZ0, and PGB high, the PEFB flag is forced high regardless of the state of the B0-B35 inputs.
PGA	I	Port-A parity generation. Parity is generated for data reads from port A when PGA is high. The type of parity generated is selected by the state of the ODD/EVEN input. Bytes are organized as A0-A8, A9-A17, A18-A26, and A27-A35. The generated parity bits are output in the most significant bit of each byte.
PGB	I	Port-B parity generation. Parity is generated for data reads from port B when PGB is high. The type of parity generated is selected by the state of the ODD/EVEN input. Bytes are organized as B0-B8, B9-B17, B18-B26, and B27-B35 . The generated parity bits are output in the most significant bit of each byte.
$\overline{RST}$	I	Reset. To reset the device, four low-to-high transitions of CLKA and four low-to-high transitions of CLKB must occur while $\overline{RST}$ is low. This sets the AFA, AFB, $\overline{MBF1}$, and $\overline{MBF2}$ flags high and the EFA, EFB, AEA, AEB, FFA, and FFB flags low. The low-to-high transition of $\overline{RST}$ latches the status of FS0 and FS1 inputs to select almost-full flag and almost-empty flag offsets.
SIZ0, SIZ1	I	Port-B bus size selects. A low-to-high transition of CLKB latches the states of SIZ0, SIZ1, and BE, and the following low-to-high transition of CLKB implements the latched states as a port-B bus size. Port-B bus sizes can be long word, word, or byte. A high on both SIZ0 and SIZ1 accesses the mailbox registers for a port-B 36-bit write or read.
SW0, SW1	I	Port-B byte swap selects. At the beginning of each long word transfer, one of four modes of byte-order swapping is selected by SW0 and SW1. The four modes are no swap, byte swap, word swap, and byte-word swap. Byte order swapping is possible with any bus-size selection.
W/RA	I	Port-A write/read select. A high on W/RA selects a write operation and a low selects a read operation on port A for a low-to-high transition of CLKA. The A0-A35 outputs are in the high-impedance state when W/RA is high.
$\overline{W}$/RB	I	Port-B write/read select. A high on W/$\overline{RB}$ selects a write operation and a low selects a read operation on port B for a low-to-high transition of CLKB. The B0-B35 outputs are in the high-impedance state when W/$\overline{RB}$ is low.

6.5.1 Timing limits. The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. For example, address setup time would be shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. For example, the access time would be shown as a maximum since the device never provides data later than that time.

6.5.2 Waveforms.

Waveform symbol	Input	Output
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
		HIGH IMPEDANCE

6.6 Sources of supply.

6.6.1 Sources of supply for device classes N, Q, and V. Sources of supply for device classes N, Q, and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 97-12-04

Approved sources of supply for SMD 5962-95609 are listed below for immediate acquisition only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revisions of MIL-HDBK-103 and QML-38535 .

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9560901NXD	01295	ABT3614PCB
5962-9560901QYA	01295	SNJ54ABT3614HFP

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for the part. If the desired lead finish is not listed, contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments Incorporated 13500 N. Central Expressway P.O. Box 655303 Dallas, TX 75265 Point of contact: I-20 at FM 1788 Midland, TX 79711-0448

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in thisinformation bulletin.