HIGH PERFORMANCE V53C261	10	12
Max. RAS Access Time, (t_{RAC})	100 ns	120 ns
Max Column Address Time, (t_{CAA})	45 ns	55 ns
Min. Fast Page Mode Cycle Time, (t_{PC})	60 ns	70 ns
Min. Read/Write Cycle Time, (t_{RC})	175 ns	205 ns
Min. Serial Port Cycle Time, (t_{SCC})	35 ns	40 ns

Features

- Low power dissipation for V53C261-12
  - RAM Port operating alone - 50 mA
  - SAM Port operating alone - 35 mA
  - RAM/SAM operating together - 85 mA
- Low CMOS standby current - 6 mA
- Fast Page Mode access, $\overline{RAS}$-only refresh, and $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- Bi-directional data transfer between RAM and SAM with Turbomode™ real-time operation.
- Bit-masked Write function on RAM port for additional flexibility.
- 256 Refresh cycles/4 ms.
- Standard packages are 24 pin 400 mil Plastic DIP and 24 pin ZIP.

Description

The Vitelic V53C261 is a high speed 65,536 x 4 bit multiport CMOS dynamic memory. The two ports, random access and serial access, are configured to offer optimum flexibility in graphics and other systems that require an interface between a processor and a high speed serial data channel such as a CRT or graphics display device.

The organization of the random access port of the V53C261 is exactly like that of the V53C464, a 64K x 4 CMOS DRAM. Additional functions such as transfer between RAM and SAM utilize otherwise unused states of the $\overline{CAS}$, $\overline{DT}/\overline{OE}$, $\overline{WB}/\overline{WE}$ and $\overline{SE}$ signals sampled at the falling edge of $\overline{RAS}$ at the beginning of a cycle.

The Serial Access Memory (SAM) is organized as 256 x 4 bits that can be read or written at high speed. The contents of the SAM can be loaded into RAM, and the contents of a selected RAM row (256 x 4) can be loaded into SAM. Except when transferring data between one another, the SAM and RAM operate in an asynchronous manner. The transfer from RAM to SAM or SAM to RAM also refreshes the transferred row in the RAM.

In a RAM to SAM load cycle, 8 bits are needed to specify which of the 256 rows is to be transferred. The state of the address lines at the falling edge of $\overline{CAS}$ is used to specify the starting point in the SAM where data is to be written or read. The static mechanization of the SAM (allowed by CMOS) does not require refreshing. The first access to SAM, either read or write, will be to the location specified at $\overline{CAS}$ time in the previous cycle, and subsequent accesses will continue in an increasing address direction, modulo 256.

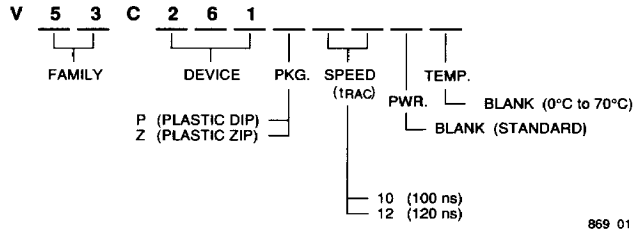
The V53C261 is processed utilizing Vitelic's VICMOS technology. This advanced CMOS processing allows memory devices to be fabricated with lower operating current and higher performance than comparable NMOS designs. All I/O signals are TTL compatible. Input and I/O capacitances are significantly lowered to enhance system performance.

Device Usage Chart

Operating Temperature Range	Package Outline		Access Time (ns)		Power	Temperature Mark
	P	Z	100	120	Std.	
0°C to 70 °C	•	•	•	•	•	Blank

V53C261 Rev. 02 June 1990

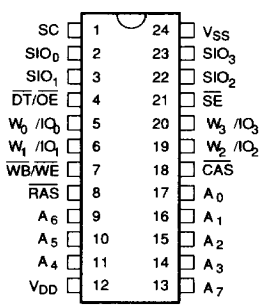
Description	Pkg.	Pin Count
Plastic DIP	P	24
Plastic ZIP	Z	24



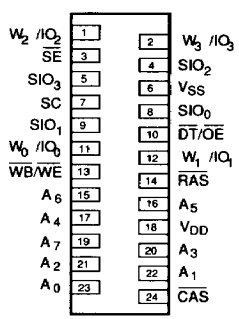
869 01

869 01

24 Lead Plastic DIP PIN CONFIGURATION
Top View



24 Lead Plastic ZIP PIN CONFIGURATION
Top View



869 02

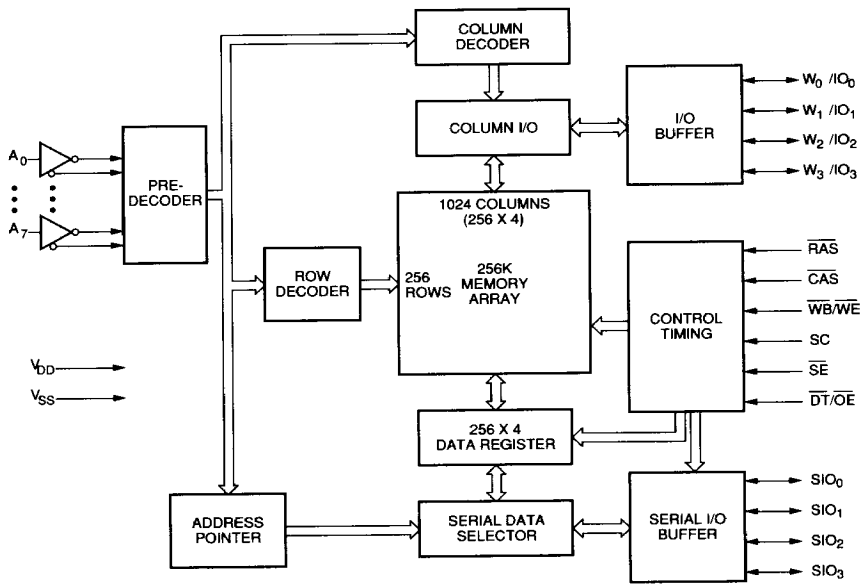
Capacitance*

T_A = 25°C, V_{DD} = 5 V ± 10%, V_{SS} = 0 V

Symbol	Parameter	Typ.	Max.	Unit
C_{IN1}	Address Input Capacitance		5	pF
C_{IN2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WB/WE}$ $\overline{SE}$, SC, $\overline{DT/OE}$ Capacitance		8	pF
C_{OUT}	I/O Capacitance		7	pF

* Note: Capacitance is sampled and not 100% tested

Block Diagram



869 03

Absolute Maximum Ratings*

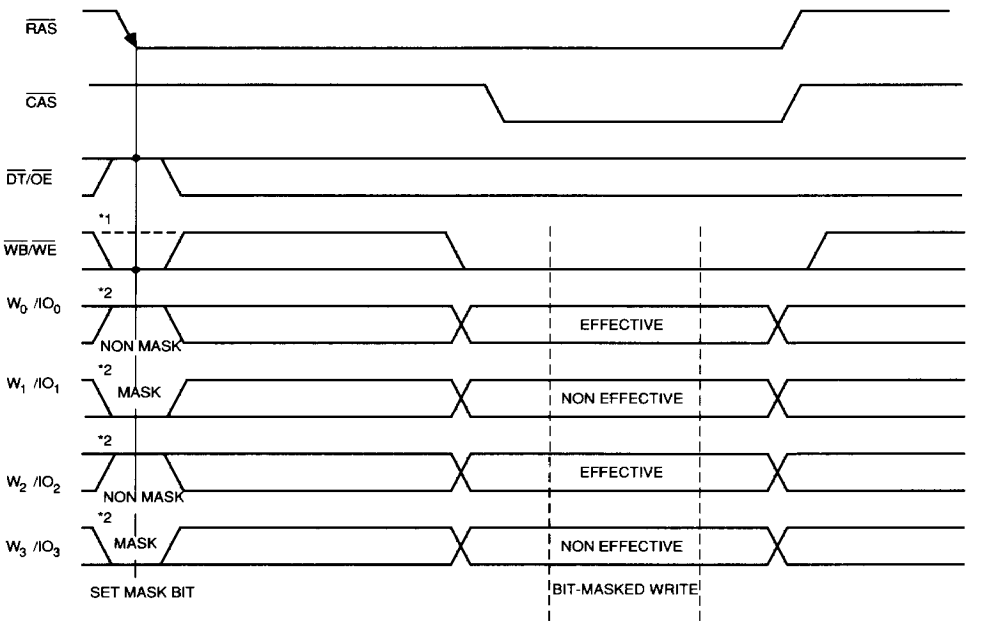
Ambient Temperature
Under Bias ..... −10°C to +80°C
Storage Temperature (plastic) .... −55°C to +125°C
Voltage on any Pin Except V_{DD}
Relative to V_{SS} ..... −1.0 V to +7.0 V
Voltage on V_{DD} relative to V_{SS} ..... −1.0 V to +7.0 V
Data Output Current ..... 50 mA
Power Dissipation ..... 1.0 W

*Note: Operation above Absolute Maximum Ratings can adversely affect device reliability.

AC Test Conditions

Input Voltage Levels ..... 0 to 3.0 V
Input Rise and Fall Times ..... 5 ns between 0.8 and 2.4 V
Input Timing Reference Levels ..... 0.8 and 2.4 V
Output Timing Reference Levels ..... 0.8 and 2.4 V
Output Load (RAM Port) ..... 2 TTL and 100 pF
Output Load (SAM Port) ..... 2 TTL and 50 pF

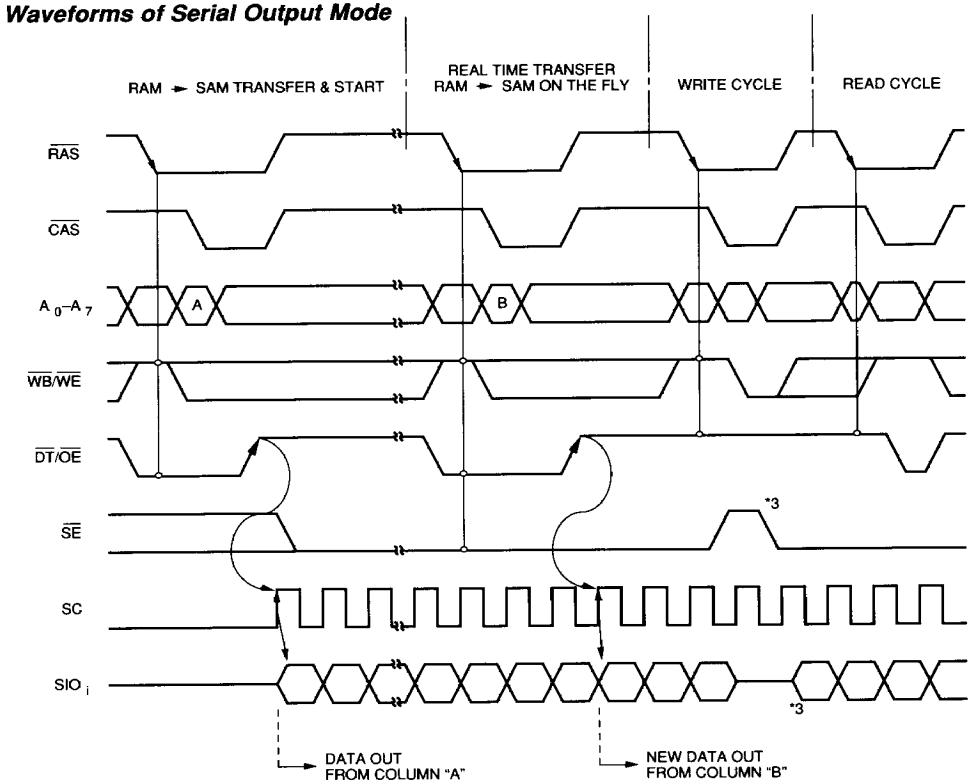
Waveforms of Bit Masked Write



*1 If WB/WE = "H" all 4 bits of data are written into RAM
*2 W0–3/IO0–3 = "H" Non masked
W0–3/IO0–3 = "L" Masked

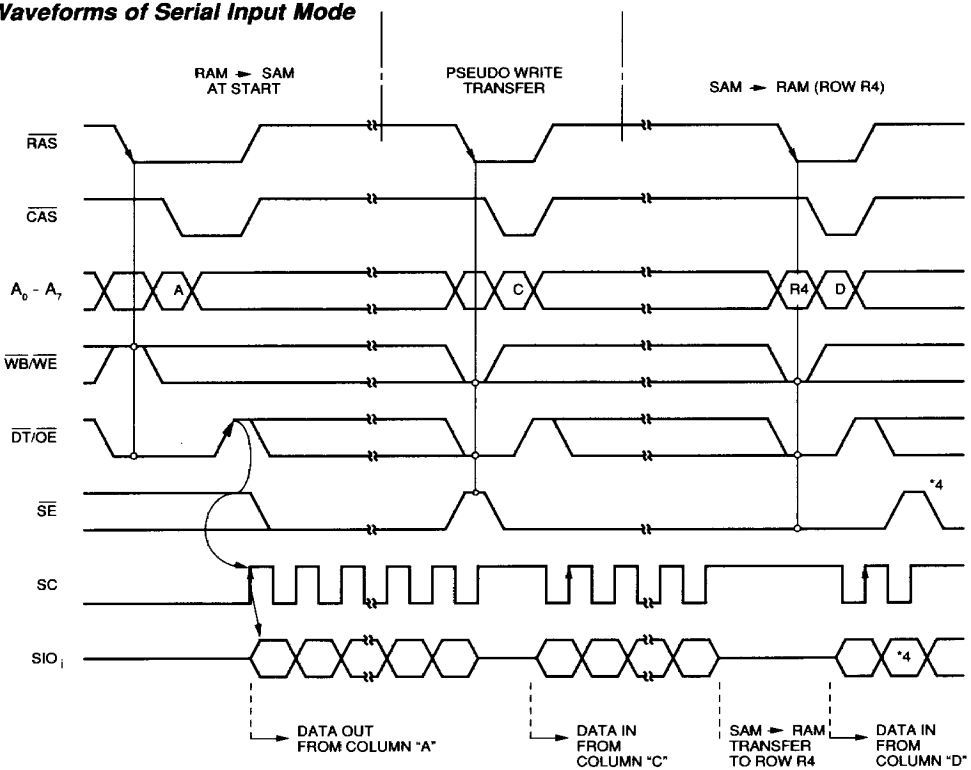
869 04

Waveforms of Serial Output Mode



*3 If $\overline{SE}$ goes to "H" level, SIO_i enters the high impedance state, but the serial data selector continues to function.

Waveforms of Serial Input Mode



*4 If $\overline{SE}$ goes to "H" level, SIO_i input data is ignored, but the serial data selector continues to function

869 06

DC Characteristics (1, 5)

T_A = 0°C to 70°C, V_{DD} = 5 V ± 10%, V_{SS} = 0 V, unless otherwise specified.

Symbol	Parameter	Access Time	V53C261 min	V53C261 max	Unit	Test Conditions	Notes
I_{LI}	Input Leakage Current (any input pin)		−10	10	µA	$V_{SS} < V_{IN} < V_{DD}$	
I_{LO}	Output Leakage Current (for High-Z State)		−10	10	µA	$V_{SS} < V_{OUT} < V_{DD}$ $\overline{RAS}$, $\overline{CAS}$ and $\overline{SE}$ at V_{IH}	
I_{DD1}	V_{DD} Supply Current	100		60	mA	$\overline{RAS}/\overline{CAS}$ Cycling, SAM port TTL Standby t_{RC} (min), SC=V_{IL}	2,3
		120		50			
I_{DD2}	V_{DD} Supply Current TTL Standby			8	mA	RAM/SAM ports TTL Standby $\overline{RAS}$, $\overline{CAS}$ at V_{IH}, I/O > V_{SS} SC=V_{IL}	
I_{DD3}	V_{DD} Supply Current $\overline{RAS}$-Only Refresh	100		60	mA	$\overline{RAS}$ Cycling, $\overline{CAS}$ at V_{IH} SAM port TTL Standby t_{RC} (min), SC=V_{IL}	2,3
		120		50			
I_{DD4}	V_{DD} SupplyCurrent Fast Page Mode Operation	100		50	mA	$\overline{RAS}$=V_{IL}, $\overline{CAS}$ Cycling SAM port TTL Standby t_{PC} (min), SC=V_{IL}	2,3
		120		40			
I_{DD5}	V_{DD} Supply Current $\overline{CAS}$-before-$\overline{RAS}$ Refresh	100		60	mA	$\overline{RAS}/\overline{CAS}$ Cycling, SAM port TTL Standby t_{RC} (min), SC=V_{IL}	2,3
		120		50			
I_{DD6}	V_{DD} SupplyCurrent RAM/SAM Transfer Mode	100		65	mA	$\overline{RAS}/\overline{CAS}$ Cycling, SAM port TTL Standby t_{RC} (min), SC=V_{IL}	2,3
		120		55			
I_{DD7}	V_{DD} SupplyCurrent Both Ports Active	100		100	mA	$\overline{RAS}/\overline{CAS}$ Cycling, SAM port Active t_{RC} (min), t_{SCC} (min)	2,3
		120		85			
I_{DD8}	V_{DD} Supply Current SAM Only Operation	100		40	mA	$\overline{RAS}/\overline{CAS}$ at V_{IH}, I/O > V_{SS} SAM port Active t_{SCC} (min)	2
		120		35			
I_{DD9}	V_{DD} Supply Current $\overline{RAS}$-Only Refresh and SAM Active	100		100	mA	$\overline{RAS}$ Cycling, $\overline{CAS}$ at V_{IH}, SAM port Active t_{RC} (min), t_{SCC} (min)	2,3
		120		85			
I_{DD10}	V_{DD} Supply Current, Fast Page Mode Operation and SAM Active	100		90	mA	$\overline{RAS}$=V_{IL}, $\overline{CAS}$ Cycling SAM port Active t_{PC} (min), t_{SCC} (min)	2,3
		120		75			

DC Characteristics (Cont'd.)

Symbol	Parameter	Access Time	V53C261 min	V53C261 max	Unit	Test Conditions	Notes
I_{DD11}	V_{DD} Supply Current $\overline{CAS}$-before-$\overline{RAS}$ Refresh and SAM Active	100		100	mA	$\overline{RAS}/\overline{CAS}$ Cycling, SAM port Active t_{RC} (min), t_{SCC} (min)	2,3
		120		85			
I_{DD12}	V_{DD} Supply Current RAM/SAM Transfer Mode and SAM Active	100		105	mA	$\overline{RAS}/\overline{CAS}$ Cycling, SAM port Active t_{RC} (min), t_{SCC} (min)	2,3
		120		90			
I_{DD13}	V_{DD} Supply Current Both Ports CMOS Standby			6	mA	$\overline{RAS}$, $\overline{CAS}$, $\overline{SE}$, $\overline{WB}/\overline{WE}$, $\overline{DT}/\overline{OE}$ >V_{DD} −0.5 V SC < 0.6 V	
V_{IL}	Input Low Voltage		−1	0.8	V		
V_{IH}	Input High Voltage		2.4	V_{DD} +1	V		
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 4.2 mA	
V_{OH}	Output High Voltage		2.4		V	I_{OH} = −2 mA	

AC Characteristics (1,4,5,6)

T_A = 0°C to 70°C, V_{DD} = 5 V ±10%, V_{SS} = 0V unless otherwise specified.

Read, Write, Read-Modify-Write and Refresh Cycles

#	Symbol	Parameter	10		12		Unit	Notes
			Min	Max	Min	Max		
	t_T	Transition Time (Rise and Fall)	3	25	3	25	ns	
	t_{RI}	Refresh Interval (256 Cycles)		4		4	ms	
1	t_{RC}	Read or Write Cycle Time	175		205		ns	
2	t_{RAS}	$\overline{RAS}$ Pulse Width	100	37K	120	37K	ns	
3	t_{RP}	$\overline{RAS}$ Precharge Time	65		75		ns	
4	t_{CSH}	$\overline{CAS}$ Hold Time	100		120		ns	
5	t_{CAS}	$\overline{CAS}$ Pulse Width	30		35		ns	
6	t_{ASR}	Row Address Setup Time	0		0		ns	
7	t_{RAH}	Row Address Hold Time	15		15		ns	
8	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10		10		ns	
9	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	25	70	25	85	ns	7
10	t_{ASC}	Column Address Setup Time	0		0		ns	
11	t_{CAH}	Column Address Hold Time	20		20		ns	
12	t_{RSH}	$\overline{RAS}$ Hold Time	30		35		ns	
13	t_{DHS}	$\overline{DT}$ High Setup Time	0		0		ns	
14	t_{DHH}	$\overline{DT}$ High Hold Time	20		20		ns	
15	t_{AR}	Column Address Hold Time from $\overline{RAS}$	70		80		ns	

AC Characteristics (Cont'd.)

Read Cycle

#	Symbol	Parameter	10		12		Unit	Notes
			Min	Max	Min	Max	Min	Max
16	t_{RAC}	$\overline{RAS}$ Access Time		100		120	ns	8,9
17	t_{CAC}	$\overline{CAS}$ Access Time		30		35	ns	9,10 11
18	t_{CAA}	Column Address Access Time		45		55	ns	9
19	t_{RCS}	Read Command Setup Time	0		0		ns	
20	t_{RRH}	Read Command Hold Time, $\overline{RAS}$-Referenced	5		10		ns	12
21	t_{RCH}	Read Command Hold Time, $\overline{CAS}$-Referenced	0		0		ns	12
22	t_{OAC}	$\overline{OE}$ Access Time		25		30	ns	9
23	t_{HZ}	$\overline{OE}$ or $\overline{CAS}$ to Output High-Z		25		30	ns	13
24	t_{LZ}	$\overline{OE}$ or $\overline{CAS}$ to Output Low-Z	0		0		ns	
25	t_{OH}	Output Hold Time From $\overline{OE}$ or $\overline{CAS}$	0		0		ns	

AC Characteristics (Cont'd.)

Write Cycle

#	Symbol	Parameter	10		12		Unit	Notes
			Min	Max	Min	Max		
26	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	30		35		ns	
27	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	30		35		ns	
28	t_{WP}	Write Command Pulse Width	20		25		ns	
29	t_{WCS}	Write Command Setup Time	0		0		ns	14
30	t_{WCH}	Write Command Hold Time	20		25		ns	
31	t_{DS}	Data In Setup Time	0		0		ns	
32	t_{DH}	Data In Hold Time	20		25		ns	
33	t_{WBS}	Write Mask Setup Time	0		0		ns	
34	t_{WBH}	Write Mask Hold Time	20		20		ns	
35	t_{WS}	Write Mask Select Setup Time	0		0		ns	
36	t_{WH}	Write Mask Select Hold Time	20		20		ns	
37	t_{OEH}	$\overline{OE}$ Hold Time Referenced to $\overline{WE}$	10		15		ns	
38	t_{WCR}	Write Hold Time from $\overline{RAS}$	80		95		ns	
39	t_{DHR}	Data Hold Time from $\overline{RAS}$	80		95		ns	

AC Characteristics (Cont'd.)

Read-Modify-Write Cycle

#	Symbol	Parameter	10		12		Unit	Notes
			Min	Max	Min	Max		
40	t_{RWC}	Read-Modify-Write Cycle Time	245		285		ns	
41	t_{RRW}	RMW Cycle $\overline{RAS}$ Pulse Width	170	37K	200	37K	ns	
42	t_{CRW}	RMW Cycle $\overline{CAS}$ Pulse Width	100		115		ns	
43	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay	135		160		ns	14
44	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay	65		75		ns	14
45	t_{AWD}	Column Address to $\overline{WE}$ Delay	80		95		ns	
46	t_{OED}	$\overline{OE}$ to Data In Delay Time	25		30		ns	

Fast Page Mode Operation

#	Symbol	Parameter	10		12		Unit	Notes
			Min	Max	Min	Max		
47	t_{PC}	Page Mode Cycle Time	60		70		ns	
48	t_{CP}	$\overline{CAS}$ Precharge Time	20		25		ns	
49	t_{CAP}	Access Time from Column Precharge		55		65	ns	15

#	Symbol	Parameter	10		12		Unit	Notes
			Min	Max	Min	Max		
50	t_{CSR}	$\overline{CAS}$-before-$\overline{RAS}$ Refresh Setup Time	10		10		ns	
51	t_{CHR}	$\overline{CAS}$-before-$\overline{RAS}$ Refresh Hold Time	25		25		ns	
52	t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time	0		0		ns	

AC Characteristics (Cont'd.)

Read/Write, Pseudo Write Transfer and Serial Read/Write Cycle

#	Symbol	Parameter	10		12		Unit	Notes
			Min	Max	Min	Max		
53	t_{SCC}	Serial Clock Cycle Time	35		40		ns	
54	t_{SCL}	SC Precharge Time	10		10		ns	
55	t_{SOO}	$\overline{SE}$ to Serial Out Setup Time	0		5		ns	
56	t_{SOH}	Serial Out Hold after SC High	0		5		ns	
57	t_{SCA}	Serial Output Access Time from SC		30		35	ns	16
58	t_{SOA}	Serial Output Access Time from $\overline{SE}$		25		30	ns	16
59	t_{SOZ}	Serial Output Disable Time from $\overline{SE}$ High		20		25	ns	13
60	t_{SCH}	SC Pulse Width	15		15		ns	
61	t_{SOE}	$\overline{SE}$ Pulse Width	10		10		ns	
62	t_{SOP}	$\overline{SE}$ Precharge Time	10		10		ns	
63	t_{DLS}	Transfer Command to $\overline{RAS}$ Setup Time	0		0		ns	
64	t_{RDH}	Transfer Command to $\overline{RAS}$ Hold Time	75		90		ns	
65	t_{CDH}	Transfer Command to $\overline{CAS}$ Hold Time	25		30		ns	
66	t_{SDD}	SC to Transfer Command Lead Time	15		20		ns	
67	t_{SDH}	SC Hold Time after $\overline{DT}$ High	10		10		ns	
68	t_{SZS}	Serial Data Input to $\overline{DT}$ High Delay Time		0		0	ns	
69	t_{DTP}	$\overline{DT}$ Precharge Time	25		30		ns	
70	t_{TRP}	$\overline{DT}$ to $\overline{RAS}$ Precharge Time	75		85		ns	
71	t_{SWS}	Serial Write Enable Setup Time	10		10		ns	
72	t_{SWH}	Serial Write Enable Hold Time	15		20		ns	
73	t_{SWIS}	Serial Write Disable Setup Time	10		10		ns	
74	t_{SWIH}	Serial Write Disable Hold Time	15		20		ns	
75	t_{SRS}	SC to $\overline{RAS}$ Setup Time	20		20		ns	

AC Characteristics (Cont'd.)

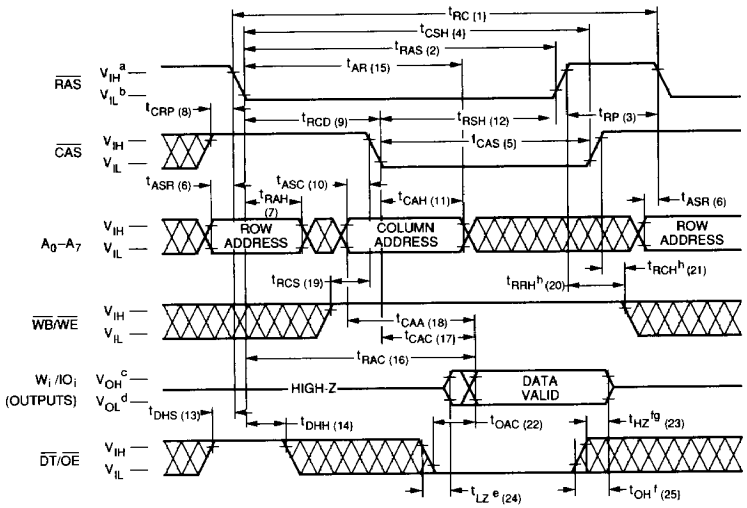
Read/Write, Pseudo Write Transfer and Serial Read/Write Cycle

#	Symbol	Parameter	10		12		Unit	Notes
			Min	Max	Min	Max		
76	t_{ES}	Pseudo Transfer Command ($\overline{SE}$) to $\overline{RAS}$ Setup Time	0		0		ns	
77	t_{EH}	Pseudo Transfer Command ($\overline{SE}$) to $\overline{RAS}$ Hold Time	20		20		ns	
78	t_{SIS}	Serial Data In Setup Time	0		0		ns	
79	t_{SIH}	Serial Data In Hold Time	10		10		ns	
80	t_{SDS}	SC to $\overline{DT}$ High Setup Time	0		0		ns	
81	t_{SCR}	SC to $\overline{RAS}$ Precharge Setup Time	0		0		ns	

Notes:

1. All voltages are referenced to V_{SS}.
2. I_{DD} is dependent on output loading when the device output is enabled. I_{DD} (max.) is measured with all outputs open.
3. I_{DD} is dependent on the number of address transitions while $\overline{CAS}$ is at V_{IH}. Specified I_{DD} (max.) is measured with a maximum of two transitions per address input per random cycle and one transition per address cycle in Fast Page Mode.
4. V_{IH} (min.) and V_{IL} (max.) are the reference levels for measuring input signal timing. Transition times are measured between V_{IH} (min.) and V_{IL} (max.).
5. An initial pause of 200 µs and 8 $\overline{RAS}$-containing cycles are required when exiting an extended period of bias without clocks or upon Power Up. An extended period of time without clocks is defined as one that exceeds the specified Refresh Interval.
6. AC characteristics assume t_T = 5 ns. All AC measurements are made with a load equivalent to two TTL inputs and either 50 or 100 pF in parallel. V_{IL} (min.) > V_{SS} and V_{IH} (max.) < V_{DD}.
7. t_{RCD} (max.) is for reference only. t_{RCD} (min.) = t_{RAH} (min.) + $2t_T$ + t_{ASC} (min.)
8. Assumes that $t_{RCD} < t_{RCD}$ (max.). If $t_{RCD} > t_{RCD}$ (max.), t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD} (max.).
9. Measured with a load equivalent to 2 TTL loads and 100 pF in parallel.
10. Assumes $t_{RCD} > t_{RCD}$ (max.).
11. If $t_{ASC} < (t_{CAA}$ (max.) - t_{CAC} (max.) - tT), access time is defined by t_{CAA} rather than t_{CAC}.
12. Either t_{RCH} or t_{RRH} must be satisfied.
13. An output disable time defines the time when the output reaches the open-circuit condition and is not referenced to output voltage levels.
14. t_{WCS}, t_{RWD} and t_{CWD} are specified for reference only. If $t_{WCS} > t_{WCS}$ (min.), the cycle is a $\overline{CAS}$-controlled write cycle (Early Write), and the $\overline{IO}$ pins will be at High-Z during the entire cycle. If $t_{CWD} > t_{CWD}$(min.), and $t_{RWD} > t_{RWD}$(min.), the cycle is a Read-Modify-Write cycle, and the $\overline{IO}$ pins will reflect the data read from the addressed location. If any of the above conditions is not satisfied, the condition of the Data Out pins will be indeterminate.
15. Access time is determined by the longest of t_{CAA}, t_{CAC} and t_{CAP}.
16. Measured with a load equivalent to 2 TTL loads and 50 pF in parallel.

Waveforms of Read Cycle



869 07

NOTES:

a., b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.

c., d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT}.

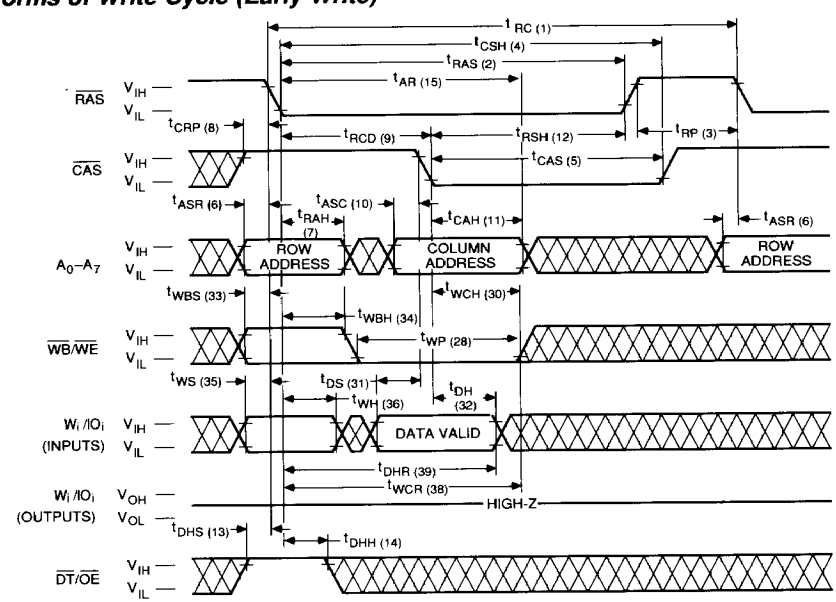
e. t_{LZ} is referenced to the later of $\overline{CAS}$ and $\overline{OE}$ low transition.

f. t_{HZ} and t_{OH} are referenced to the earlier of $\overline{CAS}$ and $\overline{OE}$ high transition.

g. Transition is measured +500 mV from steady state voltage with specified three state load (5 pF and a 380 Ohm Thevenin equivalent).

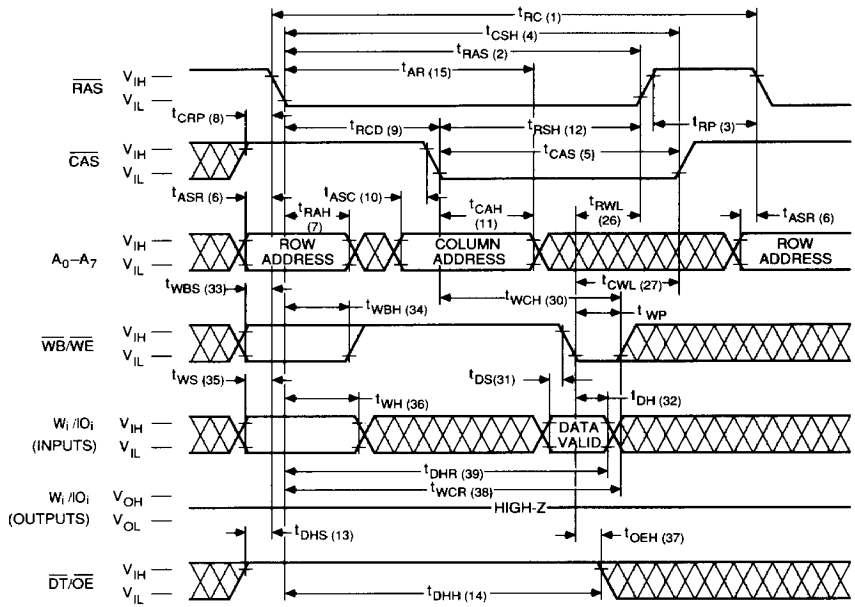
h. Either t_{RCH} or t_{RRH} must be satisfied.

Waveforms of Write Cycle (Early Write)



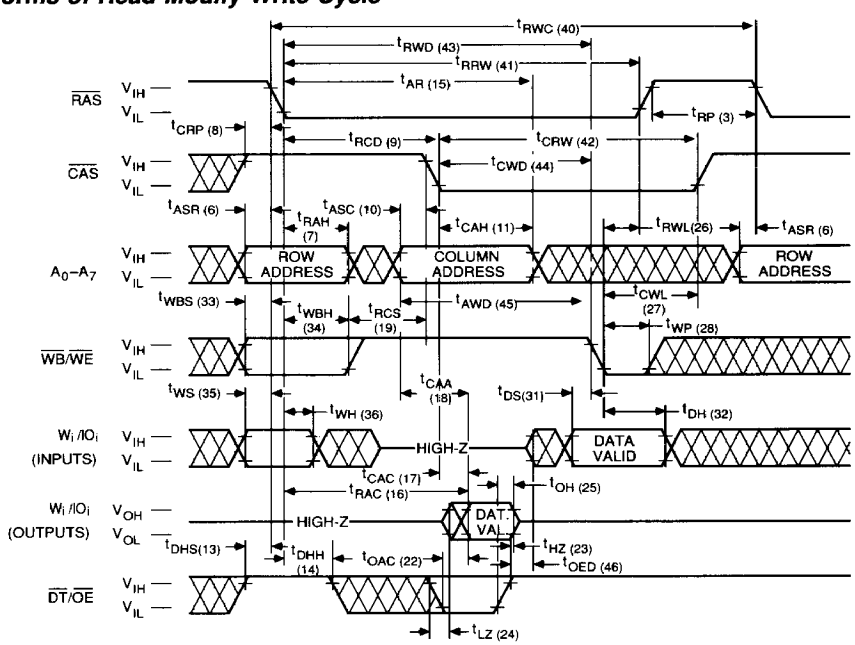
869 08

Waveforms of Write Cycle (Delayed Write)



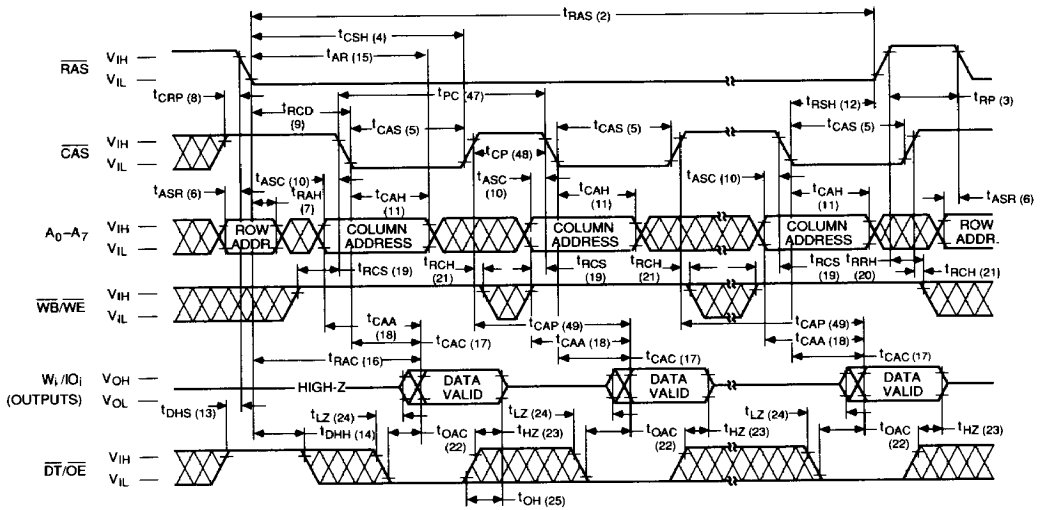
869 09

Waveforms of Read-Modify-Write Cycle



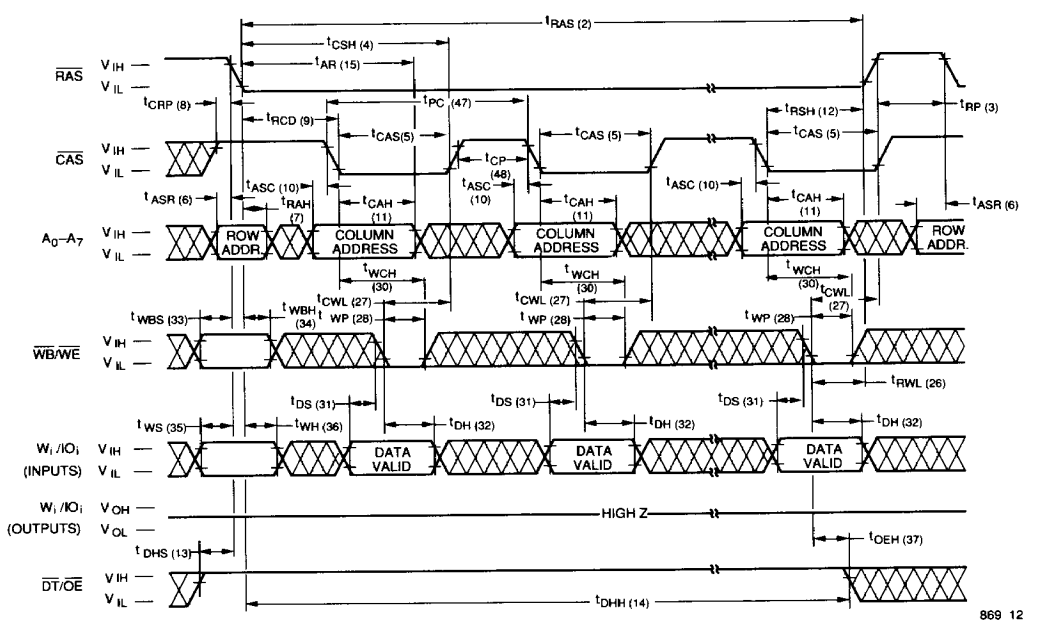
869 10

Waveforms of Fast Page Read Cycle



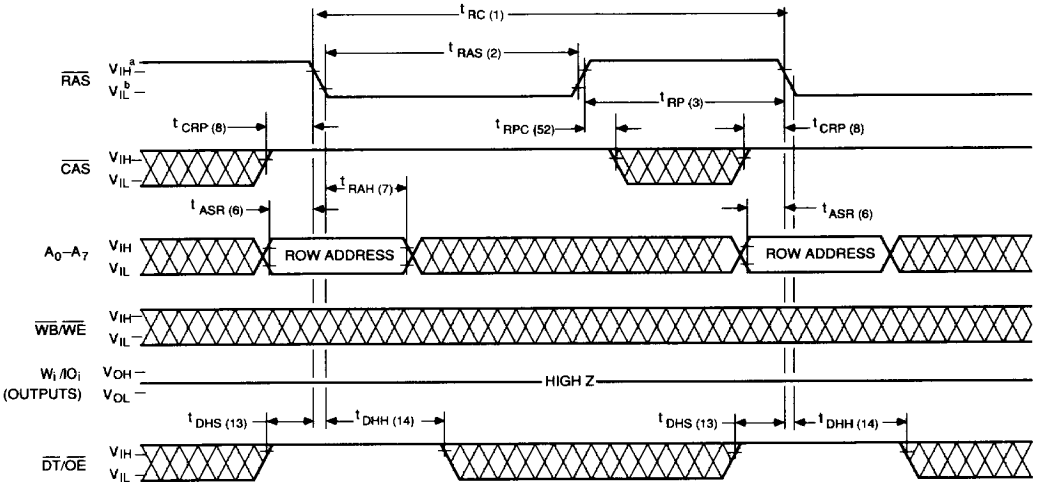
869 11

Waveforms of Fast Page Mode Write Cycle



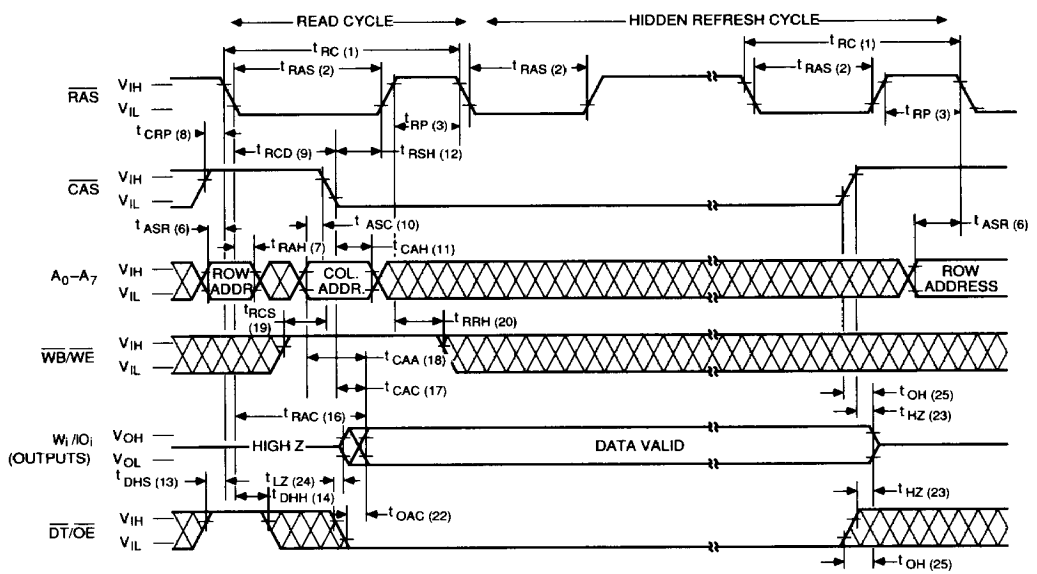
869 12

Waveforms of $\overline{RAS}$-Only Refresh Cycle



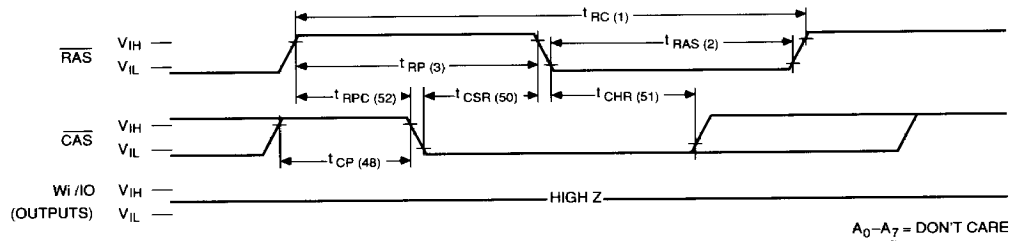
869 13

Waveforms of Hidden Refresh Cycle



869 14

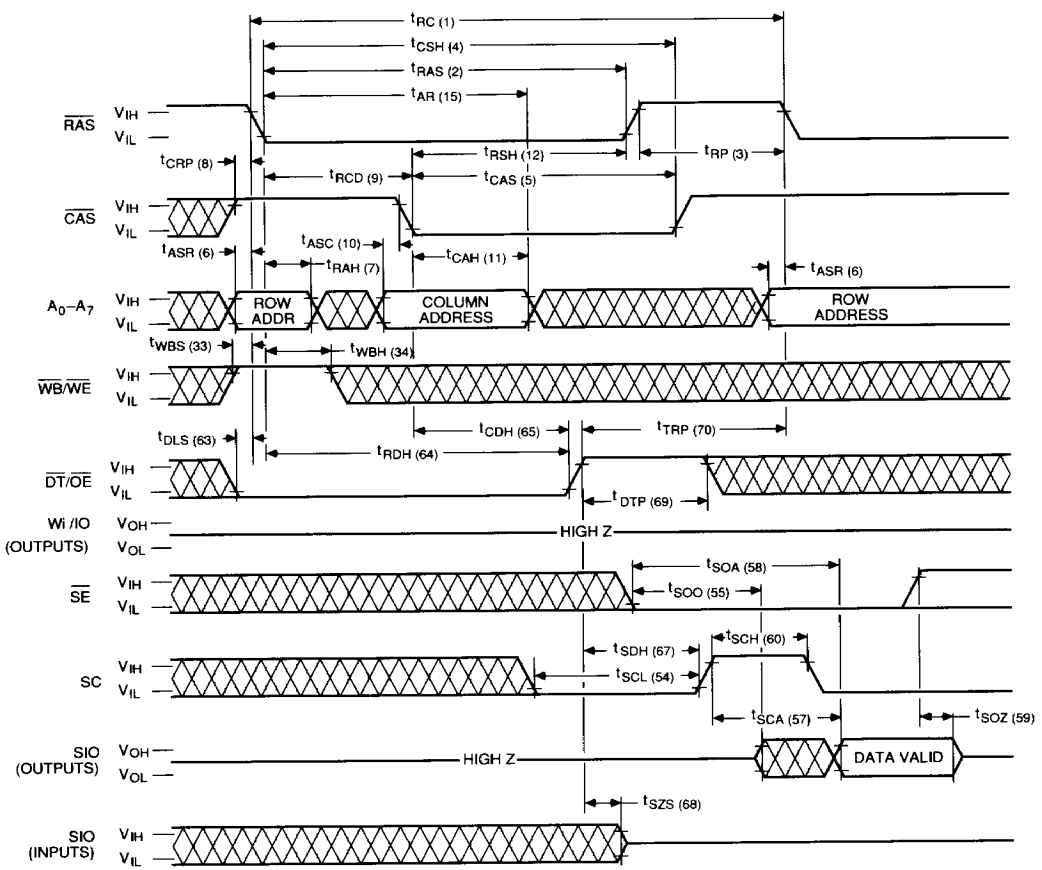
Waveforms of $\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle



A_0–A_7 = DON'T CARE
$\overline{DT}/\overline{OE}$ = DON'T CARE
$\overline{WB}/\overline{WE}$ = DON'T CARE

869 14a

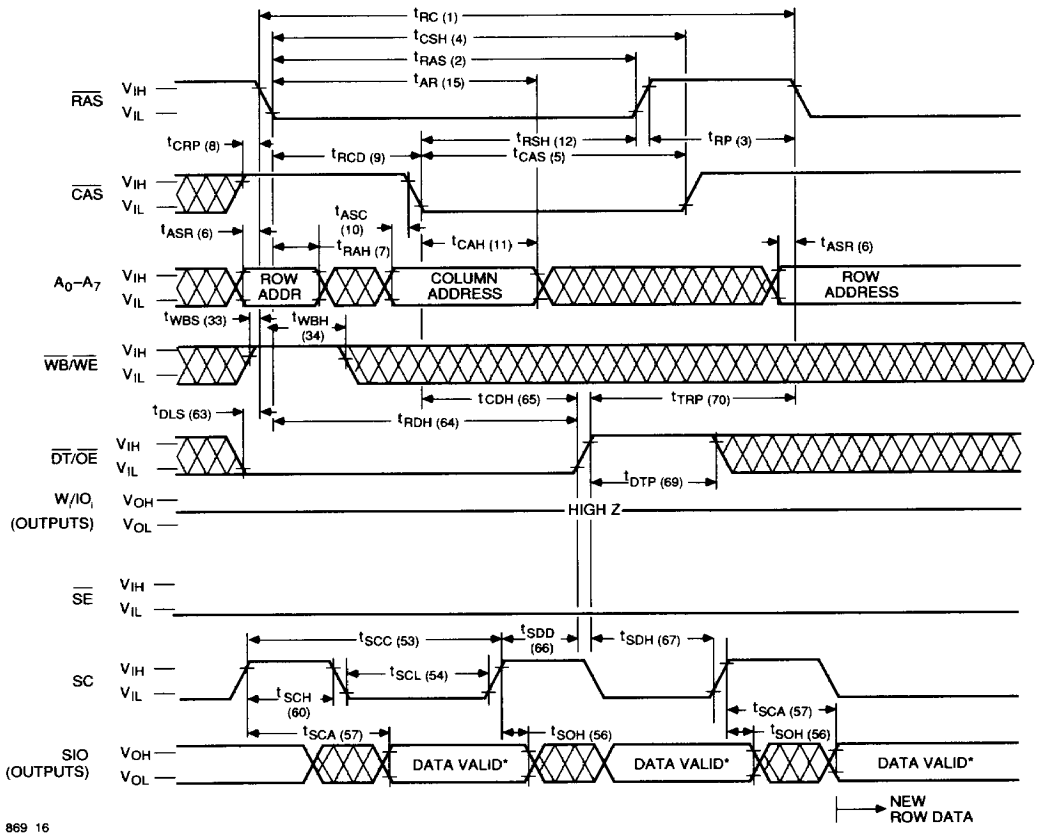
Waveforms of Read Transfer Cycle (RAM-SAM) Serial Read Setup*



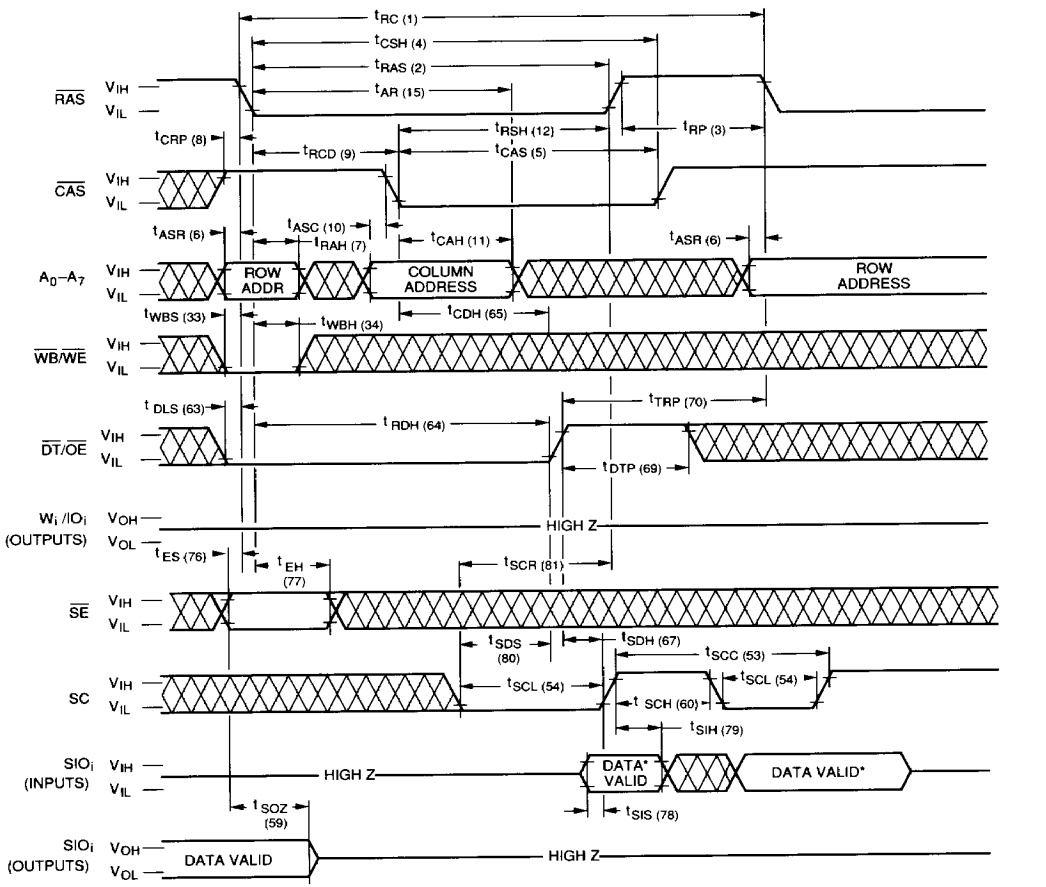
869 15

NOTE: * IN THE CASE THAT THE PREVIOUS TRANSFER IS WRITE TRANSFER.

Waveforms of Read Transfer Cycle (RAM-SAM) (Turbomode™)



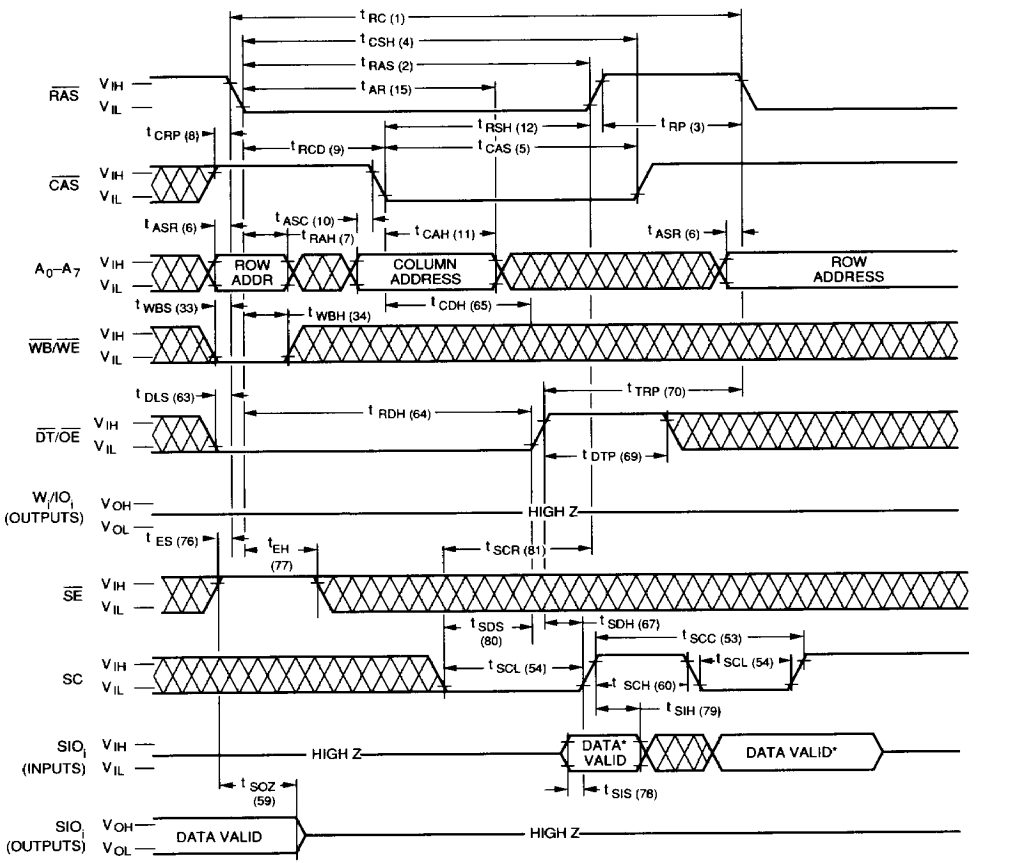
Waveforms of Write Transfer Cycle (SAM-RAM)



NOTE* IF $\overline{SE}$ IS "H" LEVEL, THE SERIAL INPUT DATA ARE NOT WRITTEN INTO THE DATA REGISTER, BUT THE SERIAL DATA SELECTOR CONTINUES TO FUNCTION.

869 17a

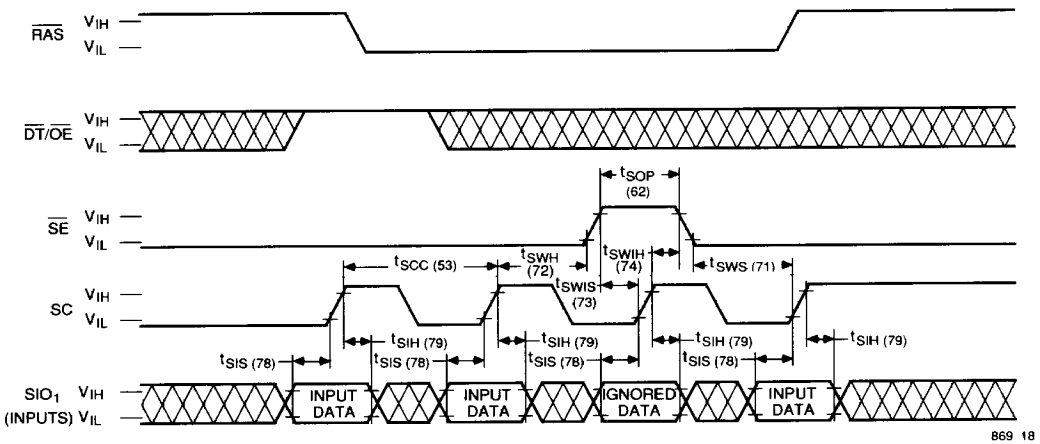
Waveforms of Pseudo Write Transfer Cycle Serial Write Setup



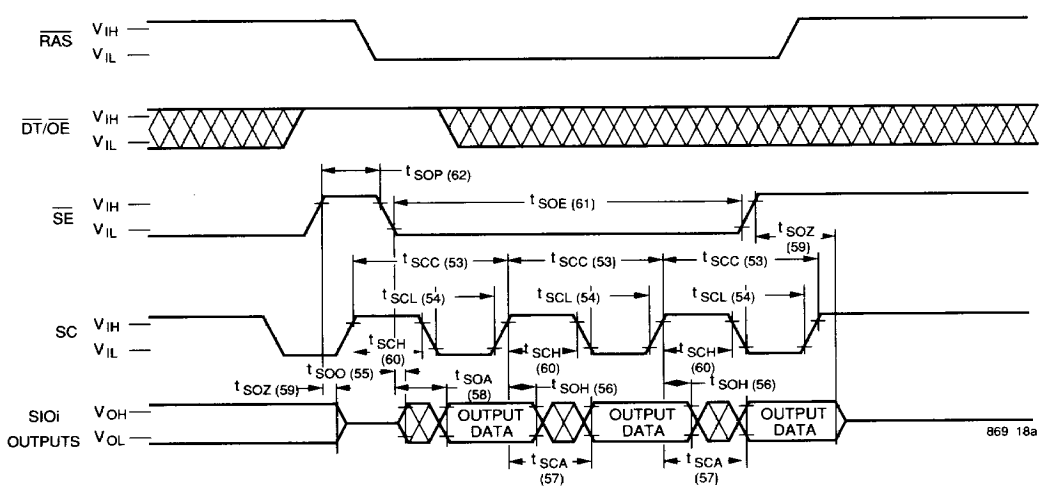
NOTE* IF $\overline{SE}$ IS "H" LEVEL, THE SERIAL INPUT DATA ARE NOT WRITTEN INTO THE DATA REGISTER, BUT THE SERIAL DATA SELECTOR CONTINUES TO FUNCTION.

869 17

Waveforms of Serial Write Cycle



Waveforms of Serial Read Cycle



Functional Description

RAM Operation

The V53C261 is a CMOS dynamic memory with 2 ports. One port, the RAM port, operates in the same way as the V53C464—64K x 4 DRAM. The other port, the Serial Access Port (SAM), allows data to be either read from or written to the memory at very high data rates.

The V53C261 reads and writes data via the RAM port by multiplexing a 16-bit address into an 8-bit row and an 8-bit column address. The Row Address Strobe ($\overline{RAS}$) latches the row address on chip. The column address, however, flows through the internal column address buffer and is latched by the Column Address Strobe ($\overline{CAS}$) signal. Because column access time becomes primarily dependent upon a valid column address rather than the falling edge of $\overline{CAS}$, signal timing restrictions on $\overline{CAS}$ can be greatly loosened with no effect on access time.

Memory Cycle

A memory cycle is initiated by the falling edge of $\overline{RAS}$. A memory cycle may not be ended or aborted prior to fulfilling the t_{RAS} (min) timing specification once it has been started. This precaution is necessary for proper device operation and integrity. A new memory cycle may not be started until the minimum precharge time t_{RP}/t_{CP} has been satisfied.

Read Cycle

A read cycle is a memory cycle in which data are retrieved from the memory array and presented on the W_i/IO_i pins. Read cycles can take the form of single operations to a specific row and column address or page mode accesses to any of 256 column addresses within a single row.

Write Cycle

A write cycle is a memory cycle in which data supplied externally to W_i/IO_i are written into the location in memory specified by the address. Using the masked write function, any combination of W_i/IO_i lines may be written and the remainder ignored. Write cycles can take the form of single operations to a specific row and column address or page mode accesses to any of 256 column addresses within a single row.

Refresh Cycle

To retain the data in a V53C261 DRAM a refresh operation activating each of the 256 row addresses must be performed at least once every 4 ms. Any operation such as read, write, RMW, $\overline{RAS}$-only cycle, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle or transfer cycle refreshes the addressed row.

Fast Page Mode Operation

Fast Page Mode permits all 256 columns of 4-bits within a selected row of the V53C261 to be randomly accessed at a high data rate. After a normal cycle initiation, maintaining $\overline{RAS}$ low while performing successive $\overline{CAS}$ cycles retains the row address internally and eliminates the need to resupply it. The column buffer acts as a transparent latch while $\overline{CAS}$ is high and, when $\overline{CAS}$ goes low, holds the addresses applied. Because of the transparent latches, the column address "flows through" and the read access begins upon stable addresses rather than the falling $\overline{CAS}$ edge. This eliminates t_{ASC} and t_T from the critical timing path and helps to speed up access while making operation simpler.

During a Fast Page Mode operation, read, write, read-modify-write, or read-write-read cycles are possible to random addresses within a selected row. Multiple operations to the same address are permitted as well as more than 256 accesses to any combination of addresses within the selected row. The only limiting factor to the number of such Page Mode accesses is consideration of refresh timing. Following the entry cycle into Page Mode, access time is t_{CAA} or t_{CAP}-dependent. If the column address is valid before or coincident with the rising edge of $\overline{CAS}$, then t_{CAP} is the access controlling parameter. If the column address is valid after the rising edge of $\overline{CAS}$, access time is determined by t_{CAA}. In both cases, the falling edge of $\overline{CAS}$ latches the address and enables the output buffers.

With Fast Page Mode, very high sustained data rates can be achieved. The following equation can be used to calculate the data rate possible:

$$\text{Data Rate} = \frac{256}{t_{RC} + 255\, t_{PC}}$$

Mode Selection

RAM Operation to to be Performed	SAM Mode to be Entered	Control Signals (Sampled at the falling edge of $\overline{RAS}$)					$A_0 - A_7$ Sample Time	
		$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	$\overline{SE}$	W_i /IO_i	$\overline{RAS}$	$\overline{CAS}$
Read	Mode not affected	H	H	X	X	X	Row	Column Add.
Write	Mode not affected			H	X	X	Row	Column Add.
Bit Masked Write	Mode not affected			L	X	H*	Row	Column Add.
	Mode not affected			L	X	L*	Row	Column Add.
RAM → SAM Transfer	Output Mode		L	H	X	X	Row	SAM Start**
SAM → RAM Transfer	Input Mode			L	L	X	Row	SAM Start**
Pseudo Transfer	Input Mode			L	H	X	X	SAM Start**
$\overline{CAS}$-before-$\overline{RAS}$ or Hidden Refresh	Mode not affected	L	X	X	X	X	X	X

X = DON'T CARE

* The state of the W_i/IO_i lines is sampled at the falling edge of $\overline{RAS}$ to set the Write Bit Mask Register. If W_i/IO_i is high at the falling edge of $\overline{RAS}$, no masking action is taken and the corresponding data bit will be subject to change by a write operation. If W_i/IO_i is low at the falling edge of $\overline{RAS}$, the corresponding bit is masked and will not be altered by a write operation.

** The 8 address signals, $A_0 - A_7$, are used to select the RAM row address that will be affected by a transfer to or from the SAM and the starting address for a SAM read or write operation. The falling edge of $\overline{RAS}$ strobes the row address, and the falling edge of $\overline{CAS}$ strobes the SAM starting address.

Combined RAM-SAM Operation

Transfer

The transfer operation of the V53C261 allows a row (256 bits) of data to be transferred between RAM and SAM in either direction. The signals and states that control the transfer operation are specified in the Mode Selection Table.

To start a serial write operation, it is necessary to cause the SIO_0–SIO_3 pins of the SAM port to be in a high-Z state. The pseudo write transfer cycle accomplishes this purpose and must be performed any time the SAM mode is to be changed from read to write. No data transfer takes place, but addresses are set up as in any other transfer cycle. A read transfer cycle (RAM to SAM) changes the mode from write to read.

SAM Operation

General

The Serial Access Memory (SAM) of the V53C261 is organized as 256 words x 4 bits per word. It is possible to load the SAM from two sources: the RAM and the external serial I/O lines, SIO_i. SAM has two operational modes, read and write (viewed externally). Mode changes were described in the previous section.

When the SAM is in the read mode, data are first transferred from the RAM to SAM and then can be accessed serially via the SIO_i lines beginning with any SAM address. The progression of data output is from lower to higher numbered bits and addresses are modulo 256.

When the SAM is in the write mode, data are captured into the SAM using the SIO_i lines and can be written into a selected row in the RAM by a write transfer operation.

Read/Write

The SC pin is used as a 'shift clock' for the SAM port. Serial access is triggered by the rising edge of SC. When the SAM is in the write mode, the rising edge of SC causes data to be strobed into the selected cell of the SAM. In the read cycle, output data become valid after t_{SCA} from the rising edge of SC and remain valid until the next cycle. The SAM address is automatically incremented by SC.

The $\overline{SE}$ pin is used as an output/input enable pin for the SAM. It does not, however, gate the SC signal. The SAM address counter for read or write operations will continue to increment regardless of the state of $\overline{SE}$.

Turbomode Read Transfer

The V53C261 offers Turbomode real-time read transfer between RAM and SAM. By using the Turbomode feature, a continuous data stream can be generated even if the row address must be changed. No loss of timing is caused by Turbomode transfer. The data transfer from the RAM to SAM is triggered by the rising edge of $\overline{DT/OE}$ after the $\overline{RAS}$/$\overline{CAS}$ cycle has set up the data to be transferred and the start address. New row data is available for SAM output after $\overline{DT/OE}$ returns to a high state in compliance with specification parameters t_{SDD} and t_{SDH}. SC should be applied continuously and $\overline{DT/OE}$ timed from SC to achieve non-stop transfer.

Write Transfer

When the SAM has been placed into a write mode, and the required data have been captured via SIO_i, the write transfer operation will cause the content of the SAM to be written into the selected RAM row. After the write transfer cycle has been completed, more data can be written to the SAM via SIO_i.

Power-On

After application of the V_{DD} supply, an initial pause of 200 µs is required followed by a minimum of 8 initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock). Eight initialization cycles are required after extended periods of bias without clocks. An extended period of time without clocks is defined as one that exceeds the specified refresh interval. During Power-On, the V_{DD} current requirement of the V53C261 is dependent on the input levels of $\overline{RAS}$ and $\overline{CAS}$. If $\overline{RAS}$ is Low during Power-On, the device will go into an active cycle, and I_{DD} will exhibit current transients. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{DD} or be held at a valid V_{IH} during Power-On to avoid current surges.