μPB100476LL
1024 x 4-Bit
100K ECL Synchronous RAM

Preliminary Information

Description

The μPB100476LL is a very-high-speed 100K interface ECL RAM organized as 1024 words by 4 bits and designed with noninverted, open-emitter outputs and low power consumption.

The device integrates input latches, high-speed ECL RAM, output latches, and a write pulse generator. The synchronous design allows precise cycle control by use of an internal clock.

Features

- 1024-word x 4-bit organization
- 100K ECL interface
- High-speed clock cycle: 6 ns
- Latched I/O
- Self-timed write
- 28-pin ceramic package, DIP or flatpack

Ordering Information

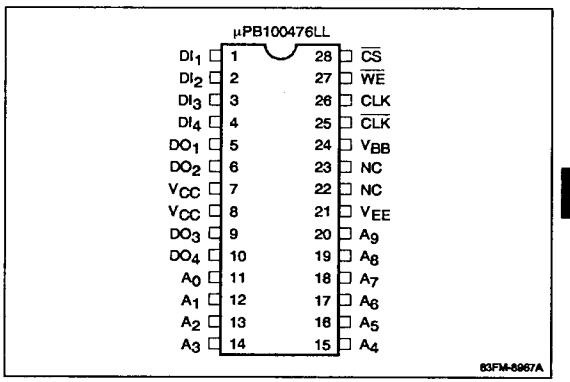
Part Number	Access Time (max)	Package
μPB100476LLDH-6	6 ns	28-pin cerdip
BH-6	6 ns	28-pin ceramic flatpack

Pin Identification

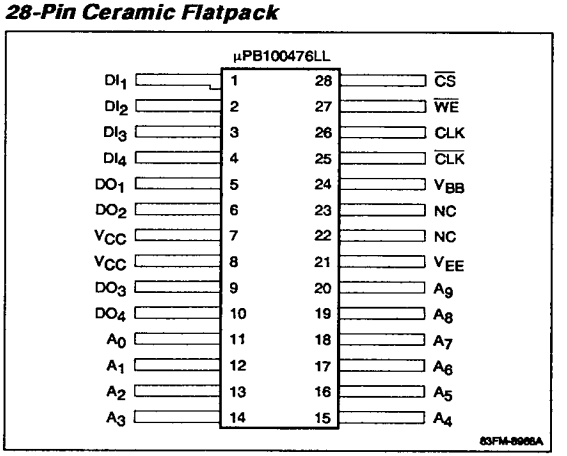
Symbol	Function
A_0 - A_9	Address inputs
DI_1 - DI_4	Data inputs
DO_1 - DO_4	Data outputs
CLK, $\overline{CLK}$	Clock inputs
$\overline{CS}$	Chip select input
$\overline{WE}$	Write enable input
V_{BB}	Reference voltage output
V_{CC}	Power supply ground (current switches and bias driver)
V_{CCA}	Power supply ground (output devices)
V_{EE}	Power supply (–5.2 volts)
NC	No connection

Pin Configurations

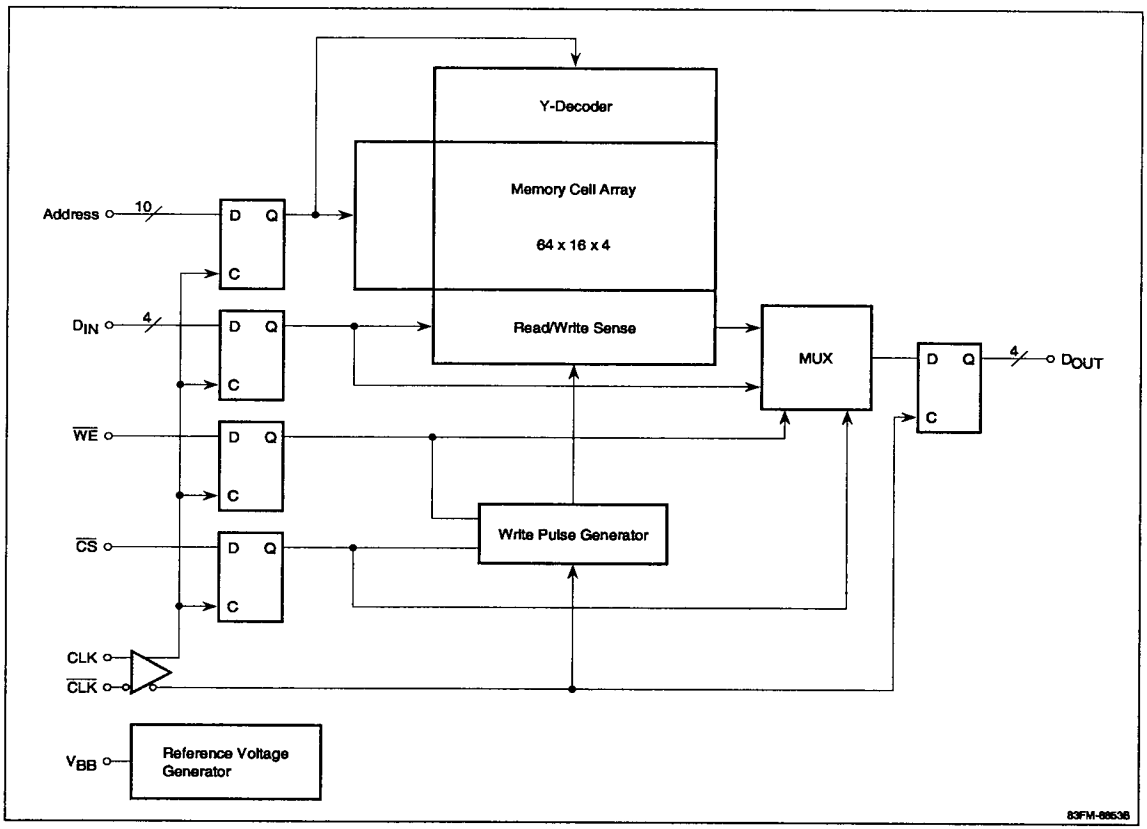
28-Pin Cerdip



28-Pin Ceramic Flatpack



Block Diagram



Absolute Maximum Ratings

Supply voltage, V_{EE} to V_{CC}	−7.0 to +0.5 V
Input voltage, V_{IN}	V_{EE} to +0.5 V
Output current, I_{OUT}	−30 to +0.1 mA
Storage temperature, T_{STG}	−65 to +150°C
Storage temperature under bias, T_{STG} (bias)	−55 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

f = 1 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_{IN}		4		pF
Output capacitance	C_{OUT}		5		pF

Truth Table

$\overline{CS}$	$\overline{WE}$	D_{IN}	Output	Mode
H	X	X	L	Not selected
L	L	L	L	Write 0
L	L	H	L	Write 1
L	H	X	D_{OUT}	Read

X = don't care.

DC Characteristics

T_A = 0 to +85°C; V_{CC} = V_{CCA} = 0 V; V_{EE} = −4.5 V; output load = 50 Ω to −2.0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	−1025		−880	mV	V_{IN} = V_{IH} max or V_{IL} min
Output voltage, low	V_{OL}	−1810		−1620	mV	V_{IN} = V_{IH} max or V_{IL} min
Output threshold voltage, high	V_{OHC}	−1035			mV	V_{IN} = V_{IH} min or V_{IL} max
Output threshold voltage, low	V_{OLC}			−1610	mV	V_{IN} = V_{IH} min or V_{IL} max
Input voltage, high	V_{IH}	−1165		−880	mV	Guaranteed input voltage high for all inputs
Input voltage, low	V_{IL}	−1810		−1475	mV	Guaranteed input voltage low for all inputs
Input current, high	I_{IH}			220	μA	V_{IN} = V_{IH} max
Input current, low	I_{IL}	0.5		170	μA	For $\overline{CS}$: V_{IN} = V_{IL} min
		−50			μA	For all others: V_{IN} = V_{IL} min
Supply current	I_{EE}	−350			mA	All inputs and outputs open
Reference voltage	V_{BB}	−1390		−1250	mV	

Notes:

(1) The device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

AC Characteristics

T_A = 0 to +85°C; V_{EE} = −4.5 V ±5%; output load = 50 Ω to −2.0 V

Parameter	Symbol	μPB100476LL-6 Min	Typ	Max	Unit	Test Conditions
Address access time	$t_{A(Add)}$			2.5	ns	t_{SA} = 0.5 ns
Clock access time	$t_{A(Clk)}$			3.3	ns	$t_{WL(Clk)}$ = 1.5 ns
$\overline{CS}$ access time	$t_{A(CS)}$			2.3	ns	t_{SC} = 0.5 ns
Data access time	$t_{A(DI)}$			2.3	ns	t_{SD} = 0.5 ns
Write access time	$t_{A(W)}$			2.3	ns	t_{SW} = 0.5 ns
Clock cycle time	t_{CYC}	6			ns	
Data release time	t_{DR}	0.3		1.8	ns	$t_{WL(Clk)} > t_{A(Clk)}$ max, $t_{SA} > t_{A(Add)}$ max, $t_{SC} > t_{A(CS)}$ max, $t_{SD} > t_{A(DI)}$ max
Address hold time	t_{HA}	1			ns	
$\overline{CS}$ hold time	t_{HC}	1			ns	
Data hold time	t_{HD}	1			ns	
$\overline{WE}$ hold time	t_{HW}	1			ns	
Address setup time	t_{SA}	0.5			ns	
$\overline{CS}$ setup time	t_{SC}	0.5			ns	
Data setup time	t_{SD}	0.5			ns	
$\overline{WE}$ setup time	t_{SW}	0.5			ns	
Clock high-pulse width	$t_{WH(Clk)}$	4.5			ns	
Clock low-pulse width	$t_{WL(Clk)}$	1.5			ns	

Notes:

(1) The device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

(2) See figure 1 for loading conditions and input pulse shape.

Figure 1. Test Circuit

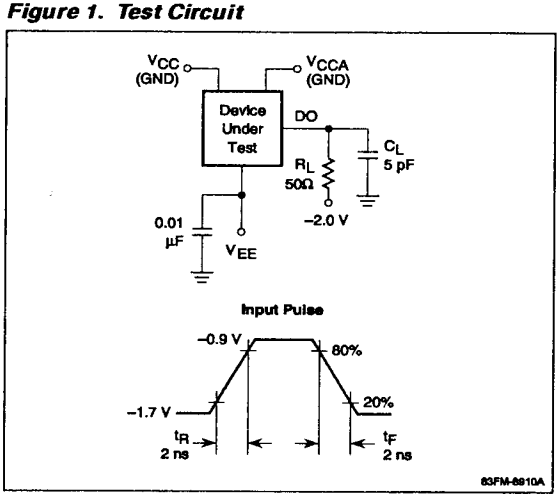
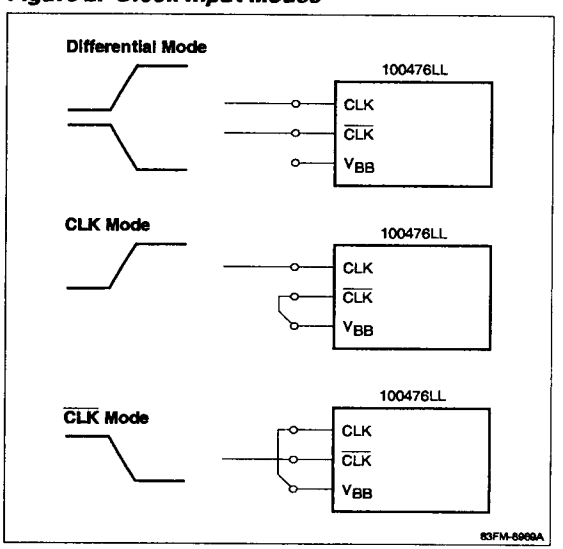
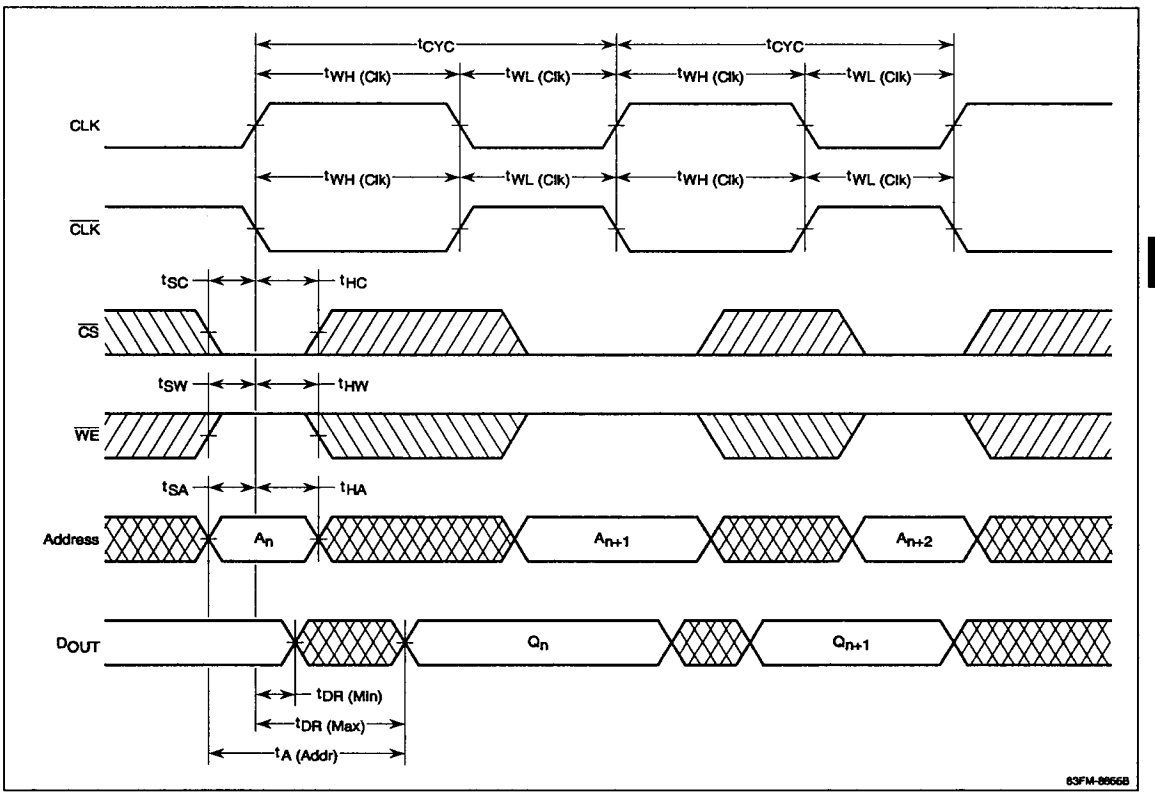


Figure 2. Clock Input Modes



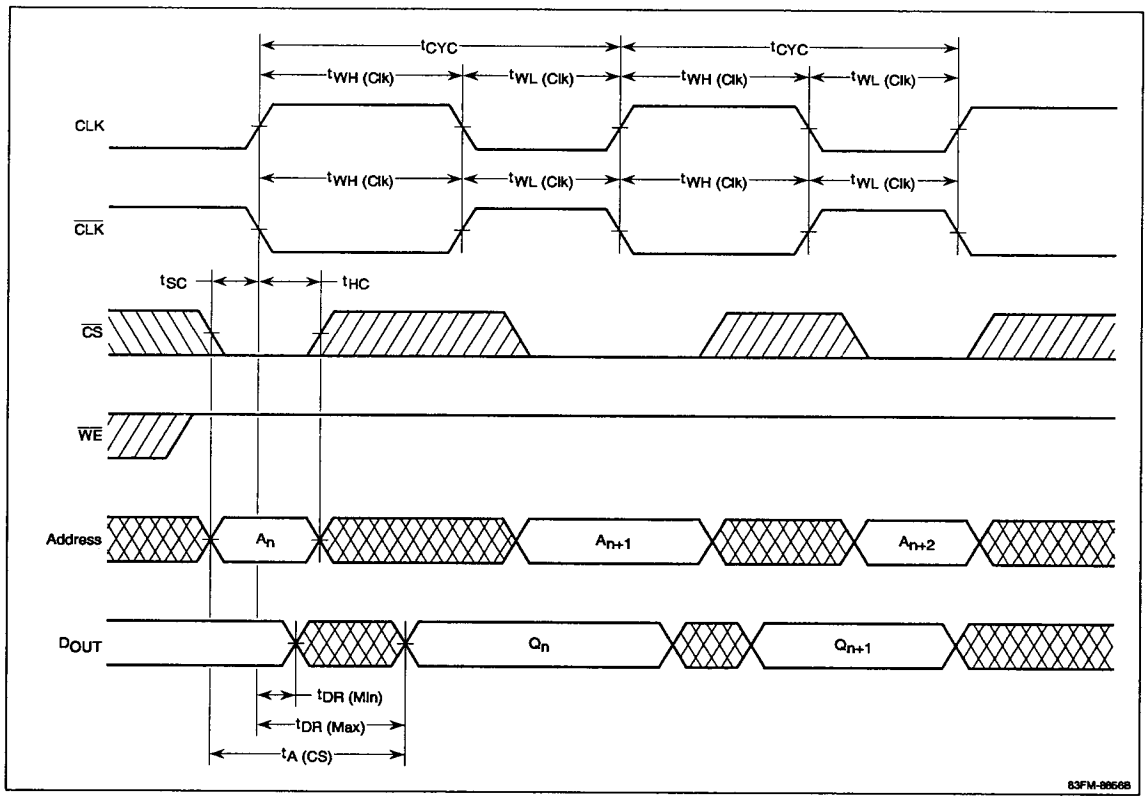
Timing Waveforms

Address Access, Read Mode



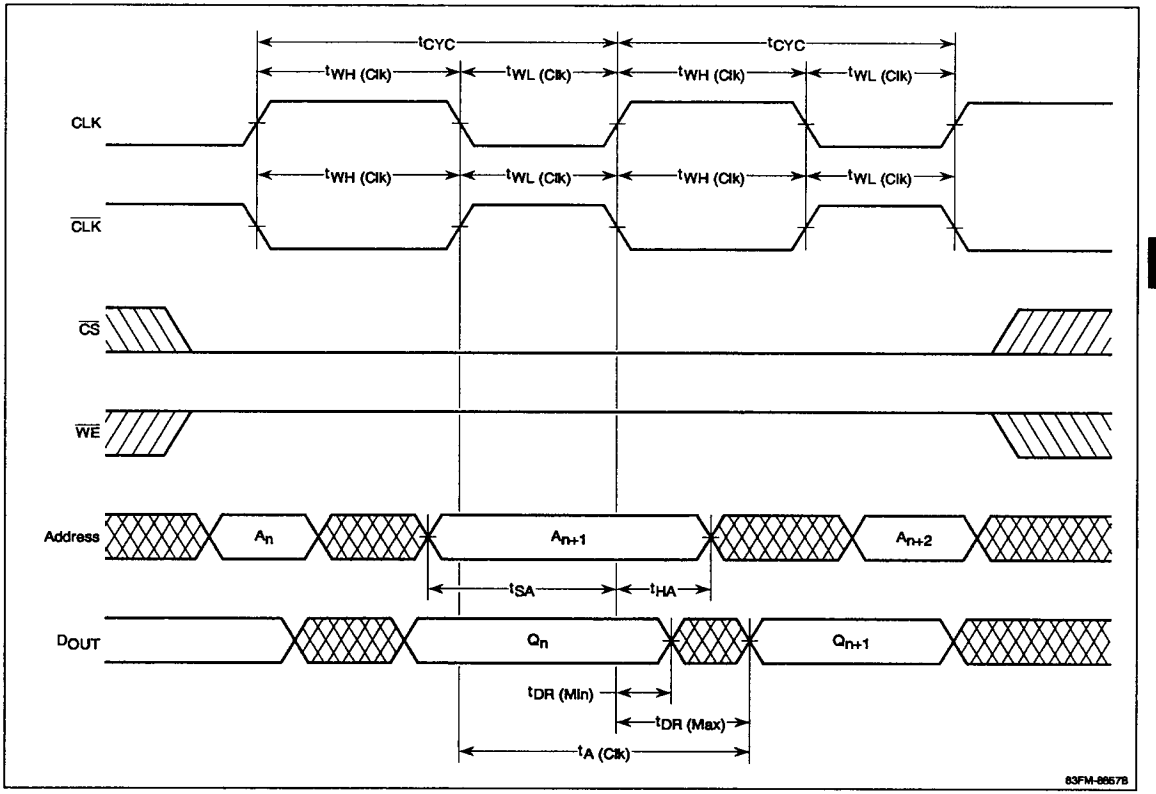
Timing Waveforms (cont)

Chip Select Access, Read Mode



Timing Waveforms (cont)

Clock Access, Read Mode



Timing Waveforms (cont)

Write Mode