Final COM'L

T-46-19-07

PALCE26V12H-20/25

28-Pin EE CMOS Versatile PAL® Device

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- 28-pin versatile PAL programmable logic device architecture
- Electrically erasable CMOS technology provides half power (only 105 mA) at high speed (20 ns propagation delay)
- 14 dedicated inputs and 12 input/output macrocells for architectural flexibility
- Macrocells can be registered or combinatorial, and active high or active low
- Varied product term distribution allows up to 16 product terms per output
- Two clock inputs for independent functions
- Global asynchronous reset and synchronous preset for initialization
- Register preload for testability and built-in register reset on power-up
- Space-efficient 28-pin SKINNYDIP® and PLCC packages
- Center V_{CC} and GND pins to improve signal characteristics
- Supported by PALASM® software and other design tools and standard logic programmers

GENERAL DESCRIPTION

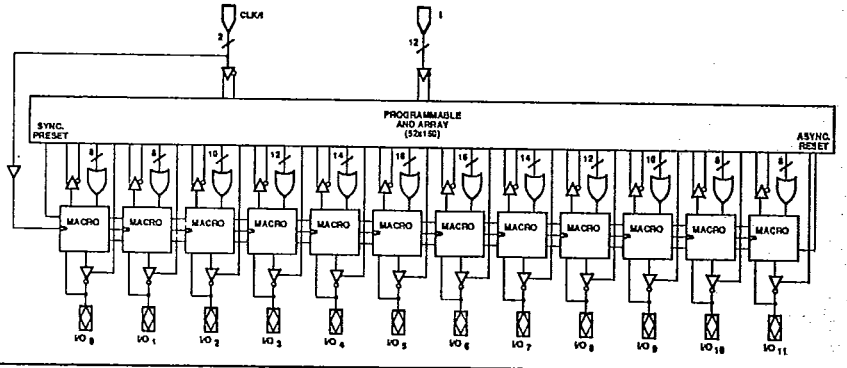
The PALCE26V12H is a 28-pin version of the popular PAL22V10 architecture. Built with low-power, high-speed, electrically-erasable CMOS technology, the PALCE26V12H offers many unique advantages.

Device logic is automatically configured according to the user's design specification. Design is simplified by PALASM design software from AMD, allowing automatic creation of a programming file based on Boolean or state equations. PALASM software also verifies the design and can provide test vectors for the programmed device. Third-party design tools and logic programmers also support the PALCE26V12H (see Programmer Reference Guide).

The PALCE26V12H utilizes the familiar sum-of-products (AND/OR) architecture that allows users to implement complex logic functions easily and efficiently. Multiple levels of combinatorial logic can always be reduced to sum-of-products form, taking advantage of the very wide input gates available in PAL devices. The functions are programmed into the device through electrically-erasable floating-gate cells in the AND logic array and the macrocells. In the unprogrammed state, all AND product terms float HIGH. If both true and complement of any input are connected, the term will be permanently LOW.

The product terms are connected to the fixed OR array with a varied distribution from 8 to 16 across the outputs (see Block Diagram). The OR sum of the products feeds the output macrocell. Each macrocell can be programmed as registered or combinatorial, active high or active low, with registered I/O possible. The flip-flop can be clocked by one of two clock inputs. The output configuration is determined by four bits controlling three multiplexers in each macrocell.

BLOCK DIAGRAM



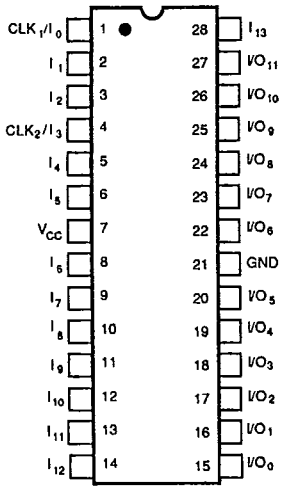
11757-001A

Publication # 11757 Rev. B Amendment /0
Issue Date: January 1990

T-46-19.07

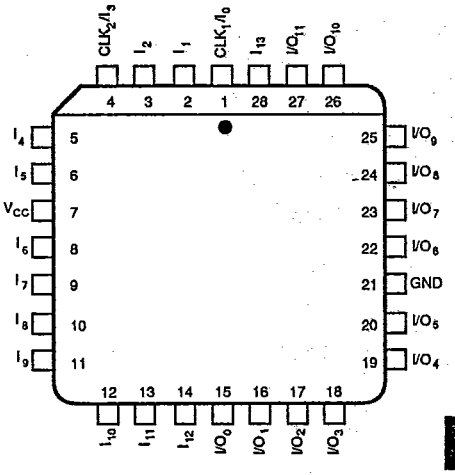
CONNECTION DIAGRAMS
Top View

SKINNYDIP



11757-005A

PLCC



11757-007A

PIN DESIGNATIONS

CLK	Clock
GND	Ground
I	Input
I/O	Input/Output
Vcc	Supply Voltage

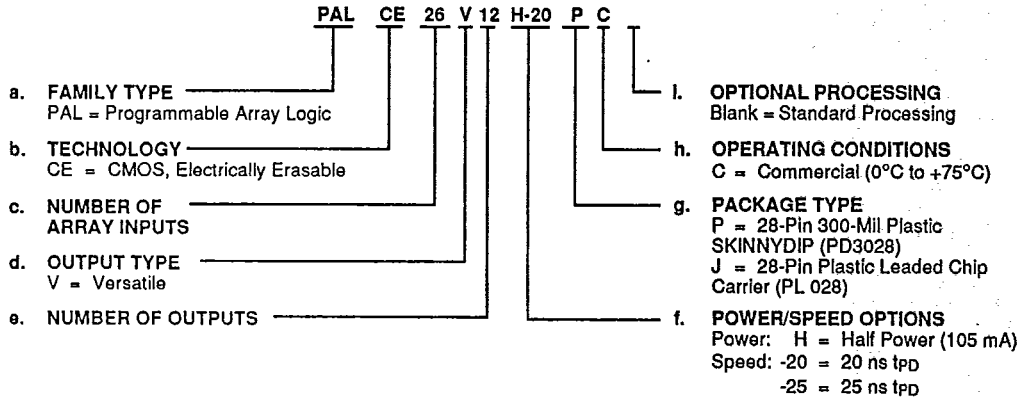
Note:
Pin 1 is marked for orientation.

T-46-19-07

ORDERING INFORMATION
Commercial Products

AMD commercial programmable logic products are available with several ordering options. The order number (Valid Combination) is formed by a combination of:

a. Family Type
b. Technology
c. Number of Array Inputs
d. Output Type
e. Number of Outputs
f. Power/Speed Options
g. Package Type
h. Operating Conditions
i. Optional Processing



Valid Combinations	
PALCE26V12H-20	PC, JC
PALCE26V12H-25	

Valid Combinations

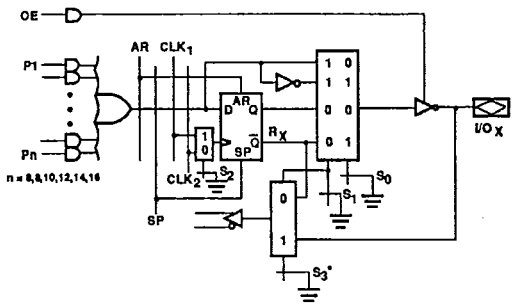
The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Note: Marked with AMD logo.

T-46-19-07

FUNCTIONAL DESCRIPTION

The PALCE26V12H has fourteen dedicated input lines, two of which can be used as clock inputs. Unused inputs should be tied directly to ground or V_{CC}. Buffers for device inputs and feedbacks have both true and complementary outputs to provide user-selectable signal polarity. The inputs drive a programmable AND logic array, which feeds a fixed OR logic array.



* When S_3 = 1 (unprogrammed), the feedback is selected by S_1. When S_3 = 0 (programmed), the feedback is the opposite of that selected by S_1.

11757-004A

Figure 1. PALCE26V12H Macrocell

S_3	S_1	S_0	Output Configuration
1	0	0	Registered Output and Feedback, Active Low
1	0	1	Registered Output and Feedback, Active High
1	1	0	Combinatorial I/O, Active Low
1	1	1	Combinatorial I/O, Active High
0	0	0	Registered I/O, Active Low
0	0	1	Registered I/O, Active High
0	1	0	Combinatorial Output, Registered Feedback, Active Low
0	1	1	Combinatorial Output, Registered Feedback, Active High

S_2	Clock Input
1	CLK_1/I_0
0	CLK_2/I_3

1 = Unprogrammed EE bit
0 = Programmed EE bit

The OR gates feed the twelve I/O macrocells (see figure 1). The macrocell allows one of eight potential output configurations; registered or combinatorial, active high or active low, with register or I/O pin feedback (see figure 2). In addition, registered configurations can be clocked by either of the two clock inputs.

The configuration choice is made according to the user's design specification and corresponding programming of the configuration bits S_0-S_3. Multiplexer controls initially float to V_{CC} (1) through a programmable cell, selecting the "1" path through the multiplexer. Programming the cell connects the control line to GND (0), selecting the "0" path.

Registered or Combinatorial

Each macrocell of the PALCE26V12H includes a D-type flip-flop for data storage and synchronization. The flip-flop is loaded on the LOW-to-HIGH edge of the selected clock input. Any macrocell can be configured as combinatorial by selecting a multiplexer path that bypasses the flip-flop. Bypass is controlled by bit S_1.

Programmable Clock

The clock input for any flip-flop can be selected to be from either pin 1 or pin 4. A 2:1 multiplexer controlled by bit S_2 determines the clock input.

Programmable Feedback

A 2:1 multiplexer allows the user to determine whether the macrocell feedback comes from the flip-flop or from the I/O pin, independent of whether the output is registered or combinatorial. Thus, registered outputs may have internal register feedback for higher speed (t_{CF} specification applies), or I/O feedback for use of the pin as a direct input (t_{CO} specification applies). Combinatorial outputs may have I/O feedback, either for use of the signal in other equations or for use as another direct input, or register feedback.

The feedback multiplexer is controlled by the same bit (S_1) that controls whether the output is registered or combinatorial, as on the 22V10, with an additional control bit (S_3) that allows the alternative feedback path to be selected. When S_3 = 1, S_1 selects register feedback for registered outputs (S_1 = 0) and I/O feedback for combinatorial outputs (S_1 = 1). When S_3 = 0, the opposite is selected: I/O feedback for registered outputs and register feedback for combinatorial outputs.

Programmable Enable and I/O

Each macrocell has a three-state output buffer controlled by an individual product term. Enable and disable can be a function of any combination of device inputs or feedback. The macrocell provides a bidirectional I/O pin if I/O feedback is selected, and may be configured as a dedicated input if the buffer is always disabled. This is accomplished by connecting all inputs to the enable term, forcing the AND of the complemented inputs to be always LOW. To permanently enable the outputs, all in-

T-46-19-07

puts are left disconnected from the term (the unprogrammed state).

Programmable Output Polarity

The polarity of each macrocell output can be active high or active low, either to match output signal needs or to reduce product terms. Programmable polarity allows Boolean expressions to be written in their most compact form (true or inverted), and the output can still be of the desired polarity. It can also save "DeMorganizing" efforts.

Selection is controlled by programmable bit S_0 in the output macrocell, and affects both registered and combinatorial outputs. Selection is automatic, based on the design specification and pin definitions. If the pin definition and output equation have the same polarity, the output is programmed to be active high.

Preset/Reset

For initialization, the PALCE26V12 has additional Preset and Reset product terms. These terms are connected to all registered outputs. When the Synchronous Preset (SP) product term is asserted high, the output registers will be loaded with a HIGH or the next LOW-to-HIGH clock transition. When the Asynchronous Reset (AR) product term is asserted high, the output registers will be immediately loaded with a LOW independent of the clock.

Note that preset and reset control the flip-flop, not the output pin. The output level is determined by the output polarity selected.

Power-Up Reset

All flip-flops power up to a logic LOW for predictable system initialization. Outputs of the PALCE26V12H will be HIGH or LOW depending on whether the output is active low or active high, respectively. The V_{CC} rise must be monotonic, and the reset delay time is 1 ms maximum.

Register Preload

The register on the PALCE26V12H can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, thereby making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

Security Bit

After programming and verification, a PALCE26V12H design can be secured by programming the security bit. Once programmed, this bit defeats readback of the internal programmed pattern by a device programmer, securing proprietary designs from competitors. Programming the security bit disables preload, and the array will read as if every bit is disconnected. The security bit can only be erased in conjunction with erasure of the entire pattern.

Quality and Testability

The PALCE26V12H offers a very high level of built-in quality. The erasability of the device provides a means of verifying performance of all AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to provide the highest programming yields and post-programming functional yields in the industry.

Programming and Erasing

The PALCE26V12 can be programmed on standard logic programmers. Approved programmers are listed in the Programmer Reference Guide.

The PALCE26V12 may be erased to reset a previously configured device back to its virgin state. Erasure is automatically performed by the programming hardware. No special erase operation is required.

T-46-19-07

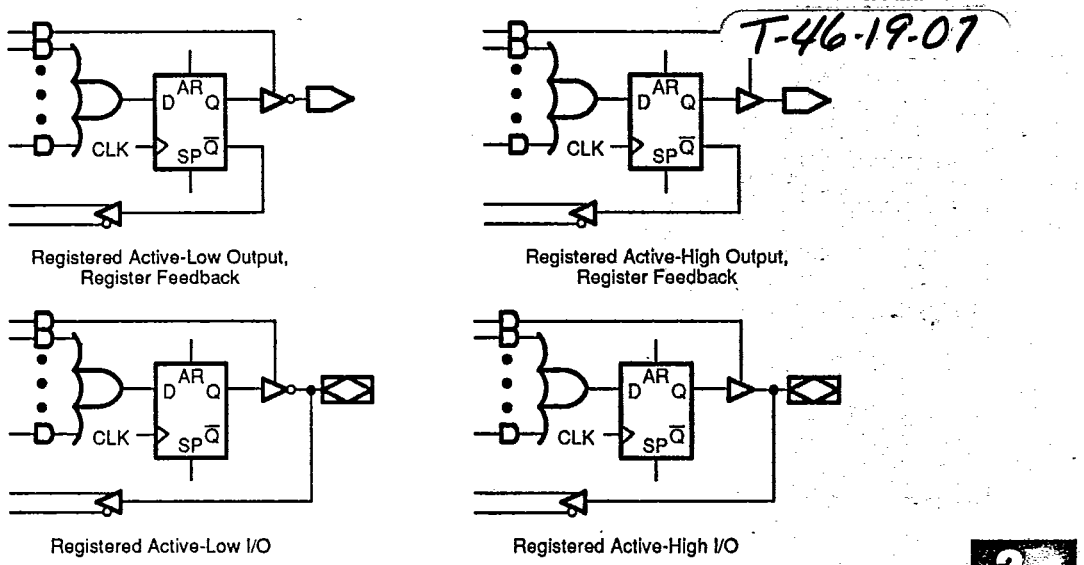
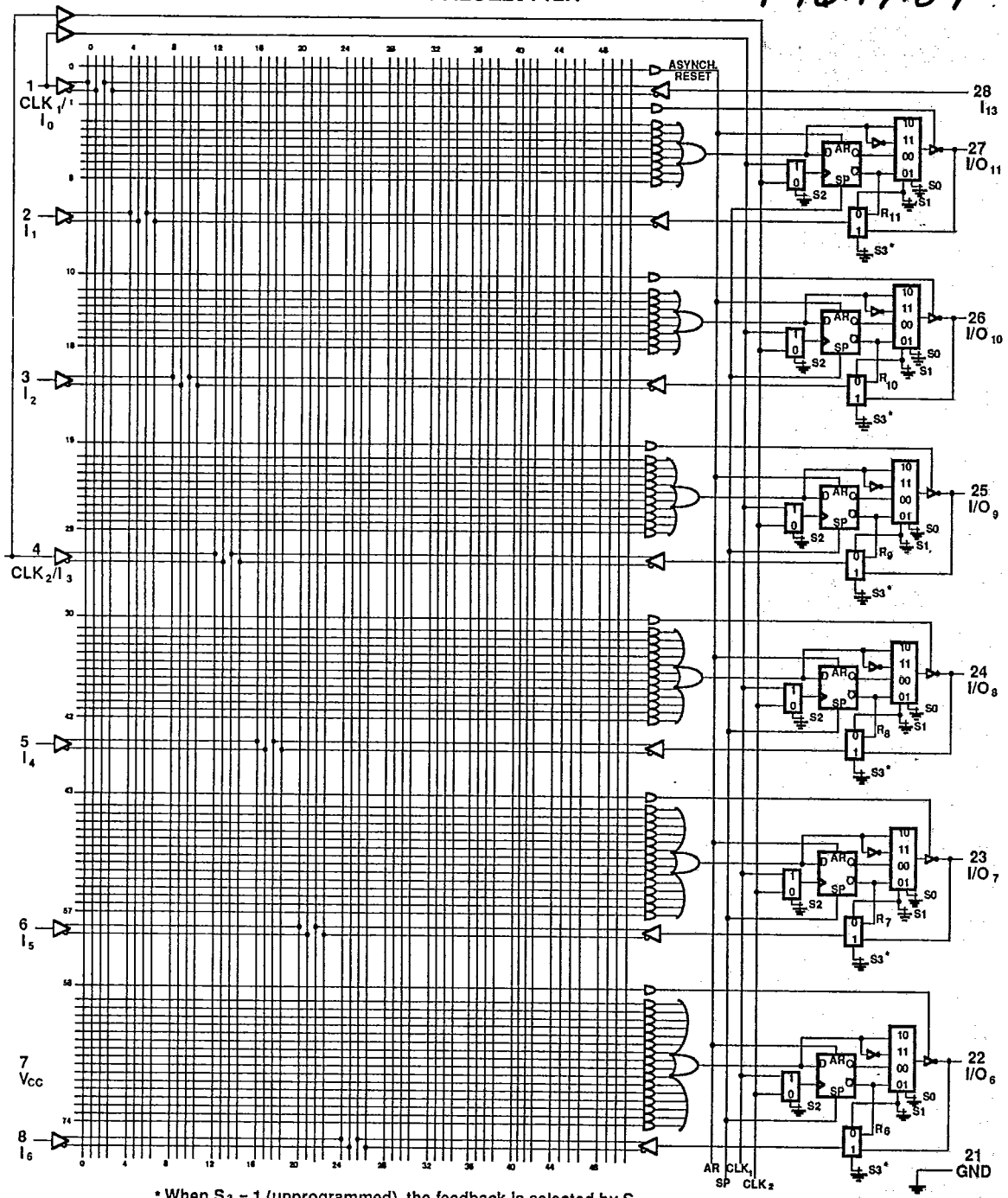


Figure 2. PALCE26V12H Macrocell Configuration Options

LOGIC DIAGRAM

PALCE26V12H

T-46-19-07



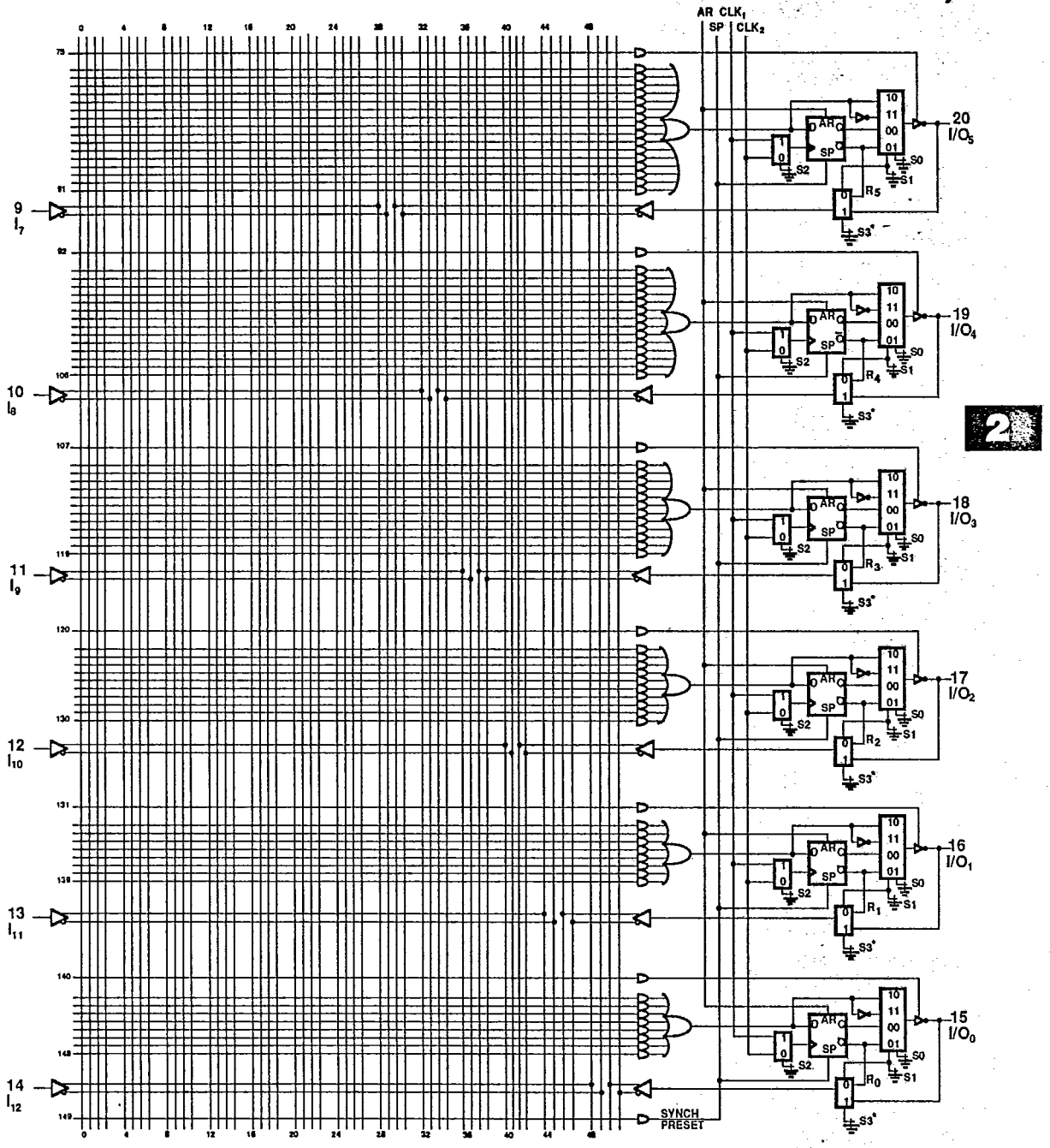
* When S_3 = 1 (unprogrammed), the feedback is selected by S_1.
When S_3 = 0 (programmed), the feedback is the opposite of that selected by S_1.

11757-006A

LOGIC DIAGRAM (Continued)

T-46-19.07

PALCE26V12H



*When S_3 = 1 (unprogrammed), the feedback is selected by S_1. When S_3 = 0 (programmed), the feedback is the opposite of that selected by S_1.

11757-006A
(Concluded)

T-46-19-07

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–0.6 V to +7.0 V
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} + 0.5 V
Static Discharge Voltage	2001 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.4	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.5 V, V_{CC} = Max. (Note 2)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max. (Note 2)		–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.5 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		105	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

T-46-19-07

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0 V	V_{CC} = 5.0 V, T_A = +25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V		8	pF

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

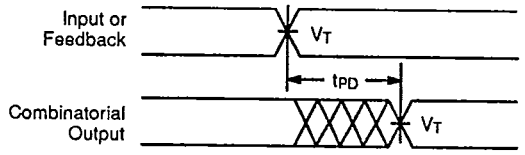
Parameter Symbol	Parameter Description			-20 Min.	-20 Max.	-25 Min.	-25 Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output				20		25	ns
t_S	Setup Time from Input, Feedback, or SP to Clock			13		15		ns
t_H	Hold Time			0		0		ns
t_{CO}	Clock to Output				12		15	ns
t_{CF}	Clock to Feedback (Note 3)				10		13	ns
t_{AR}	Asynchronous Reset to Registered Output				25		30	ns
t_{ARW}	Asynchronous Reset Width			20		25		ns
t_{ARR}	Asynchronous Reset Recovery Time			20		25		ns
t_{SPR}	Synchronous Preset Recovery Time			13		15		ns
t_{WL}	Clock Width	LOW		10		13		ns
t_{WH}		HIGH		10		13		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	$1/(t_S + t_{CO})$	40		33.3		MHz
		Internal Feedback	$1/(t_S + t_{CF})$	43		35		MHz
t_{EA}	Input to Output Enable Using Product Term Control				20		25	ns
t_{ER}	Input to Output Disable Using Product Term Control				20		25	ns

Notes:

2. See Switching Test Circuit for test conditions.
3. Calculated from measured f_{MAX} internal.
4. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

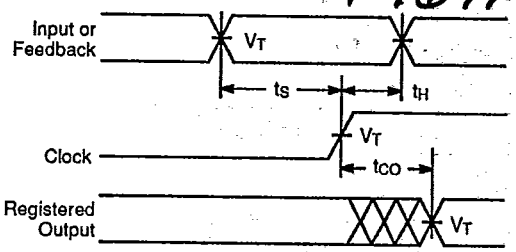
SWITCHING WAVEFORMS

T-46-19-07



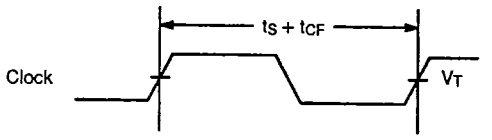
12015-010A

Combinatorial Output



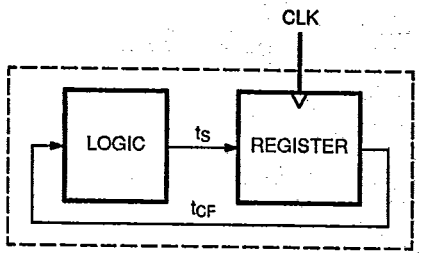
12015-012A

Registered Output

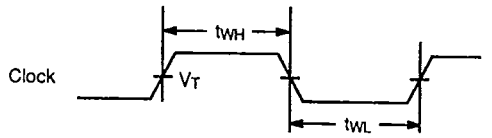


12149-025A

Clock to Feedback (f_{MAX} Internal)
See Path at Right

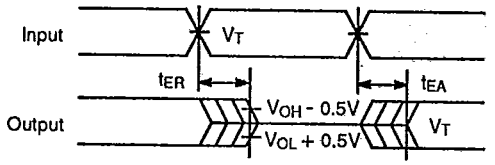


12015-021A



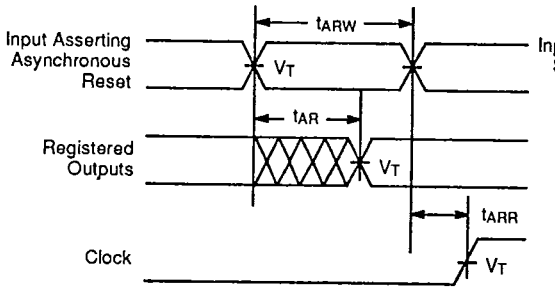
12015-011A

Clock Width



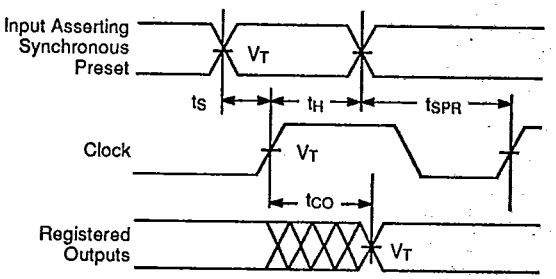
12015-013A

Input to Output Disable/Enable



11757-009A

Asynchronous Reset



11757-010A

Synchronous Preset

Notes:

1. V_T = 1.5 V
2. Input pulse amplitude 0 V to 3.0 V.
3. Input rise and fall times 2–5 ns typical.

KEY TO SWITCHING WAVEFORMS

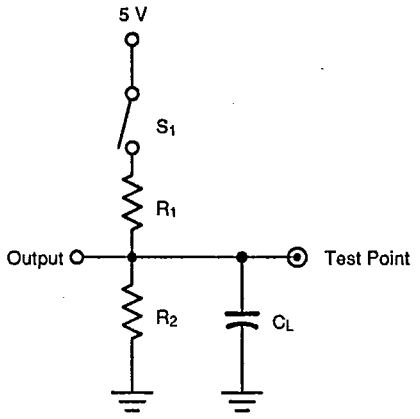
T-46-19-07

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care; Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

2

SWITCHING TEST CIRCUIT



12350-019A

Specification	S_1	C_L	R_1	R_2	Measured Output Value
t_{PD}, t_{CO}, t_{CF}	Closed	50 pF	300 Ω	390 Ω	1.5 V
t_{EA}	Z → H: Open Z → L: Closed				1.5 V
t_{ER}	H → Z: Open L → Z: Closed	5 pF			H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

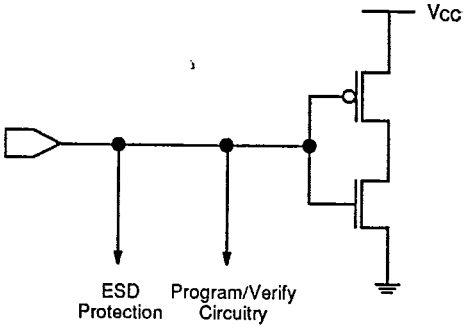
T-46-19-07

ENDURANCE CHARACTERISTICS

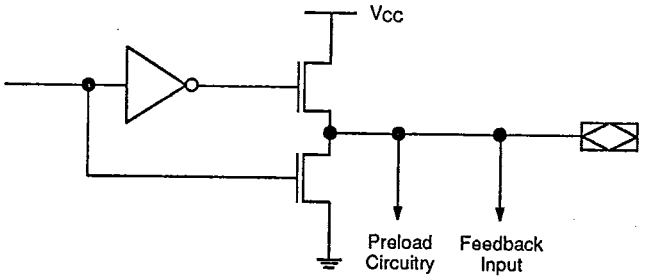
The PALCE26V12 is manufactured using AMD's advanced Electrically Erasable process. This technology uses an EE cell to replace the fuse link used in bipolar parts. As a result, the device can be erased and reprogrammed – a feature which allows 100% testing at the factory.

Symbol	Parameter	Min.	Unit	Test Conditions
t_{DR}	Min. Pattern Data Retention Time	10	Years	Max. Storage Temperature
		20	Years	Max. Operating Temperature
N	Min. Reprogramming Cycles	100	Cycles	Normal Programming Conditions

INPUT/OUTPUT EQUIVALENT SCHEMATICS



Typical Input



Typical Output

12197-013A

T-46-19-07

OUTPUT REGISTER PRELOAD

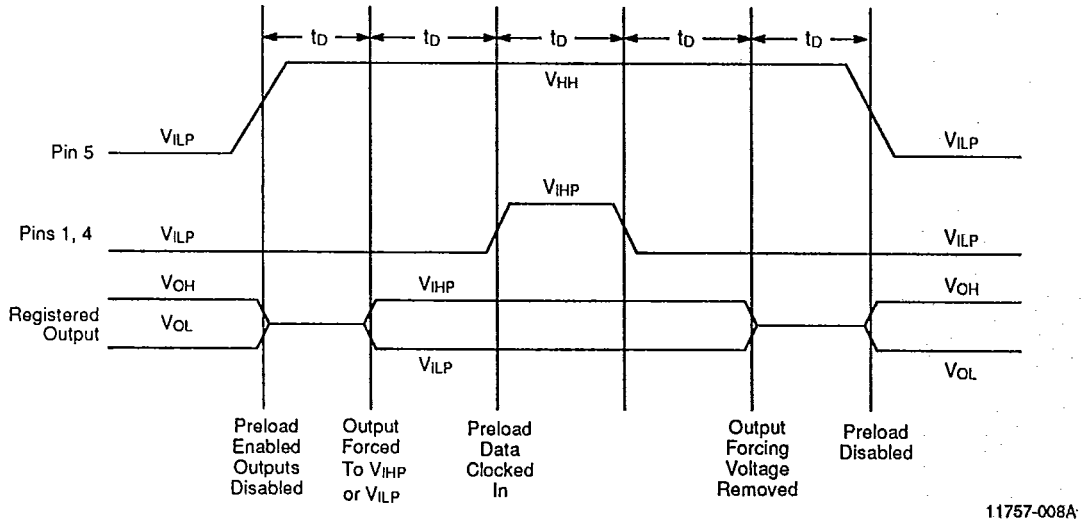
The PALCE26V12H registered outputs are provided with circuitry to allow loading each register synchronously with either a HIGH or LOW. This feature will simplify testing since any state can loaded into the registers to control test sequencing.

The pin levels and timing necessary to perform the Preload function are detailed below.

1. Raise V_{CC} to 5.0 V ± 0.5 V.
2. Set pin 5 to V_{HH} to disable outputs and enable preload.
3. Apply the desired value (V_{ILP}/V_{IHP}) to all registered output pins. Leave combinatorial output pins floating.
4. Clock appropriate pins, 1 and/or 4, from V_{ILP} to V_{IHP}.
5. Remove V_{ILP}/V_{IHP} from all registered outputs.
6. Lower pin 5 to V_{IL}/V_{IH}.
7. Enable outputs according to programmed pattern. Verify for V_{OL}/V_{OH} at all registered output pins. Note that the output pin signal will depend on the programmed polarity.

Parameter Symbol	Parameter Description	Min.	Rec.	Max.	Unit
V_{HH}	Super-level Input Voltage	10.25	10.5	10.75	V
V_{ILP}	Low-level Input Voltage	0	0	0.5	V
V_{IHP}	High-level Input Voltage	2.4	5.0	5.5	V
t_D	Delay Time	10	100		µs

Level forced on registered output pin during Preload cycle	Register Q output state after cycle
V_{IHP}	HIGH
V_{ILP}	LOW



11757-008A

Preload Waveforms

POWER-UP RESET

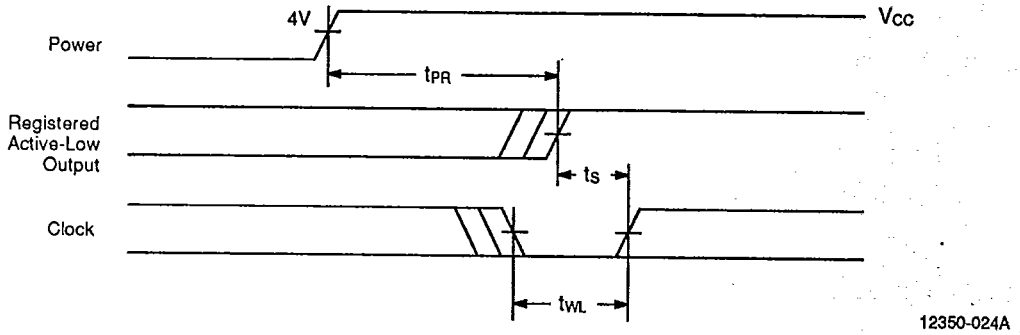
The power-up reset feature ensures that all flip-flops will be reset to LOW after the device has been powered up. The output state will depend on the programmed configuration. This feature is valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

1. The V_{CC} rise must be monotonic.

T-46-19-07

2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Description	Max.	Unit
t_{PR}	Power-up Reset Time	1000	ns
t_S	Input or Feedback Setup Time	See Switching Characteristics	
t_{WL}	Clock Width LOW		



Power-Up Reset Waveform