Integrated Device Technology, Inc.

BiCMOS STATIC RAM 256K (64K x 4-BIT)

PRELIMINARY
IDT71B258

FEATURES:

- 64K x 4 BiCEMOS™ Static RAM
- High-speed address/chip select time
  - — Military: 15/20ns
  - — Commercial: 12/15/20ns
- Single chip select
- Single 5V (±10%) power supply
- Input and output directly TTL-compatible
- Available in 24-pin, 300 mil sidebraze ceramic DIP; 24-pin, 300 mil plastic DIP and 24-pin, 300 mil plastic SOJ packages

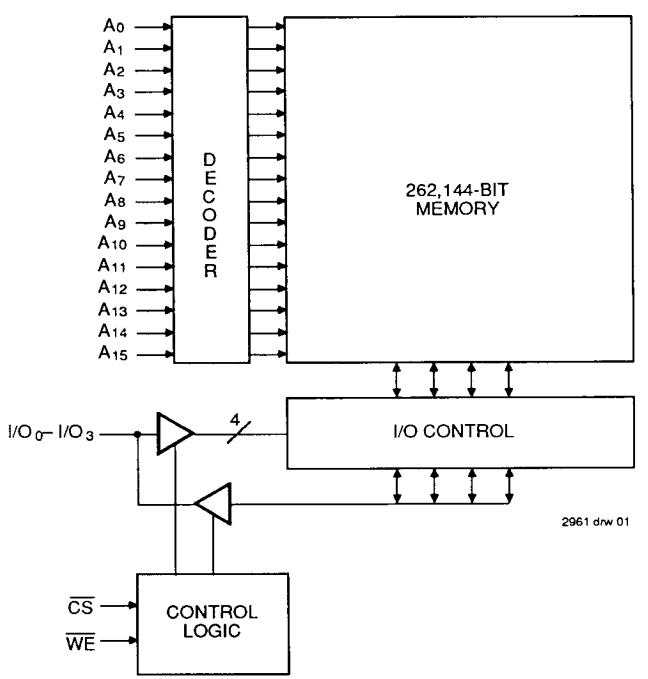
DESCRIPTION:

The IDT71B258 is a 262,144-bit high-speed static RAM organized as 64Kx4. It is fabricated using IDT's high-perfomance high-reliability BiCEMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective solution for high-speed memory needs.

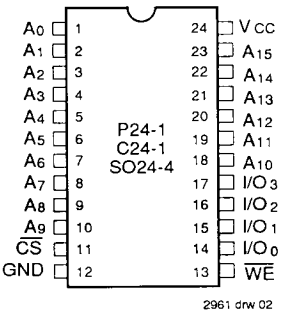
Address access times as fast as 12ns are available with power consumption of only 450mW (typ.) All inputs and outputs of the IDT71B258 are TTL-compatible and operation is from a single 5V supply. Fully static asynchronous circuitry is used, requiring no clocks or refreshing for operation.

The IDT71B258 is packaged in a 24-pin, 300-mil sidebraze; 24-pin, 300 mil plastic DIP and a 24-pin SOJ packages.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



DIP/SOJ
TOP VIEW

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TRUTH TABLE[1]

$\overline{CS}$	$\overline{WE}$	I/O	Function
L	H	DOUT	Read
L	L	DIN	Write
H	X	Hi-Z	Deselect Chip

NOTE:
1. H = VIH, L = VIL, X = Don't care.

2961 tbl 01

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0	V
VIL	Input Low Voltage	-0.5	—	0.8	V

NOTE:
1. 1.5V undershoots are allowed for 10ns once per cycle.

2961 tbl 04

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Max.	Unit
CIN	Input Capacitance	8	pF
COUT	Output Capacitance	12	pF

NOTE:
1. This parameter is guaranteed by device characterization, but is not production tested.

2961 tbl 03

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Com'l.	Mil.	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +125	°C
PT	Power Dissipation	1.0	1.0	W
IOUT	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2961 tbl 02

DC ELECTRICAL CHARACTERISTICS

VCC = 5.0V ± 10%

Symbol	Parameter	Test Condition	IDT71B258			Unit
			Min.	Typ.[1]	Max.	
|ILI|	Input Leakage Current	VCC = Max., VIN = GND to VCC	—	—	10	µA
|ILO|	Output Leakage Current	VCC = Max., $\overline{CS}$ = VIH, VOUT = GND to VCC	—	—	10	µA
VOL	Output Low Voltage	IOL = 10mA, VCC = Min.	—	—	0.5	V
		IOL = 8mA, VCC = Min.	—	—	0.4	
VOH	Output High Voltage	IOH = -4mA, VCC = Min.	2.4	—	—	V

NOTE:
1. Typical limits are at VCC = 5.0V, +25°C ambient.

2961 tbl 05

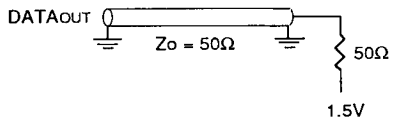
DC ELECTRICAL CHARACTERISTICS[1]

(VCC = 5.0V ± 10%)

Symbol	Parameter	71B258S12		71B258S15		71B258S20		Unit
		Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
ICC	Dynamic Operating Current $\overline{CS}$ = VIL, Outputs Open, VCC = Max., f = fMAX[2]	180	—	160	170	140	150	mA

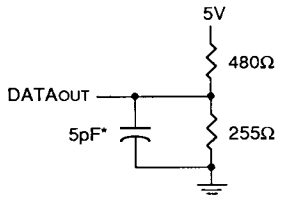
NOTES:
1. All values are maximum guaranteed values.
2. fMAX = 1/tRC.

2961 tbl 05



2961 drw 03a

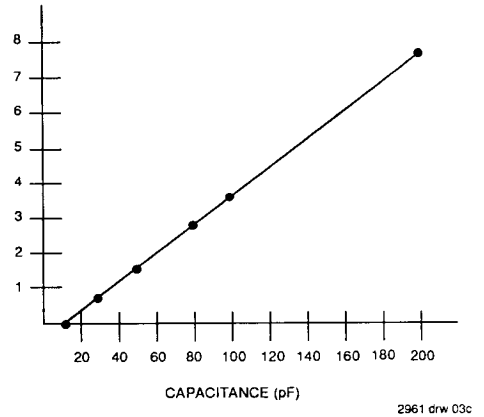
Figure 1A. AC Test Loads



2961 drw 03b

*Including jig and scope capacitance.

Figure 1B. AC Test Loads



2961 drw 03c

Figure 1C. Lumped Capacitive Load, Typical Derating

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1A, 1B & 1C

2961 tbl 06

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	71B258-12(1) Min.	71B258-12(1) Max.	71B258-15 Min.	71B258-15 Max.	71B258-20 Min.	71B258-20 Max.	Unit
Read Cycle								
tRC	Read Cycle Time	12	—	15	—	20	—	ns
tAA	Address Access Time	—	12	—	15	—	20	ns
tACS	$\overline{CS}$ Access Time	—	5	—	6	—	8	ns
tCLZ(2)	$\overline{CS}$ to Output in Low Z	2	—	2	—	2	—	ns
tCHZ(2)	$\overline{CS}$ to Output in High Z	—	5	—	6	—	7	ns
tOH	Out Hold from Add Change	5	—	5	—	5	—	ns
Write Cycle								
tWC	Write Cycle Time	12	—	15	—	20	—	ns
tCW	Chip Select to End of Write	8	—	9	—	10	—	ns
tAW	Add to End of Write	9	—	10	—	12	—	ns
tAS	Address to $\overline{CS}$	0	—	0	—	0	—	ns
tWP	Write Pulse Width	9	—	10	—	12	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tWHZ(2)	$\overline{WE}$ to Output in High Z	—	5	—	6	—	7	ns
tDW	Data Set-Up Time	5	—	6	—	8	—	ns
tDH	Data Hold from Write	0	—	0	—	0	—	ns
tOW	Out Active from End of $\overline{WE}$	2	—	2	—	2	—	ns

2961 tbl 08

NOTES:
1. 0° to +70°C temperature range only.
2. This parameter is guaranteed with the AC Load, Figure 1B, and is not tested.

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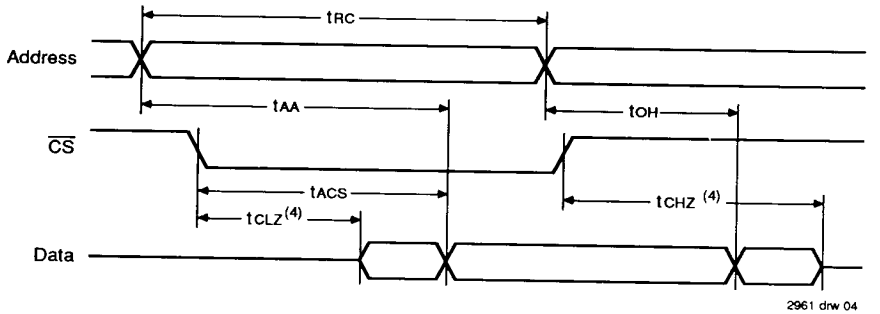
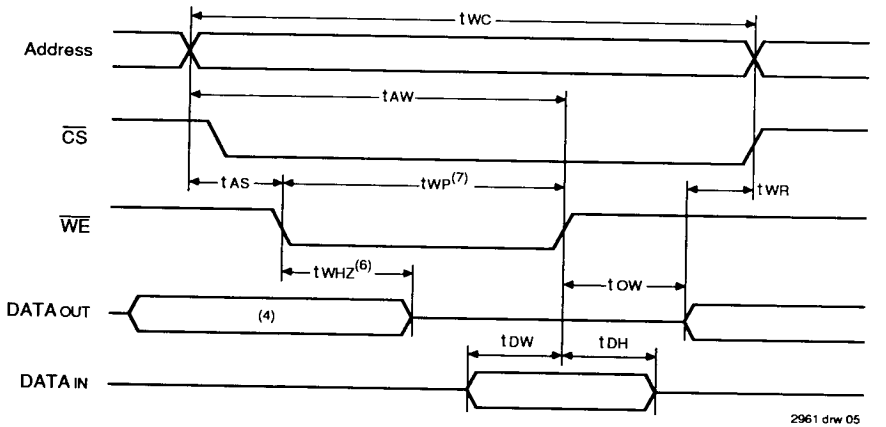
TIMING WAVEFORM OF READ CYCLE(1,2,3)



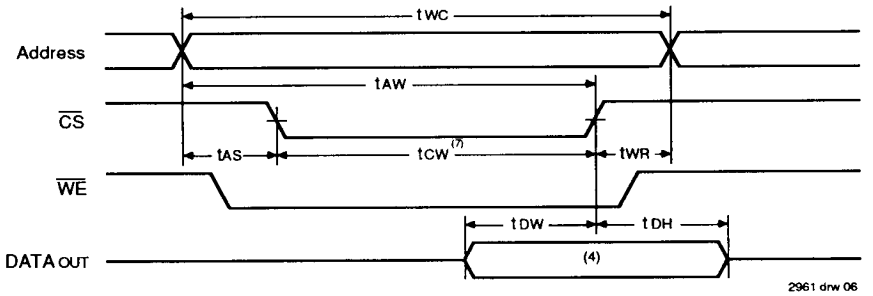
NOTES:
1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±200mV from steady state with 5pF load (including scope and jig).

TIMING WAVEFORM OF WRITE CYCLE NO.1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3, 5,6)



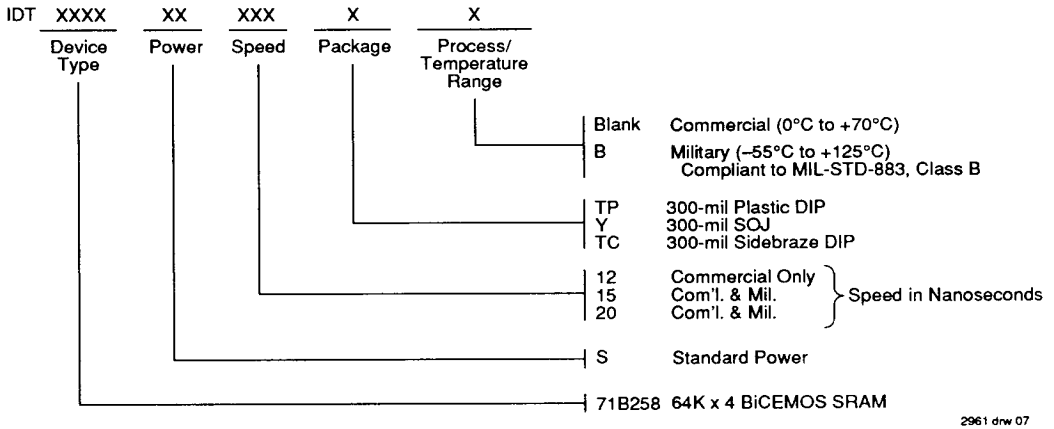
NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (twc and twp) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. twr is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in the high impedance.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig).
7. During a $\overline{WE}$ controlled write cycle, the pulse width must be the larger of twp or (tdw + twhz) to allow the I/O drivers to turn off and data to be placed on the bus for the required tdw.

TIMING WAVEFORM OF WRITE CYCLE NO.2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3, 5,6)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (twc and twp) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. twr is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in the high impedance.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig).
7. During a $\overline{WE}$ controlled write cycle, the pulse width must be the larger of twp or (tdw + twhz) to allow the I/O drivers to turn off and data to be placed on the bus for the required tdw.

ORDERING INFORMATION



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