Integrated Device Technology, Inc.

3.3V CMOS 16-BIT REGISTER (3-STATE)

IDT54/74FCT163374/A/C
IDT54/74FCT163H374/A/C

FEATURES:

- 0.5 MICRON CMOS Technology
- **Typical $t_{SK(o)}$ (Output Skew) < 250ps**
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 25 mil Center SSOP and Cerpack Packages and 19.6 mil pitch TSSOP Package
- Extended commercial range of -40°C to +85°C
- V_{CC} = 3.3V ±0.3V, Normal Range or V_{CC} = 2.7 to 3.6V, Extended Range
- CMOS power levels (10µW typ. static)
- Rail-to-Rail output swing for increased noise margin
- Military product compliant to MIL-STD-883, Class B
- Low Ground Bounce (0.3V typ.)
- Inputs (except I/O) can be driven by 3.3V or 5V components

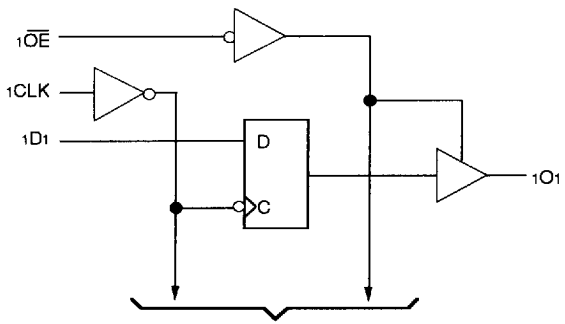
DESCRIPTION:

The IDT54/74FCT163374/A/C 16-bit edge-triggered D-type registers are built using advanced dual metal CMOS technology. These high-speed, low-power registers are ideal for use as buffer registers for data synchronization and storage. The Output Enable ($x\overline{OE}$) and clock (xCLK) controls are organized to operate each device as two 8-bit registers or one 16-bit register with common clock. Flow-through organization of signal pins facilitates ease of layout. All inputs are designed with hysteresis for improved noise margin.

The inputs of IDT54/74FCT163374/A/C can be driven from either 3.3V or 5V devices. This feature allows the use of these devices as translators in a mixed 3.3V/5V supply system.

The IDT54/74FCT163H374/A/C have "Bus Hold" which retains the input's last state whenever the input goes to high impedance. This prevents "floating" inputs and eliminates the need for pull-up/down resistors.

FUNCTIONAL BLOCK DIAGRAM



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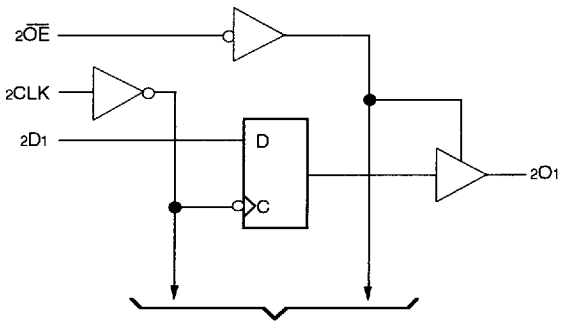

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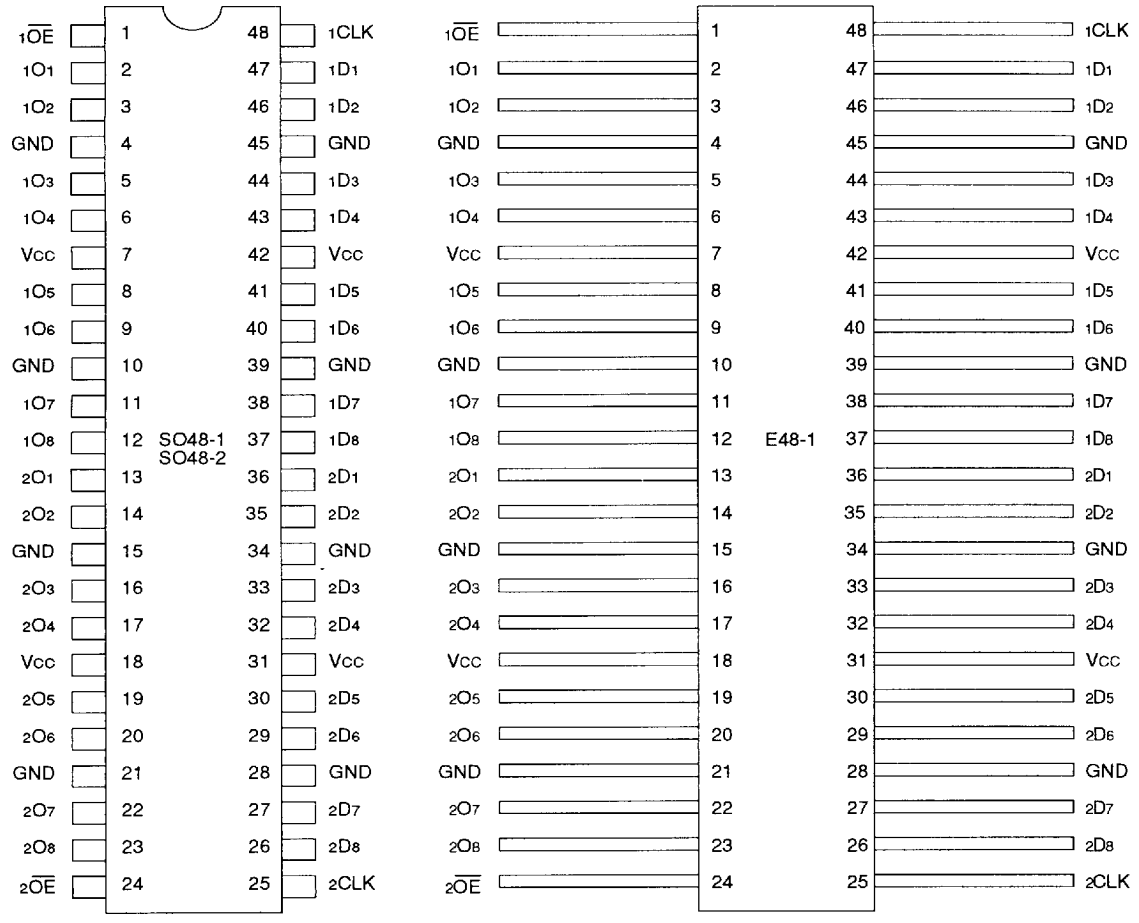
PIN CONFIGURATIONS



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PIN DESCRIPTION

Pin Names	Description
xDx	Data Inputs(1)
xCLK	Clock Inputs
xOx	3-State Outputs.
$x\overline{OE}$	3-State Output Enable Input (Active LOW)

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NOTE:
1. On FCT163H374 these pins have "Bus Hold". All other pins are standard inputs, outputs or I/Os.

FUNCTION TABLE(1)

Function	Inputs			Outputs
	xDx	xCLK	$x\overline{OE}$	xOx
Hi-Z	X	L	H	Z
	X	H	H	Z
Load Register	L	↑	L	L
	H	↑	L	H
	L	↑	H	Z
	H	↑	H	Z

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NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance
   ↑ = LOW-to-HIGH transition

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +4.6	–0.5 to +4.6	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(4)	Terminal Voltage with Respect to GND	–0.5 to V_{CC} + 0.5	–0.5 to V_{CC} + 0.5	V
T_A	Operating Temperature	–40 to +85	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	–60 to +60	–60 to +60	mA

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NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Vcc terminals.
3. Input terminals.
4. Output and I/O terminals.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	3.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	3.5	8.0	pF

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NOTE:
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (STANDARD PARTS)

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 2.7V to 3.6V; Military: T_A = –55°C to +125°C, V_{CC} = 2.7V to 3.6V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level (Input pins)	Guaranteed Logic HIGH Level		2.0	—	5.5	V
	Input HIGH Level (I/O pins)			2.0	—	V_{CC}+0.5	
V_{IL}	Input LOW Level (Input and I/O pins)	Guaranteed Logic LOW Level		–0.5	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)[6]	V_{CC} = Max.	V_I = 5.5V	—	—	±1	µA
	Input HIGH Current (I/O pins)[6]		V_I = V_{CC}	—	—	±1	
I_{IL}	Input LOW Current (Input pins)[6]		V_I = GND	—	—	±1	
	Input LOW Current (I/O pins)[6]		V_I = GND	—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = V_{CC}	—	—	±1	µA
I_{OZL}	(3-State Output pins)[6]		V_O = GND	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{ODH}	Output HIGH Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		–36	–60	–110	mA
I_{ODL}	Output LOW Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		50	90	200	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –0.1mA	V_{CC}–0.2	—	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –3mA	2.4	3.0	—	
		V_{CC} = 3.0V, V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4[5]	3.0	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 0.1mA	—	—	0.2	V
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA	—	0.2	0.4	
			I_{OL} = 24mA	—	0.3	0.5	
I_{OS}	Short Circuit Current[4]	V_{CC} = Max., V_O = GND[3]		–60	–135	–240	mA
V_H	Input Hysteresis	—		—	150	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}	COM'L.	—	0.1	10	µA
			MIL.	—	0.1	100	

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NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 3.3V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. V_{OH} = V_{CC} –0.6V at rated current.
6. The test limit for this parameter is ±5µA at T_A = –55°C.

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DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (BUS HOLD)

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 2.7V to 3.6V; Military: T_A = –55°C to +125°C, V_{CC} = 2.7V to 3.6V

Symbol	Parameter		Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level (Input pins)		Guaranteed Logic HIGH Level		2.0	—	5.5	V
	Input HIGH Level (I/O pins)				2.0	—	V_{CC}+0.5	
V_{IL}	Input LOW Level (Input and I/O pins)		Guaranteed Logic LOW Level		–0.5	—	0.8	V
I_{IH}	Input HIGH Current[7]	Standard Input[6]	V_{CC} = Max.	V_I = V_{CC}	—	—	±1	µA
		Standard I/O[6]			—	—	±1	
		Bus Hold Input			—	—	±100	
		Bus Hold I/O			—	—	±100	
I_{IL}	Input LOW Current[7]	Standard Input[6]		V_I = GND	—	—	±1	
		Standard I/O[6]			—	—	±1	
		Bus Hold Input			—	—	±100	
		Bus Hold I/O			—	—	±100	
I_{BHH}	Bus Hold Sustain Current[7]	Bus Hold Input	V_{CC} = Min.	V_I = 2.0V	–50	—	—	µA
I_{BHL}				V_I = 0.8V	+50	—	—	
I_{BHHO}	Bus Hold Overdrive Current[7]	Bus Hold Input	V_{CC} = Max.	V_I = 1.5V	—	—	TBD	mA
I_{BHLO}					—	—	TBD	
I_{OZH}	High Impedance Output Current (3-State Output pins)[6]		V_{CC} = Max.	V_O = V_{CC}	—	—	±1	µA
I_{OZL}				V_O = GND	—	—	±1	
V_{IK}	Clamp Diode Voltage		V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{DH}	Output HIGH Current		V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		–36	–60	–110	mA
I_{ODL}	Output LOW Current		V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		50	90	200	mA
V_{OH}	Output HIGH Voltage		V_{CC} = Min.	I_{OH} = –0.1mA	V_{CC}–0.2	—	—	V
			V_{IN} = V_{IH} or V_{IL}	I_{OH} = –3mA	2.4	3.0	—	
			V_{CC} = 3.0V V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4[5]	3.0	—	
V_{OL}	Output LOW Voltage		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 0.1mA	—	—	0.2	V
				I_{OL} = 16mA	—	0.2	0.4	
				I_{OH} = 24mA	—	0.3	0.5	
I_{OS}	Short Circuit Current[4]		V_{CC} = Max., V_O = GND[3]		–60	–135	–240	mA
V_H	Input Hysteresis		—		—	150	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current		V_{CC} = Max., V_{IN} = GND or V_{CC}	COM'L.	—	0.1	10	µA
				MIL.	—	0.1	100	

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NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. V_{OH} = V_{CC} –0.6V at rated current.
6. The test limit for this parameter is ±5µA at T_A = –55°C.
7. Pins with Bus Hold are identified in the pin description.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current	V_{CC} = Max.	V_{IN} = V_{CC} – 0.6V[3]	—	2.0	30	µA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $x\overline{OE}$ = GND 50% Duty Cycle One Input Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	50	75	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $x\overline{OE}$ = GND fi = 5MHz 50% Duty Cycle One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	0.5	0.8	mA
			V_{IN} = V_{CC} –0.6V V_{IN} = GND	—	0.5	0.8	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $x\overline{OE}$ = GND fi = 2.5MHz 50% Duty Cycle Sixteen Bits Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	2.5	3.8[5]	
			V_{IN} = V_{CC} –0.6V V_{IN} = GND	—	2.5	4.0[5]	

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NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Per TTL driven input; all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

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SWITCHING CHARACTERISTICS OVER OPERATING RANGE[4]

Symbol	Parameter	Condition[1]	FCT163374 FCT163H374				FCT163374A FCT163H374A				FCT163374C FCT163H374C				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay xCLK to xOx	CL = 50pF RL = 500Ω	2.0	10.0	2.0	11.0	2.0	6.5	2.0	7.2	2.0	5.2	—	—	ns
tPZH tPZL	Output Enable Time		1.5	12.5	1.5	14.0	1.5	6.5	1.5	7.5	1.5	5.5	—	—	ns
tPHZ tPLZ	Output Disable Time		1.5	8.0	1.5	8.0	1.5	5.5	1.5	6.5	1.5	5.0	—	—	ns
tSU	Set-up Time HIGH or LOW, xDx to xCLK		2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	—	—	ns
tH	Hold Time HIGH or LOW, xDx to xCLK		1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	—	—	ns
tW	xCLK Pulse Width HIGH or LOW		7.0	—	7.0	—	5.0	—	6.0	—	5.0	—	—	—	ns
tSK(o)	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	—	ns

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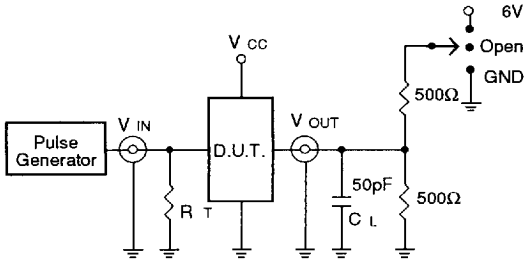
NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.
4. Propagation Delay and Enable/Disable times are with VCC = 3.3V ±0.3V, Normal Range. For VCC = 2.7V to 3.6V, Extended Range, all Propagation Delays and Enable/Disable times should be degraded by 20%.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



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SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	6V
Disable High Enable High	GND
All Other tests	Open

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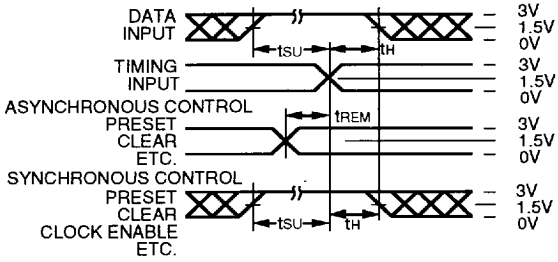
DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



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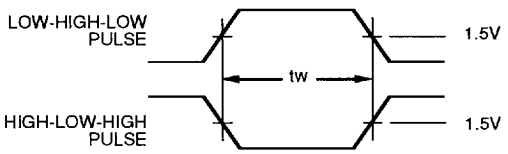
PULSE WIDTH



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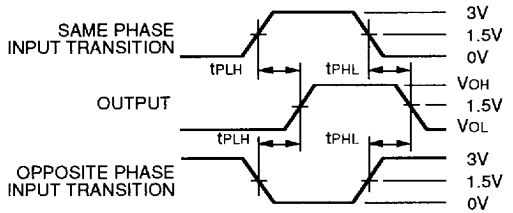
PROPAGATION DELAY



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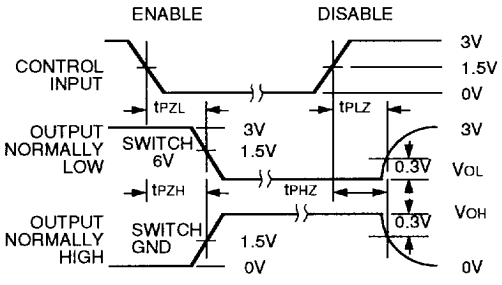
ENABLE AND DISABLE TIMES



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NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
3. If V_{CC} is below 3V, input voltage swings should be adjusted not to exceed V_{CC}.

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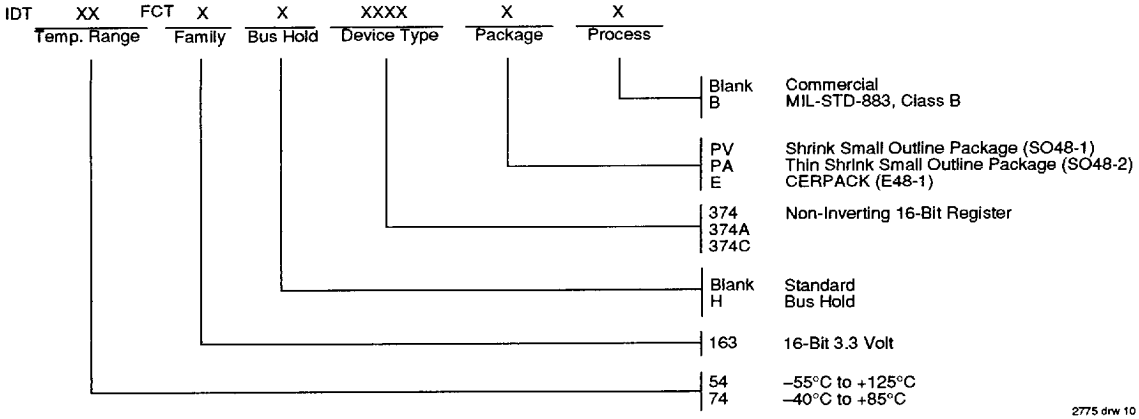
ORDERING INFORMATION



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