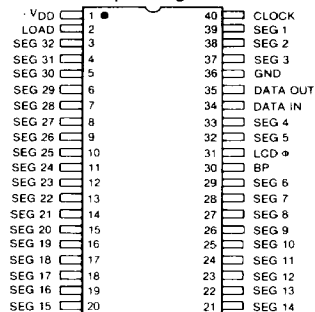


**MICROELECTRONICS CENTER**

Hughes H0438A is available in a 40 lead hermetic dual-in-line ceramic package (D suffix), plastic package (P suffix), cerdip (Y suffix), leadless chip carrier (L suffix), or surface mount quad package (Q suffix). Devices in chip form (H suffix) are available upon request. Commercial (HC prefix), Industrial (HI prefix) and Military (HB prefix) versions are available. The device designation, for example, of an industrial grade 0438A in a surface mount quad package is: HI0438A-Q.

- Drives up to 32 LCD segments of arbitrary configuration
- CMOS construction for:
  - Wide supply voltage range
  - Low power operation
  - High noise immunity
  - Wide temperature range
- CMOS, NMOS, and T<sup>2</sup>L compatible inputs
- Cascadable
- On-chip oscillator
- Requires only 3 control lines



## ABSOLUTE MAXIMUM RATINGS

V <sub>DD</sub>	−3 to +13V
Inputs (Clk, Data In, Load)	V <sub>SS</sub> −0.3V to V <sub>DD</sub> + 0.3V
LCD <sub>φ</sub> Input	−3V to + V <sub>DD</sub> + .3V
Power Dissipation	250mW
Operating Temperature	
Plastic Package	−40 to +85°C
Ceramic Package	−55 to +125°C
Storage Temperature	−65 to +150°C

NOTE: Operating the device above the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS at T<sub>A</sub> = −55 to 125°C, V<sub>DD</sub> = 5v unless otherwise stated, C<sub>L</sub> = 50pF

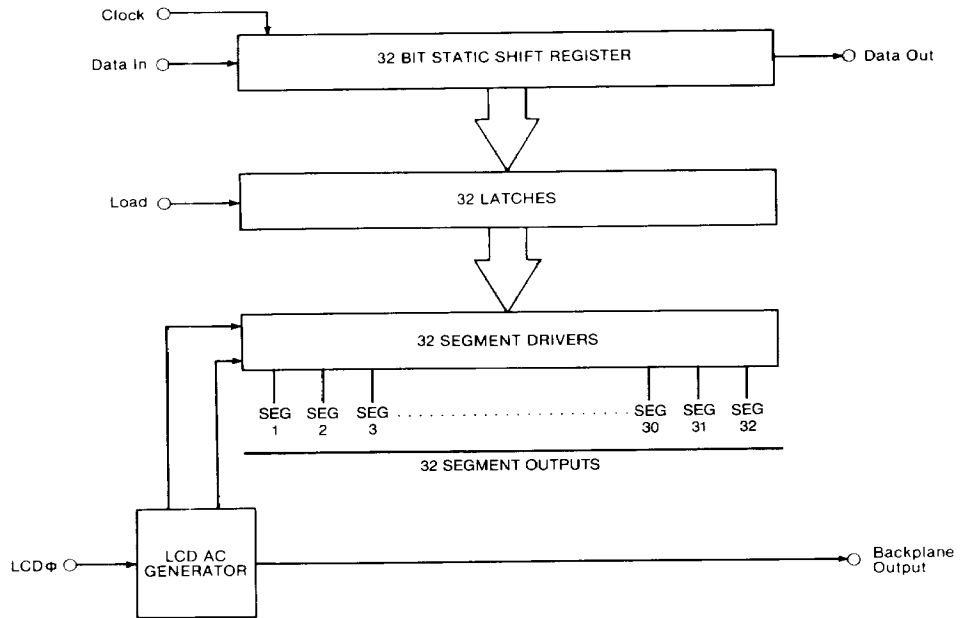
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNITS
Supply Voltage	V <sub>DD</sub>		3	10	V
Supply Current <sup>2</sup>	I <sub>DD1</sub>	LCD <sub>φ</sub> Osc < 15 KHz, V <sub>DD</sub> = 5v		60	μA
		V <sub>DD</sub> = 12v		600	μA
Quiescent Current <sup>2</sup>	I <sub>Q</sub>	V <sub>DD</sub> = 5v		40	μA
		V <sub>DD</sub> = 10v		265	μA
Input High Level	V <sub>IH</sub>		0.5V <sub>DD</sub>	V <sub>DD</sub>	V
Input Low Level	V <sub>IL</sub>		V <sub>DD</sub> · 13	0.2V <sub>DD</sub>	V
Input Current <sup>2</sup>	I <sub>L</sub>	V <sub>DD</sub> = 5v		20	μA
Input Capacitance <sup>1</sup>	C <sub>I</sub>			5	pF
Segment Output Impedance <sup>2</sup>	R <sub>ON</sub>	I <sub>L</sub> = 10μA		60	KΩ
Backplane Output Impedance <sup>2</sup>	R <sub>ON</sub>			4	KΩ
Data-Out Output Impedance <sup>2</sup>	R <sub>ON</sub>			4	KΩ
Clock Rate	f	50% Duty Cycle, V <sub>DD</sub> = 10v	DC	1.0	MHz
Data Set-up Time	t <sub>DS</sub>	Data change to Clk falling edge, V <sub>DD</sub> = 10v	210		ns
Data Hold Time	t <sub>DH</sub>	V <sub>DD</sub> = 10v	70		ns
Load Pulse Width	t <sub>PW</sub>	V <sub>DD</sub> = 10v	245		ns
Data Out Prop. Delay	t <sub>PD</sub>	C <sub>L</sub> = 50pF, V <sub>DD</sub> = 10v		700	ns
LCD <sub>φ</sub> Input High Level <sup>2</sup>	V <sub>IH</sub>		0.9V <sub>DD</sub>		V
LCD <sub>φ</sub> Input Low Level <sup>2</sup>	V <sub>IL</sub>			0.1V <sub>DD</sub>	V
LCD <sub>φ</sub> Input Current Level <sup>2</sup>	I <sub>L</sub>	Driven		20	μA
LCD <sub>φ</sub> Capacitor (external) <sup>1</sup>	C <sub>φ</sub>	30 HZ		40 (approx)	pF
LCD <sub>φ</sub> Resistor (internal) <sup>1</sup>	R <sub>φ</sub>			1	MΩ

NOTE 1: Design assured but not tested.

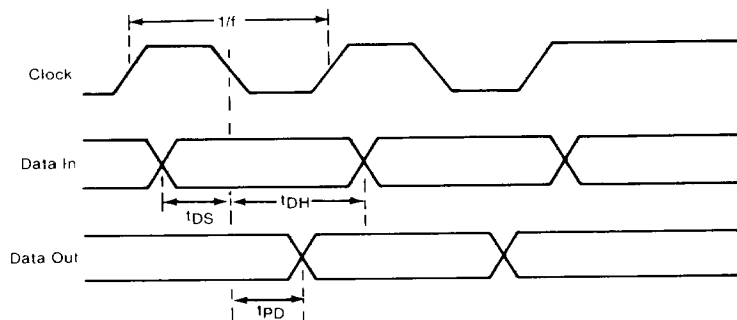
NOTE 2: Parameters guaranteed by other tests at −55°C.

# BLOCK DIAGRAM

H0438A



# TIMING DIAGRAM



## OPERATING NOTES

1. The shift register loads, shifts, and outputs on the falling edge of Clock.
2. A logic 1 on Data In causes a segment to be visible.
3. A logic 1 on Load causes a parallel load of the data in the shift register into latches that control the segment drivers. The Load control is level sensitive and not edge sensitive.
4. If  $LCD_{\phi}$  is driven, it is in phase with the Backplane Output.
5. To cascade units, either connect Backplane of one circuit to  $LCD_{\phi}$  of all other circuits (thus one capacitor provides frequency control for all circuits) or connect  $LCD_{\phi}$  of all circuits to a common driving signal. If the former is chosen, tie just one Backplane to the LCD and use a different Backplane output to drive the  $LCD_{\phi}$  inputs. Either the data can be loaded to all circuits in parallel or Data Out can be connected to Data In to form a long serial shift register.
6. The supply voltage of the H0438A is equal to half the peak driving voltage of the LCD. If the H0438A supply voltage is less than the swing of the controlling logic signals, the positive supply leads of the logic circuitry and the H0438A should be tied in common, not the ground (or negative) supply leads. Be careful that input level specifications are met.
7. The  $LCD_{\phi}$  pin can be used in two modes, driven or oscillating. If  $LCD_{\phi}$  is driven, the circuit will sense this condition and pass the  $LCD_{\phi}$  input to the Backplane output. If the  $LCD_{\phi}$  pin is allowed to oscillate, its frequency is inversely proportional to capacitance (see Figure 1) and the LCD driving waveforms have a frequency  $2^8$  slower than the oscillator itself. The frequency is nearly independent of supply voltage. If  $LCD_{\phi}$  is oscillating, it is important to keep coupling capacitance to backplane and segments as low as possible. Similarly, it is recommended that the load capacitance on  $LCD_{\phi}$  be as large as is practical.
8. There are two obvious signal races to be avoided in this circuit, (1) changing Data In when Clock is falling, and (2) changing Load when Clock is falling.
9. The number of a segment corresponds to how many clock pulses have occurred since its data was present at the input. For example, the data on Seg 19 was input 19 clock pulses earlier.
10. It is acceptable to tie the Load line high. In this case the latches are transparent. Also, remote control would only require two signal lines, Clock and Data In.

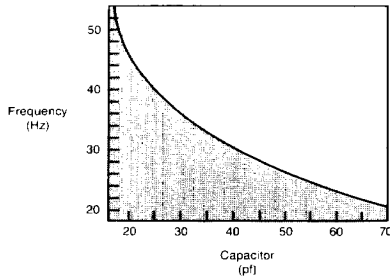


Figure 1

Information furnished by Hughes is believed to be accurate and reliable. However, no responsibility is assumed by Hughes for its use, nor for any infringements or patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Hughes.

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