National Semiconductor

DM54S196/DM74S196, DM54S197/DM74S197 Presettable Decade and Binary Counters

General Description

These high-speed counters consist of four d-c coupled, master-slave flip-flops which are internally interconnected to provide either a divide-by-two and a divide-by-five counter (S196) or a divide-by-two and a divide-by-eight counter (S197). These counters are fully programmable; that is, the outputs may be preset to any state by placing a low on the count/load input and entering the desired data at the data inputs. The outputs will change independent of the state of the clocks.

During the count operation, transfer of information to the outputs occurs on the negative-going edge of the clock pulse. These counters feature a direct clear which, when taken low, sets all outputs low regardless of the state of the clocks.

These counters may also be used as 4-bit latches by using the count/load input as the strobe and entering data at the data inputs. The outputs will directly follow the data inputs when the count/load is low, but will remain unchanged when the count/load is high and the clock inputs are inactive. (Continued)

Features

- Performs BCD, bi-quinary, or binary counting
- Fully programmable
- Fully independent clear input
- Output Q_A maintains full fan-out capability in addition to driving clock-2 input
- Typical count frequency
  - Clock 1 100 MHz
  - Clock 2 50 MHz
- Typical power dissipation 375 mW

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

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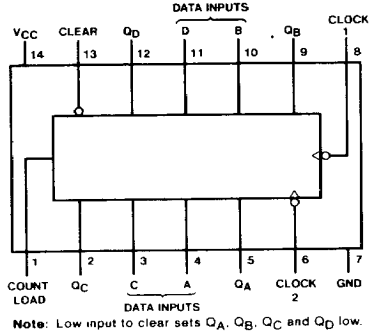
Connection Diagram

Dual-In-Line Package



Note: Low input to clear sets Q_A, Q_B, Q_C and Q_D low.

TL/F/6477-1

54S196 (J) 74S196 (N)
54S197(J) 74S197 (N)

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General Description (Continued)

TYPICAL COUNT CONFIGURATIONS S196

The output of flip-flop A is not internally connected to the succeeding flip-flops; therefore, the count may be operated in three independent modes:

1. When used as a BCD decade counter, the clock-2 input must be externally connected to the Q_A output. The clock-1 input receives the incoming count, and a count sequence is obtained in accordance with the BCD count sequence truth table.
2. If a symmetrical divide-by-ten count is desired for frequency synthesizers (or other applications requiring division of a binary count by a power of ten), the Q_D output must be externally connected to the clock-1 input. The input count is then applied at the clock-2 input and a divide-by-ten square wave is obtained at output Q_A in accordance with the bi-quinary truth table.
3. For operation as a divide-by-two counter and a divide-by-five counter, no external interconnections are required. Flip-flop A is used as a binary element for the divide-by-two function. The clock-2 input is used to obtain binary divide-by-five operation at the Q_B, Q_C, and Q_D outputs. In this mode, the two counters operate independently; however, all four flip-flops are loaded and cleared simultaneously.

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The output of flip-flop A is not internally connected to the succeeding flip-flops; therefore the counter may be operated in two independent modes:

1. When used as a high-speed 4-bit ripple-through counter, output Q_A must be externally connected to the clock-2 input. The input count pulses are applied to the clock-1 input. Simultaneous divisions by 2, 4, 8, and 16 are performed at the Q_A, Q_B, Q_C, and Q_D outputs as shown in the truth table.
2. When used as a 3-bit ripple-through counter, the input count pulses are applied to the clock-2 input. Simultaneous frequency divisions by 2, 4, and 8 are available at the Q_B, Q_C, and Q_D outputs. Independent use of flip-flop A is available if the load and clear functions coincide with those of the 3-bit ripple-through counter.

Function Tables

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Decade (BCD)
(See Note A)

Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

H = High Level, L = Low Level

Note A: Output Q_A connected to clock-2 input.
Note B: Output Q_D connected to clock-1 input.

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(See Note B)

Count	Output			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

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(See Note A)

Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

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Recommended Operating Conditions (See Section 1 for Test Waveforms and Output Load)

Sym	Parameter		DM54S196, S197			DM74S196, S197			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−1			−1	mA
I_{OL}	Low Level Output Current				20			20	mA
f_{CLK}	Clock Frequency (Note 2)		0	140	100	0	140	100	MHz
f_{CLK}	Clock Frequency (Note 3)		0	110	80	0	110	80	MHz
t_W	Pulse Width (Note 2)	Clock1	5			5			ns
		Clock2	10			10			
		Clear	30			30			
		Load	5			5			
	Pulse Width (Note 3)	Clock1	7			7			
		Clock2	12			12			
		Clear	35			35			
		Load	7			7			
t_{SU}	Data Setup Time (Notes 1 and 2)		6↑			6↑			ns
	Data Setup Time (Notes 1 and 3)		8↑			8↑			
t_H	Data Hold Time (Notes 1 and 2)		3↑			3↑			ns
	Data Hold Time (Notes 1 and 3)		5↑			5↑			
t_{EN}	Count Enable Time (Note 2 and 4)		12			12			ns
t_{EN}	Count Entable Time (Note 3 and 4)		14			14			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: The symbol (↑) indicates the rising edge of the clock pulse is used for reference.

Note 2: $C_L = 15$ pF and $R_L = 280\Omega$.

Note 3: $C_L = 50$ pF and $R_L = 280\Omega$.

Note 4: Count enable time is the interval immediately preceding the negative-going edge of the clock pulse during which the COUNT/LOAD and CLEAR inputs must both be high to ensure counting.

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'S196 Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max (Note 4)				0.5	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V	Clock1			−8	mA
			Clock2			−10	
			Others			−0.75	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			75	110	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all inputs grounded and all outputs open.

Note 4: Q_A outputs are tested at I_{OL} = max plus the limit value of I_{IL} for the CLOCK2 input. This permits driving the CLOCK2 input while maintaining full fan-out capability.

'S196 Switching Characteristics at V_{CC} = 5V and T_A = 25°C

(See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	R_L = 280Ω						Units
		C_L = 15 pF			C_L = 50 pF			
		Min	Typ	Max	Min	Typ	Max	
f_{MAX} Maximum Clock Frequency	Clock1 to Q_A	100	140		80	110		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Clock1 to Q_A		5	10		7	11	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock1 to Q_A		6	10		8	12	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock2 to Q_B		5	10		7	11	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock2 to Q_B		8	12		10	15	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock2 to Q_C		12	18		14	21	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock2 to Q_C		16	24		18	27	ns

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'S196 Switching Characteristics (Continued) at $V_{CC} = 5V$ and $T_A = 25°C$

(See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 280\Omega$						Units
		$C_L = 15$ pF			$C_L = 50$ pF			
		Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	Clock2 to Q_D		5	10		7	11	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock2 to Q_D		8	12		10	15	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Data to Any Q		7	12		9	14	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Data to Any Q		12	18		14	21	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Load to Any Q		10	18		12	18	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Load to Any Q		12	18		14	21	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Any Q		26	37		30	45	ns

'S197 Electrical Characteristics over recommended operating free air temperature

(unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	$V_{CC} = Min$, $I_I = -18$ mA				−1.2	V
V_{OH}	High Level Output Voltage	$V_{CC} = Min$, $I_{OH} = Max$, $V_{IL} = Max$, $V_{IH} = Min$	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	$V_{CC} = Min$, $I_{OL} = Max$, $V_{IH} = Min$, $V_{IL} = Max$ (Note 4)				0.5	V
I_I	Input Current@Max Input Voltage	$V_{CC} = Max$, $V_I = 5.5V$				1	mA
I_{IH}	High Level Input Current	$V_{CC} = Max$, $V_I = 2.7V$				50	μA
I_{IL}	Low Level Input Current	$V_{CC} = Max$, $V_I = 0.5V$	Clock1			−8	mA
			Clock2			−6	
			Others			−0.75	
I_{OS}	Short Circuit Output Current	$V_{CC} = Max$ (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CC}	Supply Current	$V_{CC} = Max$ (Note 3)			75	110	mA

Note 1: All typicals are at $V_{CC} = 5V$, $T_A = 25°C$.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all inputs grounded and all outputs open.

Note 4: Q_A outputs are tested at I_{OL} = max plus the limit value of I_{IL} for the CLOCK2 input. This permits driving the CLOCK2 input while maintaining full fan-out capability.

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'S197 Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$

(See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 280\Omega$						Units
		$C_L = 15$ pF			$C_L = 50$ pF			
		Min	Typ	Max	Min	Typ	Max	
f_{MAX} Maximum Clock Frequency	Clock1 to QA	100	140		80	110		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Clock1 to Q_A		5	10		7	11	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock1 to Q_A		6	10		8	12	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock2 to Q_B		5	10		7	11	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock2 to Q_B		8	12		10	15	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock2 to Q_C		12	18		14	21	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock2 to Q_C		15	22		17	26	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock2 to Q_D		18	27		20	30	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock2 to Q_D		22	33		25	38	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Data to Any Q		7	12		9	14	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Data to Any Q		12	18		14	21	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Load to Any Q		10	18		12	18	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Load to Any Q		12	18		14	21	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Any Q		26	37		30	45	ns

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Logic Diagrams

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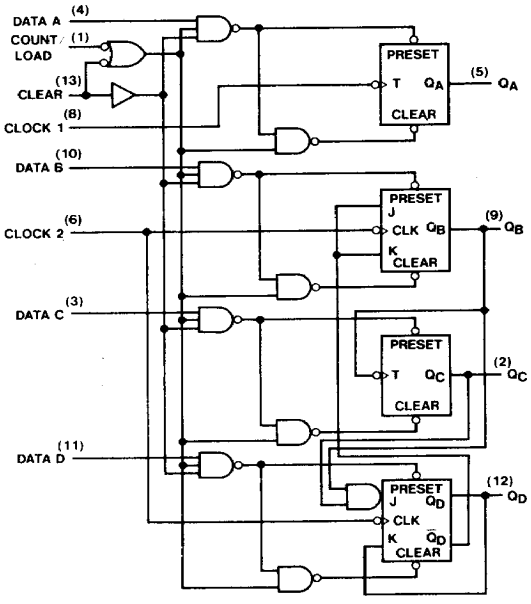

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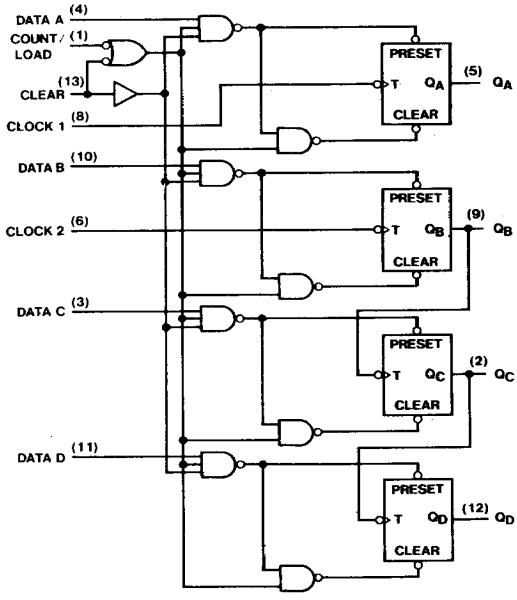

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