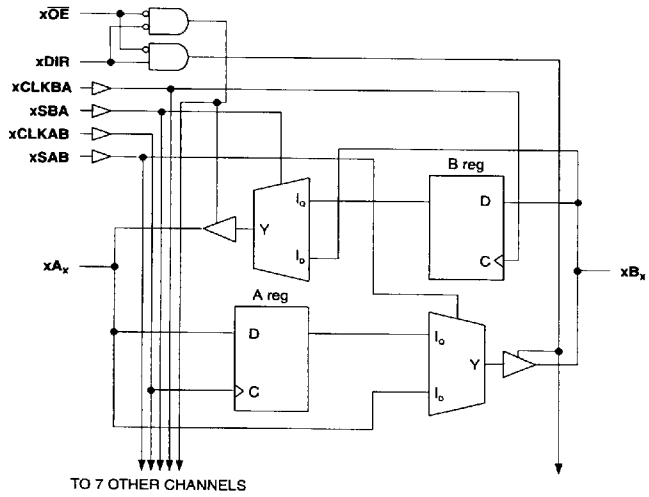
Features

- **Fastest Propagation Speeds in the Industry T_{PD} (F grade) = 2.5 ns, T_{PD} (G grade) = 2.0 ns**
- **Maximum derating for capacitive loads 1.5ns/100 pF (F grade) and 1.1ns/100 pF (G grade)**
- **Very low ground bounce < 0.6 V @ V_{CC}=5.00 V, T_a=25°C**
- **Typical output skew ≤0.25ns**
- **Bus Hold circuitry to retain last active state during Tri-State™**
- **Available in SSOP and TSSOP packages**

Description

Atmel's AT16646 devices are 16-bit high speed, low power Tri-statable D type registers, ideal for use in systems requiring both transparent and registered mode functions. They are organized as two separate 8-bit bus transceivers. Data flow is bi-directional, and can be controlled for multiplexed transmission between A bus and B bus either directly or from the D registers by use of the direction control pin (xDir), output enable ($x\overline{OE}$), and select lines (xSAB and xSBA). Storage of data on the A bus and B bus is controlled by the output pins. They have very low ground bounce and excellent input noise rejection, giving the user stable signals in a high speed environment. The Bus Hold feature eliminates the need for pull-up or pull-down resistors and retains the last active state during a Tri-State event.

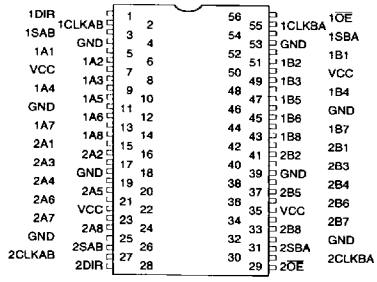
Functional Block Diagram(1)



Pin Configurations

Pin Names	Descriptions
xDir, $x\overline{OE}$	Output Enable Inputs
xCLKAB,xCLKBA	Clock Pulse Inputs
xSAB, xSBA	Output Data Source Select Inputs
xAχ	Data Register A Inputs Data Register B Outputs
xBχ	Data Register B Inputs Data Register A Outputs

SSOP/TSSOP



Top View

Function Table[1]

Inputs						Data I/O[2]		Operation or Function
$\overline{xOE}$	xDir	xCLKAB	xCLKBA	xSAB	xSBA	xAχ	xBχ	
H H	X X	H or L ↑	H or L ↑	X X	X X	Input	Input	Isolation Store A and B Data
L L	L L	X X	X H or L	X X	L H	Output	Input	Real Time B Data to A Bus Stored B Data to A Bus
L L	H H	X H or L	X X	L H	X X	Input	Output	Real Time A Data to B Bus Stored A Data to B Bus

Notes: 1. H = High voltage level, L = Low voltage level, X = Don't care, ↑ = Low-to-High transition
2. The data output functions may be enabled or disabled by various signals at the $\overline{xOE}$ or xDir inputs. Data input functions are always enabled, i.e. data at the bus pins will be stored on every LOW-to-HIGH transition on the clock inputs.

Absolute Maximum Ratings*

Operating Temperature	0°C to +70°C
Storage Temperature	-65°C to +150°C
Voltage on any Pin with Respect to Ground	-2.0 V to +7.0 V[1]
Maximum Operating Voltage	6.0V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:1.Minimum voltage is -0.6 V dc which may undershoot to -2.0 V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} +0.75 V dc which may overshoot to +7.0 V for pulses of less than 20 ns.

5.0 Volt DC Characteristics

Applicable over recommended operating range from T_a = 0°C to +70°C, V_{CC} = +5.0V +/- 5% (unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
ΔI_{CC}	Quiescent Power Supply Current	V_{CC} = Max, V_{IN} = 3.4 V		0.8	1.2	mA
V_{IH}	Input High Voltage		2.0			V
V_{IL}	Input Low Voltage				0.8	
I_{IH}	Input High Current (I/O Pins)	V_{IN} = V_{CC}			±15	µA
I_{IL}	Input Low Current (I/O Pins)	V_{IN} = GND			±15	µA
I_{OZ}	Output Leakage Current				±10	µA
V_{OH} (1)	Output High Voltage F Grade only	V_{CC} = 4.75 V I_{OH} = -10 mA	2.7			V
V_{OH} (2)	Output High Voltage G Grade only	V_{CC} = 4.75 V I_{OH} = -12 mA	2.7			V
V_{OL}	Output Low Voltage (F Grade)	I_{OL} = 10 mA			0.55	V
V_{OL}	Output Low Voltage (G Grade)	I_{OL} = 12 mA			0.55	V

Note: 1.F grade: At $V_{CC\ (max)}$, the value of $V_{OH(max)}$ = 3.75 V and at $V_{CC(min)}$, $V_{OH(max)}$ = 3.25 V
2. G grade: At $V_{CC\ (max)}$, the value of $V_{OH(max)}$ = 3.75 V and at $V_{CC(min)}$, $V_{OH(max)}$ = 3.35 V

AC Characteristics
AT16646F

Applicable over recommended operating range from T_a = 0°C to +70°C, V_{CC} = 5.0V +/- 5% (unless otherwise noted)

Symbol	Parameter	Test Conditions[1]	Min	Typ	Max	Units
t_{PHL} t_{PLH}	Propagation Delay	CL = 50 pF			2.5	ns
t_{PZH} t_{PZL}	Output Enable Time	CL = 50 pF			7.4	ns
t_{PHZ} t_{PLZ}	Output Disable Time	CL = 50 pF			6.4	ns
t_{SK} (1)	Output Skew	CL = 50 pF			0.5	ns
Δt_{PHL} (1) Δt_{PLH}	Propagation Delay vs Output Loading			1.3	1.5	ns/100 pF
t_{su}	Set-up Time Bus to Clock	CL = 50 pF	2.0			ns
t_H	Hold Time Bus to Clock	CL = 50 pF	2.0			n

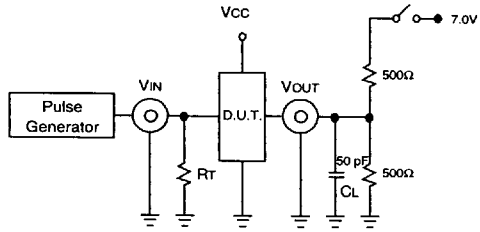
AT16646G

Applicable over recommended operating range from T_a = 0°C to +70°C, V_{CC} = 5.0V +/- 5% (unless otherwise noted)

Symbol	Parameter	Test Conditions[1]	Min	Typ	Max	Units
t_{PHL} t_{PLH}	Propagation Delay	CL = 50 pF			2.0	ns
t_{PZH} t_{PZL}	Output Enable Time	CL = 50 pF			7.4	ns
t_{PHZ} t_{PLZ}	Output Disable Time	CL = 50 pF			5.8	ns
t_{SK} (1)	Output Skew	CL = 50 pF			0.5	ns
Δt_{PHL} (1) Δt_{PLH}	Propagation Delay vs Output Loading			0.9	1.1	ns/100 pF
t_{su}	Set-up Time Bus to Clock	CL = 50 pF	2.0			ns
t_H	Hold Time Bus to Clock	CL = 50 pF	2.0			n

Note:1.This parameter is guaranteed but not 100% tested.

Test Circuits[1,2]



Note:1.Pulse Generator: Rate ≤ 1.0 MHz, $t_F \leq 2.5$ ns, $t_R \leq 2.5$ ns.

2.AC tests are done with a single bit switching, and timings need to be derated when multiple outputs are switching in the same direction simultaneously. This derat-

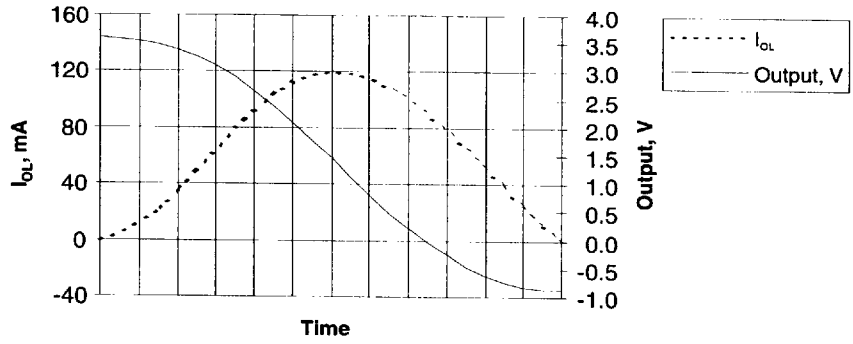
Switch Position

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

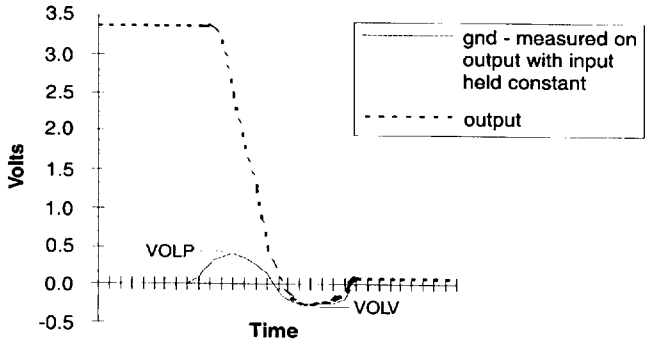
Definitions:

C_L = Load capacitance; Includes jig and probe capacitance.

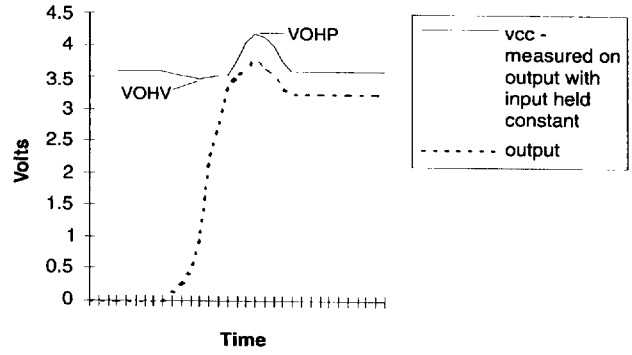
IOL Pull Down Current



Ground Bounce for High to Low Transitions(1)



Supply Bounce for Low to High Transitions(2)



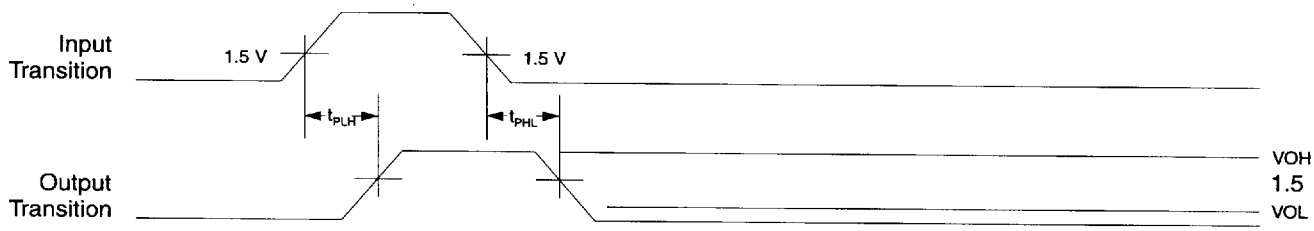
Typical Values

Parameter	Value	Units
V_{OLP}	0.4	V
V_{OLV}	-0.26	V
V_{OHV}	V_{CC} - 0.13	V
V_{OHP}	V_{CC} + 0.6	V

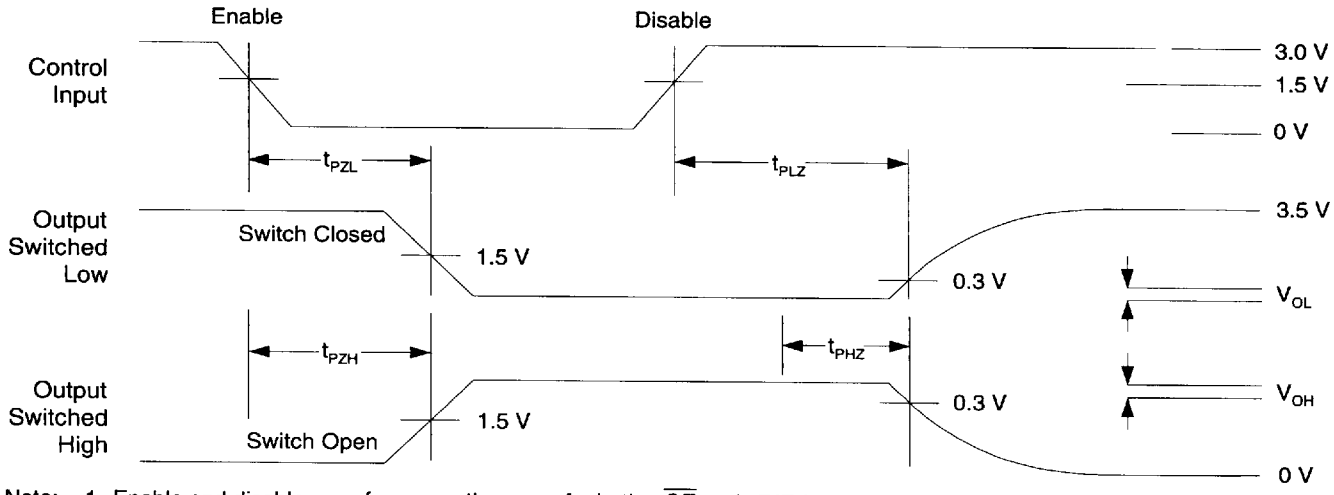
Note: 1. When multiple outputs are switched at the same time, rapidly changing current on the ground and V_{CC} path causes a voltage to develop across the parasitic inductance of the wire bond and package pins. This occurrence is called simultaneous switching noise. Atmel's AT16646 products have minimized this phenomenon as shown on the graph. Output data is for 15 outputs switching simultaneously at a frequency of 1 MHz. The ground data is measured on the one remaining output, which is set to logic low and will reflect any device ground movement.

2. As on the graph for Ground Bounce, a similar condition occurs for low to high transitions. Output data is for 15 outputs switching simultaneously at a frequency of 1 MHz. V_{CC} droop is measured on the one remaining output pin, which is set to a logic high. This output will reflect any movement on the device V_{CC}.

Propagation Delay Waveforms



Enable and Disable Waveforms[1]



Note: 1. Enable and disable waveforms are the same for both $x\overline{OE}$ and xDIR inputs.

Ordering Information

T_{PD}	Ordering Code	Package	Operation Range
2.5 ns	AT16646F - 25YC AT16646F - 25XC	56Y 56X	Commercial
2.0 ns	AT16646G -25YC AT16646G - 25XC	56Y 56X	Commercial

Package Type	
56X	56 Pin, Plastic thin shrink small outline package (TSSOP)
56Y	56 Pin, Plastic shrink small outline package (SSOP)