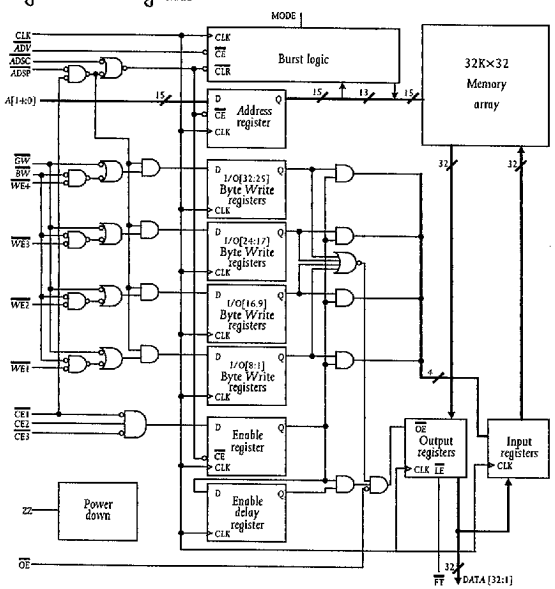
32K×32 Synchronous burst SRAM

Preliminary information

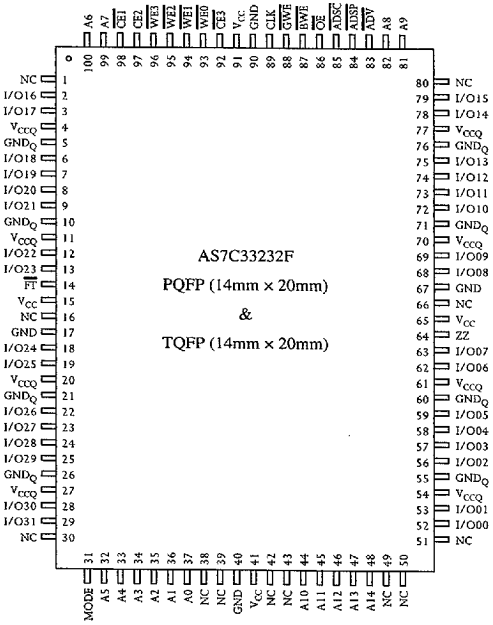
Features

- Organization: 32,768 words × 32 bits
- Fully synchronous pipelined operation
- Flow-through or pipelined
- Fast clocking speed: 100/75/66 MHz
- Fast clock to data access: 5.5/6/7 ns
- Self-timed write cycle
- On-chip address, control, and data registers
- Byte write enable & global write enable control
- Asynchronous output enable control
- $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$, MODE burst control pins
- Pentium™ or PowerPC™ count sequence
- Transparent logic support for 1 or 2 CPUs
- Single 3.3 ± 0.3V power supply
- 5V safe inputs
- ESD protection ≥ 2000 volts
- Latch-up current ≥ 200 mA

Logic block diagram



Pin arrangement



Selection guide

	7C33232F-5	7C33232F-6	7C33232F-7	Unit
Minimum cycle time	10	13.3	15	ns
Maximum clock frequency	100	75	66	MHz
Maximum pipelined clock access time	5.5	6	7	ns
Maximum operating current	300	275	250	mA
Maximum standby current	30	30	30	mA
Maximum CMOS standby current (DC)	6	6	6	mA

SRAM

Functional description

The AS7C33232F is a high performance CMOS 1 Mbit synchronous Static Random Access Memory (SRAM) organized as 32,768 words × 32 bits and incorporates a 2-bit burst counter and output register. It is designed for high performance 3.3V Pentium,™ Cyrix, and PowerPC™ cache applications.

Fast cycle times of 10/13/15 ns with clock access times (t_{OE}) of 5.5/6/7 ns are ideal for 100, 75, and 66 MHz bus frequencies. Three chip enable inputs permit easy memory expansion. Burst operation is initiated in one of two ways: the controller address strobe ($\overline{ADSC}$), or the processor address strobe ($\overline{ADSP}$). The burst advance pin ($\overline{ADV}$) allows subsequent internally generated burst addresses.

Read cycles are initiated with $\overline{ADSP}$ (regardless of $\overline{WE}$ and $\overline{ADSC}$) using an address that is clocked into the on-chip address register when $\overline{ADSP}$ is sampled Low, the chip enables are sampled active, and the output buffer is enabled with $\overline{OE}$. In a read operation the data accessed by the current address, registered in the address registers by the positive edge of CLK, are carried to the data-out registers and driven on the output pins on the next positive edge of CLK. $\overline{ADV}$ is ignored on the clock edge that samples $\overline{ADSP}$ asserted, but is sampled on all subsequent clock edges. Address is incremented internally for the next access of the burst when $\overline{WE}$ is sampled High, $\overline{ADV}$ is sampled Low, and both address strobes are High. Burst operation is selectable with the MODE input. With MODE unconnected or driven High, burst operations use a Pentium/486 count sequence. With MODE driven Low the device uses a linear count sequence, suitable for PowerPC and other applications (refer to the Burst sequence table on page 140).

Write cycles are performed by disabling the output buffers with $\overline{OE}$ and asserting $\overline{WE}$. A global write enable $\overline{GWE}$ writes all 32 bits regardless of the state of individual $\overline{WE0}$–$\overline{WE3}$ inputs. Alternately, when $\overline{GWE}$ is High, one or more bytes may be written by asserting $\overline{BWE}$ and the appropriate individual byte $\overline{WE}$ signal(s). $\overline{WE0}$ controls I/O0-I/O7; $\overline{WE1}$ controls I/O8-I/O15; $\overline{WE2}$ controls I/O16-I/O23; and $\overline{WE3}$ controls I/O24-I/O31.

$\overline{WE}$ is ignored on the clock edge that samples $\overline{ADSP}$ Low, but is sampled on all subsequent clock edges. Output buffers are disabled when $\overline{WE}$ is sampled Low (regardless of $\overline{OE}$). Data is clocked into the data input register when $\overline{WE}$ is sampled Low. Address is incremented internally to the next burst of address if $\overline{WE}$ and $\overline{ADV}$ are sampled Low.

Read or write cycles may also be initiated with $\overline{ADSC}$ instead of $\overline{ADSP}$. The differences between cycles initiated with $\overline{ADSC}$ and $\overline{ADSP}$ follow.

- $\overline{ADSP}$ must be sampled High when $\overline{ADSC}$ is sampled Low to initiate a cycle with $\overline{ADSC}$.
- $\overline{WE}$ signals are sampled on the clock edge that samples $\overline{ADSC}$ Low (and $\overline{ADSP}$ High).
- Master chip select $\overline{CE1}$ blocks $\overline{ADSP}$, but not $\overline{ADSC}$.

The AS7C33232F incorporates a flow-through feature which makes the output registers transparent. Tying the $\overline{FT}$ pin low enables flow-through mode and disables pipelined operation. The ZZ sleep mode reduces power consumption in standby mode. The AS7C33232 operates from a single 3.3V±0.3V supply and is packaged in a 100-pin 14×20 mm PQFP or TQFP package.

Write enable truth table (per byte)

$\overline{GWE}$	$\overline{BWE}$	$\overline{WE}$n	WRITEn
L	X	X	T
X	L	L	T
H	H	X	F
H	L	H	F †

Key: X = Don't Care, L = Low, H = High.

† Valid read.

Asynchronous truth table

$\overline{OE}$	I/O [31:0]
L	Read data
H	High Z

Note: For write cycles that follow read cycles, output buffers must be disabled with $\overline{OE}$ to prevent data bus contention.

Key: L = Low, H = High.

Burst sequence table

	Mode = High/No connect Pentium count sequence				Mode = Low Linear count sequence			
Start address	00	01	10	11	00	01	10	11
Second address	01	00	11	10	01	10	11	00
Third address	10	11	00	01	10	11	00	01
Fourth address	11	10	01	00	11	00	01	10

Note: The burst sequence wraps around to its initial state upon completion.

Signal descriptions

Signal	I/O	properties	Description
CLK	I	CLOCK	Clock. All inputs except $\overline{OE}$ are synchronous to this clock.
A0–A14	I	SYNC	Address. Sampled when all chip enables are active and $\overline{ADSC}$ or $\overline{ADSP}$ are asserted.
I/O0–I/O31	I/O	SYNC	Data. Driven as output when the chip is enabled and $\overline{OE}$ is active.
$\overline{CE1}$	I	SYNC	Master chip enable. Sampled on clock edges when $\overline{ADSP}$ or $\overline{ADSC}$ is active. When $\overline{CE1}$ is inactive, $\overline{ADSP}$ is blocked. Refer to the SYNCHRONOUS TRUTH TABLE for more information.
CE2, $\overline{CE3}$	I	SYNC	Synchronous chip enables. Active High and active Low, respectively. Sampled on clock edges when $\overline{ADSC}$ is active or when $\overline{CE1}$ and $\overline{ADSP}$ are active.
$\overline{ADSP}$	I	SYNC	Address strobe processor. Asserted Low to load a new bus address or to enter standby mode.
$\overline{ADSC}$	I	SYNC	Address strobe controller. Asserted Low to load a new address or to enter standby mode.
$\overline{ADV}$	I	SYNC	Advance. Asserted Low to continue burst read/write.
$\overline{GWE}$	I	SYNC default = High	Global write enable. Asserted Low to write all 32 bits. When High, $\overline{BWE}$ and $\overline{WE0}$–$\overline{WE3}$ control write enable. *This signal is internally pulled High.*
$\overline{BWE}$	I	SYNC default = Low	Byte write enable. Asserted Low with $\overline{GWE}$ = High to enable effect of $\overline{WE0}$–$\overline{WE3}$ inputs. *This signal is internally pulled Low.*
$\overline{WE0}$–$\overline{WE3}$	I	SYNC	Write enables. Used to control write of individual bytes when $\overline{GWE}$ = High and $\overline{BWE}$ = Low. If any of $\overline{WE0}$–$\overline{WE3}$ is active with $\overline{GWE}$ = High and $\overline{BWE}$ = Low the cycle is a write cycle. If all $\overline{WE0}$–$\overline{WE3}$ are inactive the cycle is a read cycle.
$\overline{OE}$	I	ASYNC	Asynchronous output enable. I/O pins are driven when $\overline{OE}$ is active and the chip is synchronously enabled.
MODE	I	STATIC default = High	Burst count mode. When driven High, count sequence follows Intel XOR convention. When driven Low, count sequence follows Motorola/linear convention. *This signal is internally pulled High.*[18]
$\overline{FT}$	I	STATIC	Flow-through mode.When low, enables flow-through mode. Connect to V_{CC} if unused or for pipelined operation.
ZZ	I	ASYNC	Sleep. Places device in low power mode; data is retained. Connect to GND if unused.[19]

Absolute maximum ratings

Parameter	Symbol	Min	Max	Unit
Power supply voltage relative to GND	V_{CC}	−0.5	+4.6	V
Input voltage relative to GND (input pins)	V_{IN}	−0.5	+6.0	V
Input voltage relative to GND (I/O pins)	V_{IN}	−0.5	V_{CC}+0.5	V
Power dissipation	P_D	–	1.2	W
DC output current	I_{OUT}	–	30	mA
Storage temperature (plastic)	T_{stg}	−65	+150	°C
Temperature under bias	T_{bias}	−65	+135	°C

NOTE: Stresses greater than those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect reliability.

Capacitance [1]

Parameter	Symbol	Signals	Test conditions	Max	Unit
Input capacitance	C_{IN}	Address and control pins, MODE, ZZ	V_{in} = 0V	5	pF
I/O capacitance	$C_{I/O}$	I/O pins	V_{in} = V_{out} = 0V	7	pF

Synchronous truth table

$\overline{CE1}$	CE2	$\overline{CE3}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	WRITEn†	$\overline{OE}$	Address accessed	CLK	Operation
H	X	X	X	L	X	X	X	NA	L to H	Deselect
L	L	X	L	X	X	X	X	NA	L to H	Deselect
L	L	X	H	L	X	X	X	NA	L to H	Deselect
L	X	H	L	X	X	X	X	NA	L to H	Deselect
L	X	H	H	L	X	X	X	NA	L to H	Deselect
L	H	L	L	X	X	F	L	External	L to H	Begin read
L	H	L	L	X	X	F	H	External	L to H	Begin read
L	H	L	H	L	X	F	L	External	L to H	Begin read
L	H	L	H	L	X	F	H	External	L to H	Begin read
X	X	X	H	H	L	F	L	Next	L to H	Cont. read
X	X	X	H	H	L	F	H	Next	L to H	Cont. read
X	X	X	H	H	H	F	L	Current	L to H	Suspend read
X	X	X	H	H	H	F	H	Current	L to H	Suspend read
H	X	X	X	H	L	F	L	Next	L to H	Cont. read
H	X	X	X	H	L	F	H	Next	L to H	Cont. read
H	X	X	X	H	H	F	L	Current	L to H	Suspend read
H	X	X	X	H	H	F	H	Current	L to H	Suspend read
L	H	L	H	L	X	T	X	External	L to H	Begin write
X	X	X	H	H	L	T	X	Next	L to H	Cont. write
H	X	X	X	H	L	T	X	Next	L to H	Cont. write
X	X	X	H	H	H	T	H	Current	L to H	Suspend write
H	X	X	X	H	H	T	H	Current	L to H	Suspend write

Key: X = Don't Care, L = Low, H = High, T = TRUE, F = FALSE.

† See write enable truth table for detailed information.

DC operating conditions

			-5		-6		-7		
Parameter	Symbol	Test conditions	Min	Max	Min	Max	Min	Max	Unit
Input leakage current*	$\lvert I_{LI} \rvert$	V_{CC} = Max, V_{in} = GND to V_{CC}	–	2	–	2	–	2	µA
Output leakage current	$\lvert I_{LO} \rvert$	$\overline{OE} \geq V_{IH}$, V_{CC} = Max, V_{out} = GND to V_{CC}	–	2	–	2	–	2	µA
Operating power supply current	I_{CC}[14]	$\overline{CE1} = V_{IL}$, CE2 = V_{IH}, $\overline{CE3} = V_{IL}$, f = f_{max}, I_{out} = 0 mA	–	300	–	275	–	250	mA
Standby power supply current	I_{SB}	Deselected, f = f_{max}	–	30	–	30	–	30	mA
	I_{SB1}	Deselected, f = 0, all $V_{IN} \leq 0.2V$ or $\geq V_{CC}$ - 0.2V	–	6	–	6	–	6	mA
	I_{SB2}	ZZ > V_{IH}	–	4	–	4	–	4	mA
Output voltage	V_{OL}	I_{OL} = 5 mA, V_{CC} = Max	–	0.4	–	0.4	–	0.4	V
	V_{OH}	I_{OH} = –5 mA, V_{CC} = Min	2.4	–	2.4	–	2.4	–	V

*FT and ZZ pins have internal pull-up and pull-down resistors, respectively, which create 150µA of input leakage; BWE, GWE, and MODE create 50µA of input leakage.

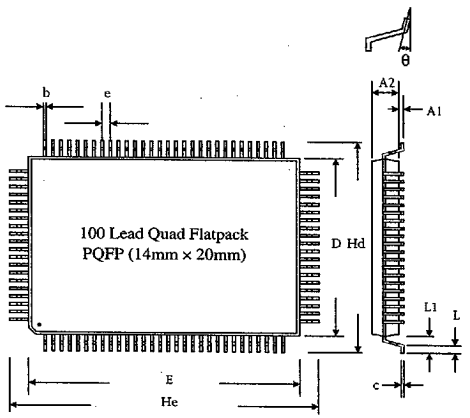
Recommended operating conditions

Applicable to all portions of this specification unless otherwise noted.

Parameter		Symbol	Min	Nominal	Max	Unit
Supply voltage		V_{CC}	3.0	3.3	3.6	V
		GND	0.0	0.0	0.0	V
I/O supply voltage		V_{CCQ}	3.0	3.3	3.6	V
		GND_Q	0.0	0.0	0.0	V
Input voltage	Address and control pins	V_{IH}	2.0	–	5.5	V
		V_{IL}	−0.5*	–	0.8	V
	I/O pins	V_{IH}	2.0	–	V_{CC}+0.5	V
		V_{IL}	-0.5*	–	0.8	
Ambient operating temperature		T_a	0	–	70	°C

* V_{IL} min = −2.0V for pulse width less than $t_{RC}/2$.

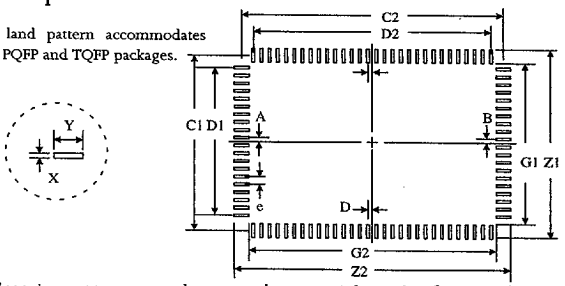
Package dimensions



	PQFP		TQFP	
	Min	Max	Min	Max
JEDEC	MO−108		MO−136	
A1	0.25	0.45	0.05	0.15
A2	2.57	2.87	1.35	1.45
b	0.20	0.40	0.22	0.38
c	0.10	0.20	0.09	0.20
D	13.90	14.10	13.90	14.10
e	0.65		0.65	
E	19.90	20.10	19.90	20.10
Hd	17.00	17.40	15.90	16.10
He	23.00	23.40	21.90	22.10
L	0.65	0.95	0.45	0.75
L1	1.60		1.00	
q	0°	10°	0°	7°

PCB land pattern

This land pattern accommodates both PQFP and TQFP packages.



Symbol	Description	TQFP/PQFP Min	Max
C1	Reference	15.98 ref.	
C2	Reference	21.98 ref.	
D1	Reference	12.35 ref.	
D2	Reference	18.85 ref.	
e	Pad pitch	0.65	
G1	Pad inner dimension	13.69	13.79
G2	Pad inner dimension	19.69	19.79
N	Pad count	100	
X	Pad width	0.35	0.38
Y	Pad length	2.24 ref.	
Z1	Pad outer dimension	18.16	18.26
Z2	Pad outer dimension	24.16	24.26

Notes

1 Pad requirement to accommodate two package types is larger than for one package type.
2 All dimensioning and tolerancing conform to ANSI Y14.5M-1982. Dimensions in mm.
3 Datums A--B and --D-- to be determined from the center two leads.
4 Based on the surface mount Design and Land Pattern Standard in IPC-SM-782 rev. A, subsection 11.3, 8/93 for PQFP.

Timing characteristics over operating range

		-5		-6		-7			
Parameter	*Symbol*	*Min*	*Max*	*Min*	*Max*	*Min*	*Max*	*Unit*	*Notes*
Cycle time (pipelined mode)	t_{CYC}	10	-	13	-	15	-	ns	
Clock access time (pipelined mode)	t_{CD}	-	5.5	-	6	-	7	ns	
Cycle time (flow-through mode)	t_{CYC}	14	-	18	-	20	-	ns	
Clock access time (flow-through mode)	t_{CDF}	-	14	-	18	-	20	ns	
Output enable to data valid	t_{OE}	-	4	-	5	-	6	ns	3
Clock High to output Low-Z	t_{LZC}	2	-	2	-	2	-	ns	5, 8, 15
Output hold from clock High	t_{OH}	2	-	2	-	2	-	ns	5, 8
Output enable Low to output Low-Z	t_{LZOE}	2	-	2	-	2	-	ns	5, 8, 15
Output enable High to output High Z	t_{HZOE}	-	4.5	-	5	-	6	ns	5, 8, 15
Clock High to output High Z	t_{HZC}	-	4.5	-	5	-	6	ns	5, 8, 15
Clock High pulse width	t_{CH}	3	-	4.5	-	5.5	-	ns	
Clock Low pulse width	t_{CL}	3	-	4.5	-	5.5	-	ns	
Address setup to clock High	t_{AS}	2	-	2.5	-	2.5	-	ns	9, 10
Address strobe setup to clock High	t_{SS}	2	-	2.5	-	2.5	-	ns	9, 10
Data setup to clock High	t_{DS}	2	-	2.5	-	2.5	-	ns	9, 10
Write setup to clock High	t_{WS}	2	-	2.5	-	2.5	-	ns	9, 10
Address advance setup to clock High	t_{ADVS}	2	-	2.5	-	2.5	-	ns	9, 10
Chip select setup to clock High	t_{CSS}	2	-	2.5	-	2.5	-	ns	9, 10
Address hold from clock High	t_{AH}	0.5	-	0.5	-	0.5	-	ns	9, 10
Address status hold from clock High	t_{SH}	0.5	-	0.5	-	0.5	-	ns	9, 10
Data hold from clock High	t_{DH}	0.5	-	0.5	-	0.5	-	ns	9, 10
Write hold from clock High	t_{WH}	0.5	-	0.5	-	0.5	-	ns	9, 10
Address advance hold from clock High	t_{ADVH}	0.5	-	0.5	-	0.5	-	ns	9, 10
Chip select hold from clock High	t_{CSH}	0.5	-	0.5	-	0.5	-	ns	9, 10
Output rise time (unloaded)	t_R	1	-	1	-	1	-	V/ns	5, 1
Output fall time (unloaded)	t_F	1	-	1	-	1	-	V/ns	5, 1
ZZ High to snooze mode	t_{ZZ}	t_{CYC}	-	t_{CYC}	-	t_{CYC}	-	ns	1
Snooze mode recovery	t_{ZZR}	-	t_{CYC}	-	t_{CYC}	-	t_{CYC}	ns	1

Notes

1 This parameter is guaranteed but not tested.

2 For test conditions, see *AC Test Conditions*, Figures A, B, C.

3 $\overline{OE}$ state is "don't care" when a byte write enable is sampled Low.

4 This parameter is sampled and not 100% tested.

5 Read cycle is defined as byte write enables all High or $\overline{ADSP}$ Low for required setup and hold times. Write cycle is defined as at least one byte write enable Low and $\overline{ADSP}$ High for required setup and hold times.

6 This is a synchronous device. All addresses must meet the specified setup and hold times for all rising edges of CLK when either $\overline{ADSP}$ or $\overline{ADSC}$ is Low and chip enabled. All other synchronous inputs must meet the setup and hold times with stable logic levels for all rising edges of CLK when chip is enabled. Chip enable must be valid at each rising edge of CLK with either $\overline{ADSP}$ or $\overline{ADSC}$ Low to remain enabled.

7 Typical values measured at 3.3V, 25°C and 15 ns cycle time.

8 All voltages referenced to GND.

9 Overshoot: $V_{IH} \leq +6.0V$ for $t \leq t_{CYC}/2$
Undershoot: $V_{IL} \geq -2.0V$ for $t \leq t_{CYC}/2$
Power up: $V_{IH} \leq +6.0V$ and $V_{CC} \leq 3.1V$ for $t \leq 200$ ms

10 I_{CC} given with no output current. I_{CC} increases with faster cycle times and greater output loading.

11 Transitions are measured ±500 mV from steady state voltage. Output loading specified with C_L = 5 pF as in Figure C.

12 t_{HZOE} is less than t_{LZOE}; and t_{HZC} is less than t_{LZC} at any given temperature and voltage.

13 Deselect = device inactive, in powered-down mode. Otherwise device active (not in powered-down mode).

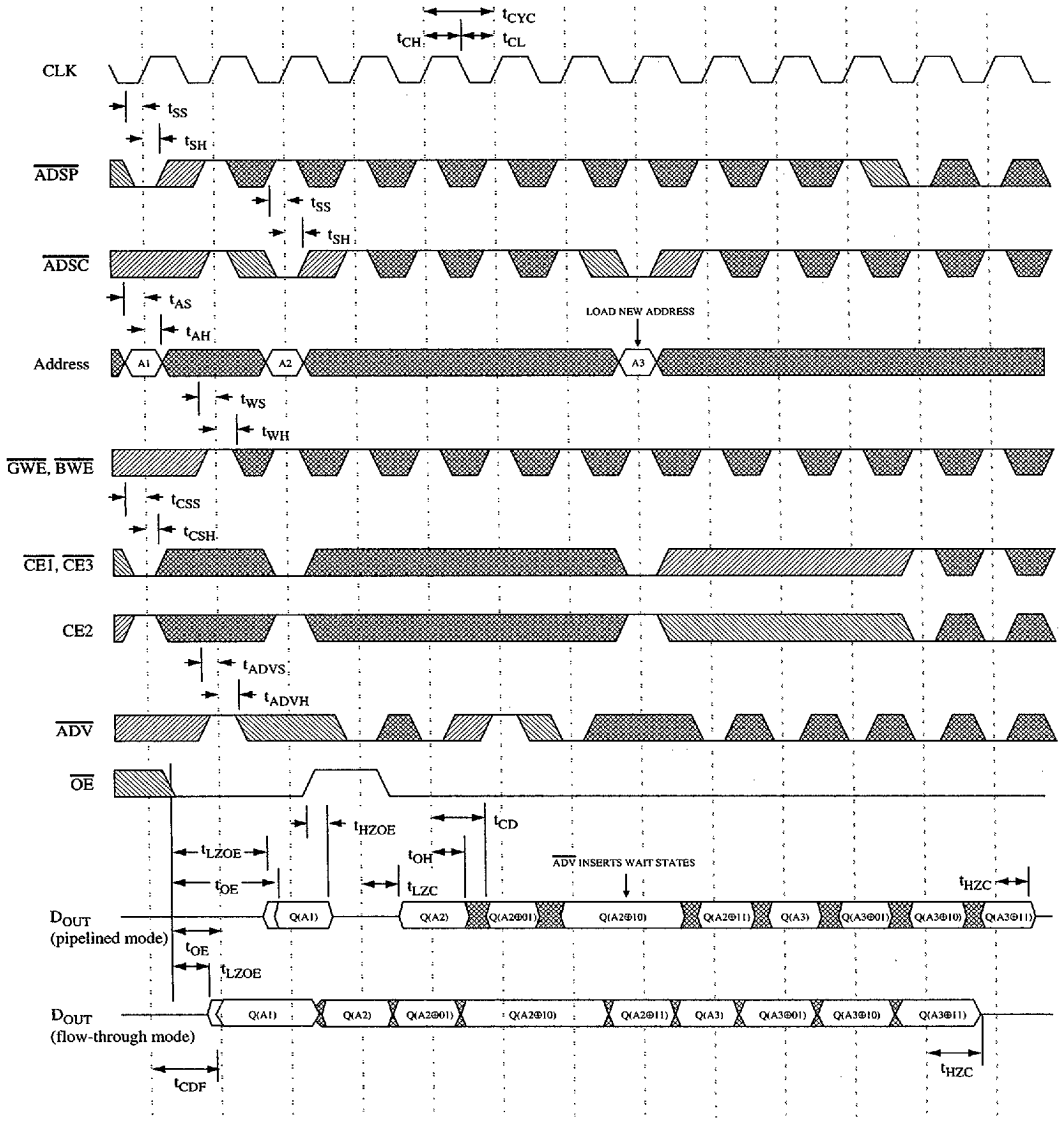
14 Mode pin exhibits input leakage current of ±10µA in linear burst mode and has an internal pull-up.

15 At least two clock cycles are required for entry or exit from sleep mode after ZZ assertion. ZZ specifications to comply with Intel documentation.

Key to switching waveforms

Rising input | Falling input | Undefined output/don't care

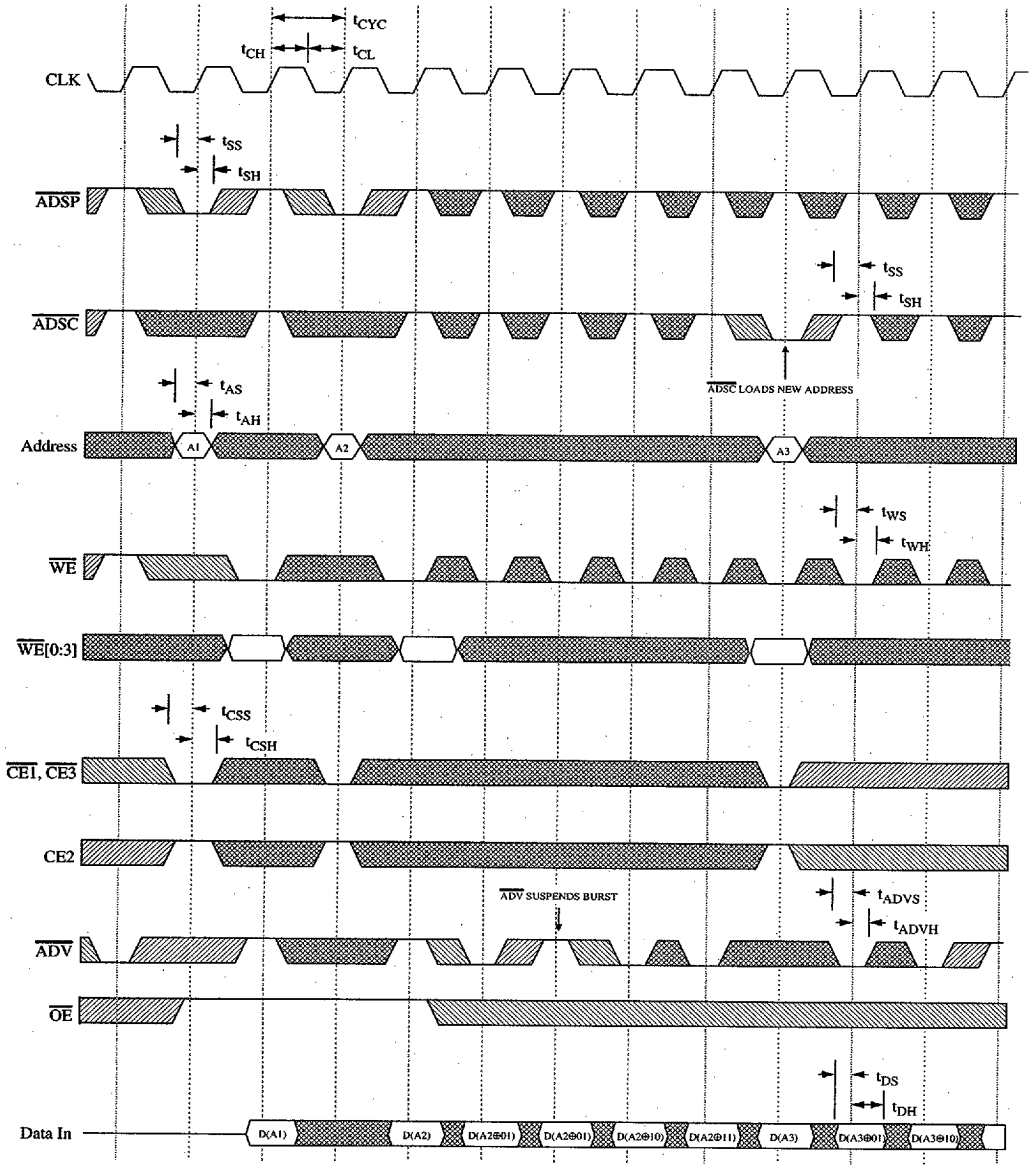
Read waveform



Note: ⊕ = XOR when MODE = High/No Connect; ⊕ = ADD when MODE = Low. Refer to Burst sequence table on page 140.
$\overline{WE}$[0:3] is don't care.

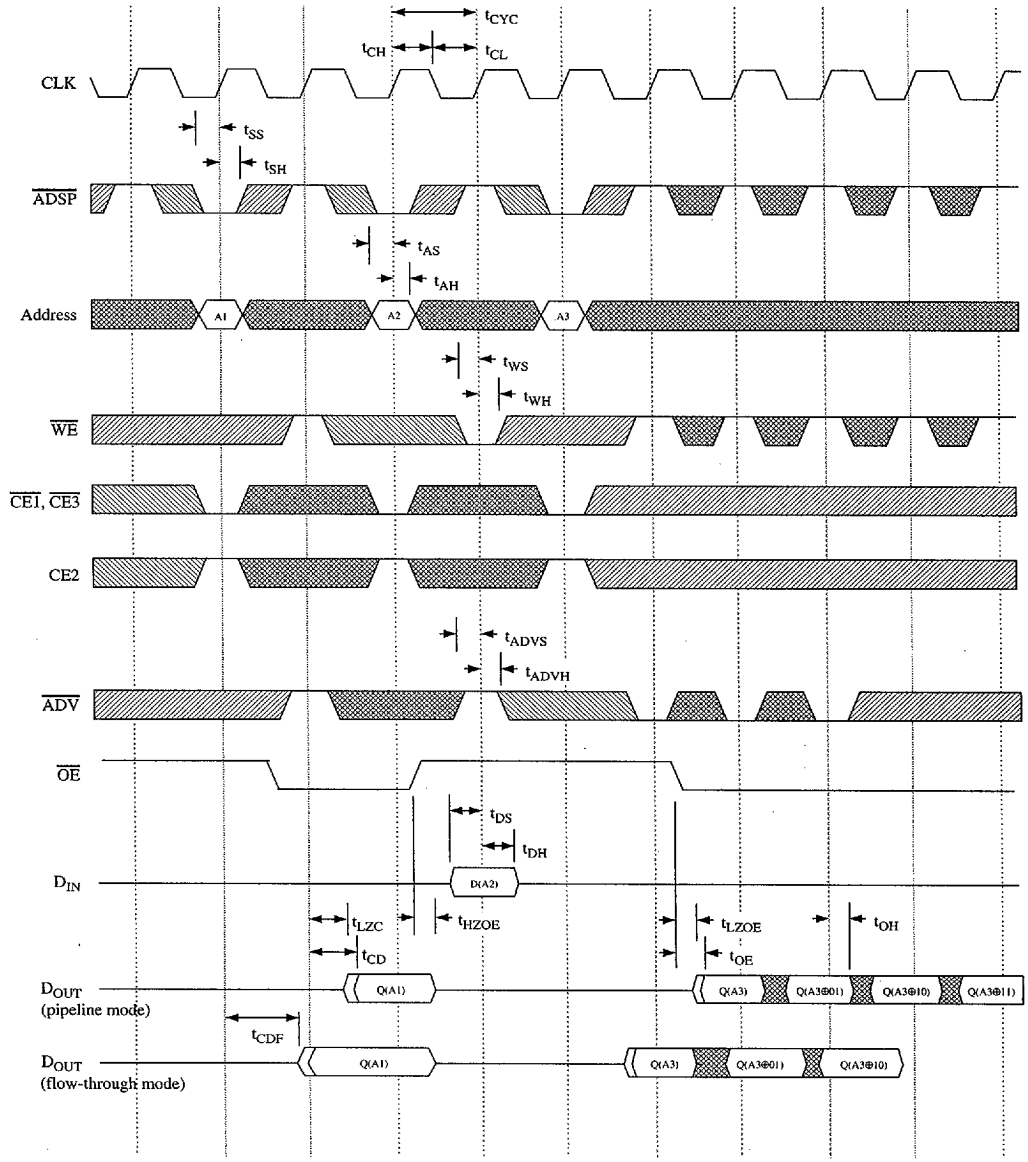
SRAM

Write waveform



Note: ⊕ = XOR when MODE = High/No Connect; ⊕ = ADD when MODE = Low. Refer to Burst sequence table on page 140.

Read/write waveform



Note: ⊕ = XOR when MODE = High/No Connect; ⊕ = ADD when MODE = Low. Refer to Burst sequence table on page 140.

AC test conditions

- Output load: see Figure B,
  except for t_{LZC}, t_{LZOE}, t_{HZOE}, t_{HZC} see Figure C.
- Input pulse level: GND to 3V. See Figure A.
- Input rise and fall time (Measured at 0.3V and 2.7V): 2 ns. See Figure A.
- Input and output timing reference levels: 1.5V.

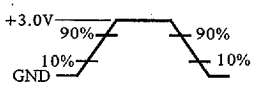


Figure A: Input waveform

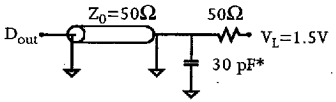


Figure B: Output load (A)

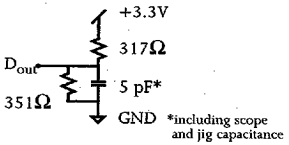
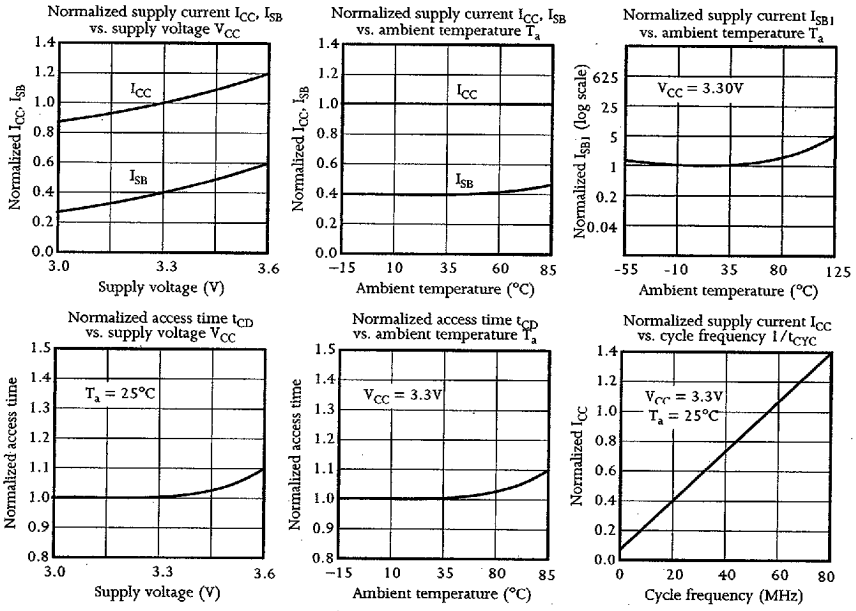


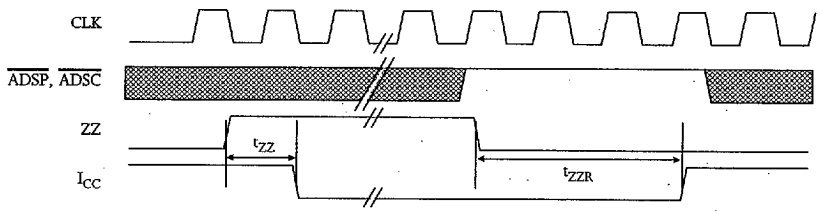
Figure C: Output load(B)
for t_{LZC}, t_{LZOE}, t_{HZOE}, t_{HZC}

Typical DC and AC electrical characteristics



Power-down waveform[19]

(preliminary information)



Application connectivity examples

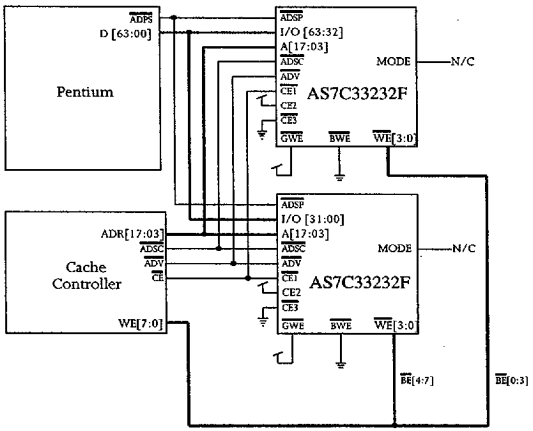


Figure A: Pentium 256KB cache

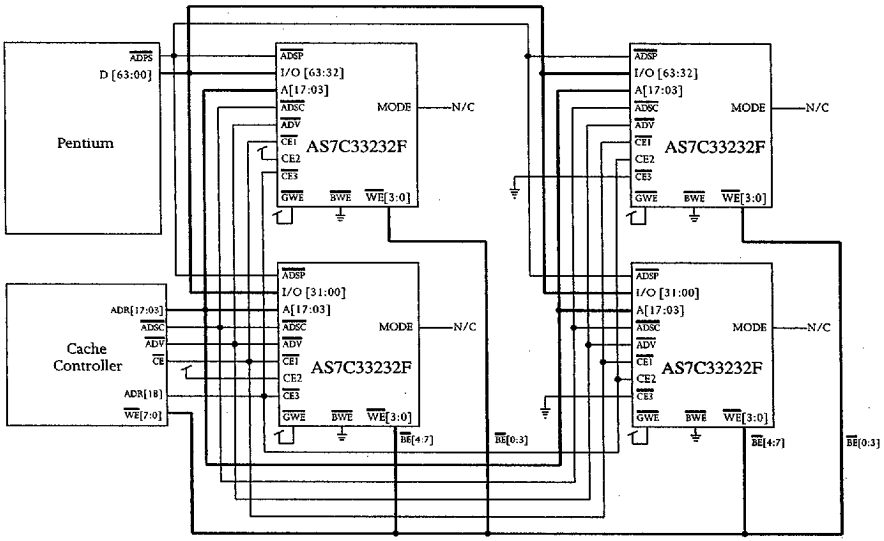


Figure B: Pentium 512KB two bank cache

AS7C33232F ordering information

Package \ Min cycle time	5 ns	6 ns	7 ns
PQFP	AS7C33232F-5QC	AS7C33232F-6QC	AS7C33232F-7QC
TQFP	AS7C33232F-5TQC	AS7C33232F-6TQC	AS7C33232F-7TQC

Shaded areas contain preliminary information.

AS7C33232F part numbering system

AS7C	3	3232F	–XX	XX	C
SRAM prefix	3 = 3.3V supply	Device number	Minimum access time	Package: Q = PQFP TQ = TQFP	Commercial temperature range, 0°C to 70 °C