AMD-K6™E

High-Performance, AMD-K6 Embedded Processor

AMD◢

DISTINCTIVE CHARACTERISTICS

■ **Advanced 6-Issue RISC86® Superscalar Microarchitecture**
  - Seven parallel specialized execution units
  - Multiple sophisticated x86-to-RISC86® instruction decoders
  - Advanced two-level branch prediction
  - Speculative execution
  - Out-of-order execution
  - Register renaming and data forwarding
  - Issues up to six RISC86 instructions per clock

■ **High-Performance IEEE 754-Compatible and 854-Compatible Floating-Point Unit**

■ **High-Performance Industry-Standard MMX™ Instructions**

■ **Large On-Chip Split 64-Kbyte Level-One (L1) Cache**
  - 32-Kbyte instruction cache with additional predecode cache
  - 32-Kbyte writeback dual-ported data cache
  - MESI protocol support

■ **321-Pin Ceramic PGA (Socket 7 Compatible) Package**

■ **Industry-Standard System Management Mode (SMM)**

■ **IEEE 1149.1 Boundary Scan**

■ **x86 Binary Software Compatibility**

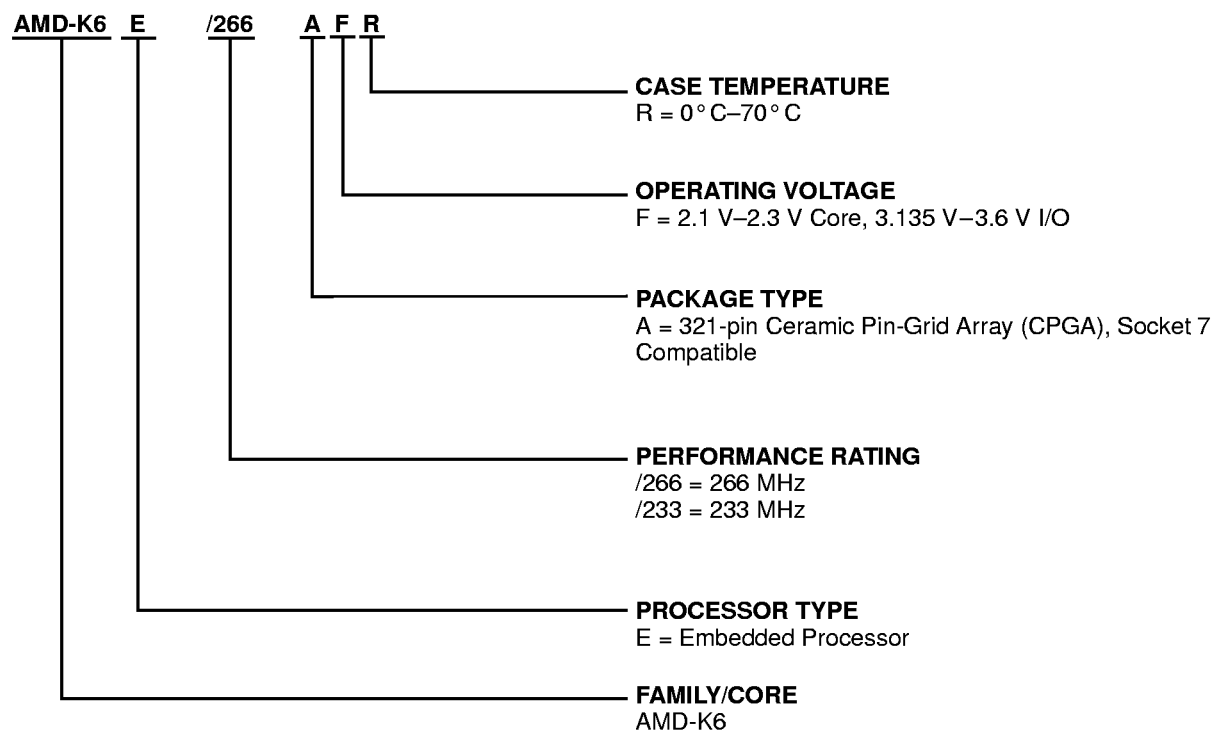■ **0.25-Micron Process Technology**

GENERAL DESCRIPTION

Note: This data sheet provides information specific to the AMD-K6E processor. For more information about the AMD-K6E processor, see the Model 7 section of the AMD-K6 Processor Data Sheet, order #20695.

With the AMD-K6E embedded processor, AMD continues to deliver leading-edge processor solutions. Based on the highly successful AMD-K6 processor with 0.25-micron process technology, the AMD-K6E processor delivers high performance with a low core voltage and low power dissipation. This new, embedded version of the AMD-K6 processor continues to leverage today's cost-effective infrastructure to deliver a superior price/performance solution.

As a member of AMD's E86™ family of embedded x86-based processors, the AMD-K6E processor extends the range of software-compatible performance allowing existing x86 designs and software to be used in high-performance products. In addition to a wide selection of inexpensive development tools, compilers, debuggers, chip sets, and PC operating systems, the AMD-K6E processor is also supported by a number of real-time operating systems (RTOS) such as QNX, pSOS, RTXC, and Windows® CE. This compatibility and support result in decreased development costs and improved time to market.
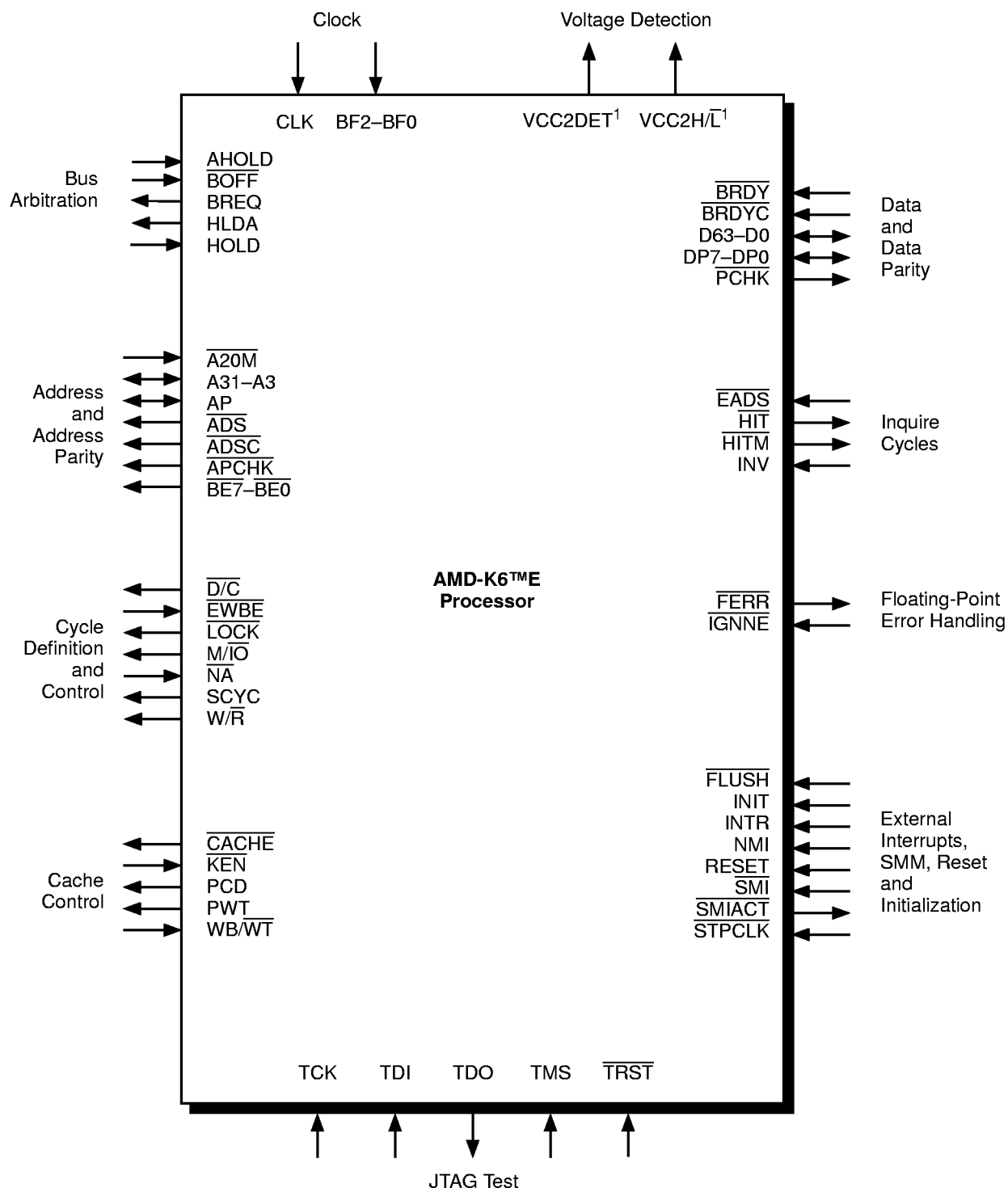
AMD

ORDERING INFORMATION

AMD-K6 E   /266   A F R

CASE TEMPERATURE
R = 0° C–70° C

OPERATING VOLTAGE
F = 2.1 V–2.3 V Core, 3.135 V–3.6 V I/O

PACKAGE TYPE
A = 321-pin Ceramic Pin-Grid Array (CPGA), Socket 7
Compatible

PERFORMANCE RATING
/266 = 266 MHz
/233 = 233 MHz

PROCESSOR TYPE
E = Embedded Processor

FAMILY/CORE
AMD-K6

Valid Combinations	
AMD-K6E/266 AMD-K6E/233	AFR

Valid Combinations
Valid combinations list configurations planned to
be supported in volume for this device. Consult the
local AMD sales office to confirm availability of
specific valid combinations and to check on newly
released combinations.

LOGIC DIAGRAM BY INTERFACE

Clock   Voltage Detection

CLK BF2–BF0   VCC2DET[1] VCC2H/$\overline{L}$[1]

Bus Arbitration
- AHOLD
- $\overline{BOFF}$
- BREQ
- HLDA
- HOLD

Address and Address Parity
- $\overline{A20M}$
- A31–A3
- AP
- $\overline{ADS}$
- $\overline{ADSC}$
- $\overline{APCHK}$
- $\overline{BE7}$–$\overline{BE0}$

Cycle Definition and Control
- $D/\overline{C}$
- $\overline{EWBE}$
- $\overline{LOCK}$
- $M/\overline{IO}$
- $\overline{NA}$
- SCYC
- $W/\overline{R}$

Cache Control
- $\overline{CACHE}$
- KEN
- PCD
- PWT
- $WB/\overline{WT}$

AMD-K6™E Processor

Data and Data Parity
- $\overline{BRDY}$
- $\overline{BRDYC}$
- D63–D0
- DP7–DP0
- $\overline{PCHK}$

Inquire Cycles
- $\overline{EADS}$
- $\overline{HIT}$
- $\overline{HITM}$
- INV

Floating-Point Error Handling
- $\overline{FERR}$
- $\overline{IGNNE}$

External Interrupts, SMM, Reset and Initialization
- $\overline{FLUSH}$
- INIT
- INTR
- NMI
- RESET
- $\overline{SMI}$
- $\overline{SMIACT}$
- $\overline{STPCLK}$

TCK TDI TDO TMS $\overline{TRST}$

JTAG Test

Notes:

1. *For information about the VCC2DET and VCC2H/$\overline{L}$ pins, see Chapter 26, "Signal Descriptions," in the* AMD-K6 Processor Data Sheet, *order #20695.*

ARCHITECTURAL OVERVIEW

Figure 1 shows the block diagram for the AMD-K6E embedded processor. The sections that follow describe the features of the part.
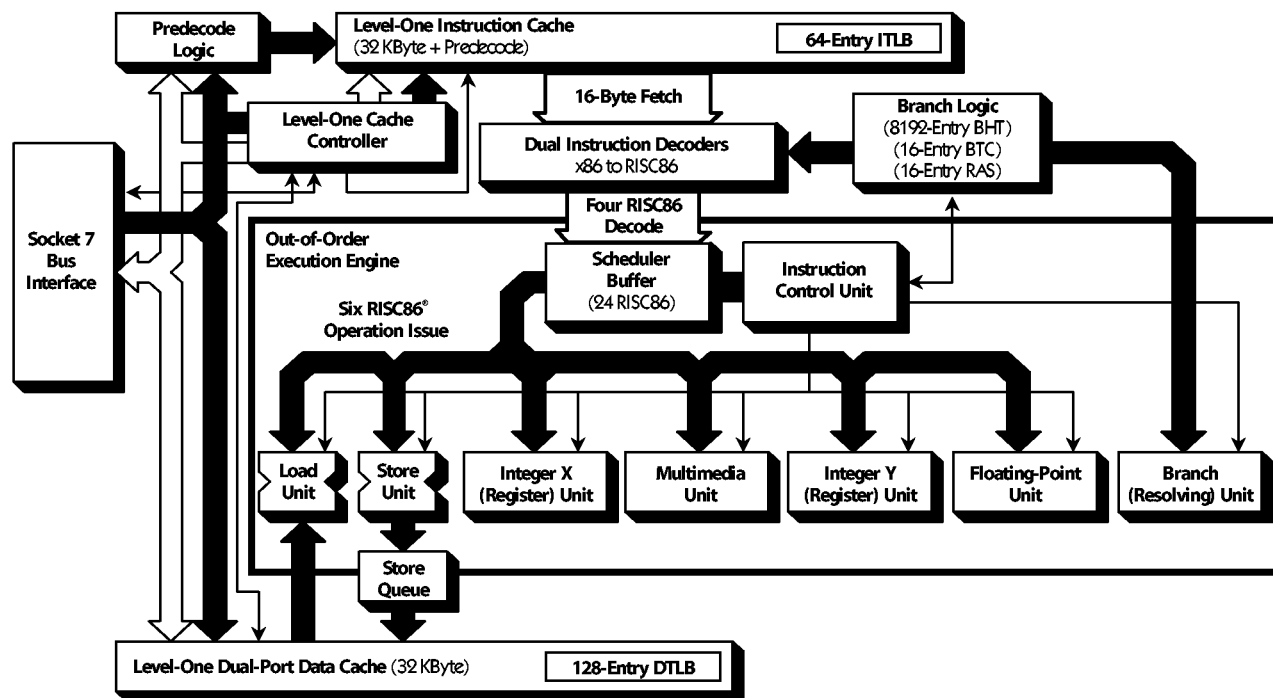

Figure 1. AMD-K6™E Embedded Processor Block Diagram

The AMD-K6™E Processor

The AMD-K6E embedded processor is function- and pin-compatible with the industry-leading AMD-K6 processor (Model 7). It is an excellent choice for embedded applications that require a high-performance x86-compatible processor such as central office switches, network routers, point-of-sale terminals, information appliances, and Socket 7/Windows based single-board computers.

The AMD-K6™ Processor Core

The AMD-K6E embedded processor is based on the AMD-K6 processor (Model 7), and it maintains pin, function, and software compatibility.

To provide industry-leading performance, the AMD-K6 processor core incorporates the innovative and efficient RISC86 microarchitecture, a large 64-Kbyte level-one cache (32-Kbyte dual-ported data cache, 32-Kbyte instruction cache with predecode data), a powerful IEEE 754-compatible and 854-compatible floating-point execution unit, and a high-performance multimedia execution unit for executing industry-standard MMX™ instructions. These features have been combined to deliver industry leadership in

16-bit and 32-bit performance.

The AMD-K6 processor's RISC86 microarchitecture is a decoupled decode/execution superscalar design that implements state-of-the-art design techniques to achieve leading-edge performance. Advanced design techniques implemented in the AMD-K6 include multiple x86 instruction decode, single-clock internal RISC operations, seven execution units that support superscalar operation, out-of-order execution, data forwarding, speculative execution, and register renaming. In addition, the processor supports state-of-the-art advanced branch prediction logic by implementing an 8192-entry branch history table (the industry's only branch target cache) and a return address stack, which combine to deliver an extremely high prediction rate. These design techniques enable the AMD-K6 processor to issue, execute, and retire multiple x86 instructions per clock, resulting in excellent scalable performance.

Designed to run both 16-bit and 32-bit software, the AMD-K6 processor is x86 binary-code compatible. AMD's extensive experience through four generations of x86 processors has been carefully integrated into the AMD-K6 to provide complete compatibility with

Windows 3.x, Windows CE, Windows 95, Windows 98, Windows NT®, DOS, OS/2, UNIX, Solaris, NetWare®, Vines, and other leading x86 operating systems and applications. The AMD-K6 processor is Socket 7 compatible, allowing the processor to be quickly and easily integrated into a mature and cost-effective industry-standard infrastructure of motherboards, chip sets, power supplies, and thermal solutions.

AMD has designed, manufactured, and delivered over 50 million Microsoft Windows compatible processors. The AMD-K6 processor is one in a long line of processors.

With its combination of state-of-the-art features, industry-leading performance, high-performance multimedia engine, full x86 compatibility, and low-cost infrastructure, the AMD-K6E embedded processor is an excellent choice for high-performance embedded applications and fast time to market.

Maximum Frequency

Table 1 shows the maximum CPU and maximum bus frequencies for the AMD-K6E processor.

Table 1. Maximum Frequency

Processor	CPU Clock Max. Frequency	Bus Input Clock Max. Frequency
AMD-K6™E/266	266 MHz	66 MHz
AMD-K6E/233	233 MHz	66 MHz

OPERATING RANGES

The functional operation of the AMD-K6E processor is designed to work within the voltage and temperature parameters defined in Table 2.

Table 2.   AMD-K6™E Operating Ranges

Parameter	Minimum	Typical	Maximum
V_{CC2}[1,2]	2.1 V	2.2 V	2.3 V
V_{CC3}[1]	3.135 V	3.3 V	3.6 V
T_{CASE}	0°C	—	70°C

Notes:

1. V_{CC2} and V_{CC3} are referenced from V_{SS}.
2. V_{CC2} specification for 2.2 V components.

ABSOLUTE RATINGS

Exposure to conditions outside the operating ranges listed in Table 2 for extended periods of time can affect long-term reliability. Permanent damage can occur if the absolute ratings listed in Table 3 are exceeded.

Table 3.   AMD-K6™E Absolute Ratings

Parameter	Minimum	Maximum
V_{CC2}	–0.5 V	2.5 V
V_{CC3}	–0.5 V	3.6 V
V_{PIN}[1]	–0.5 V	V_{CC3} + 0.5 V and ≤ 4.0 V
T_{CASE} (under bias)	–65°C	+110°C
$T_{STORAGE}$	–65°C	+150°C

Notes:

1. V_{PIN} (the voltage on any I/O pin) must not be greater than 0.5 V above the voltage being applied to V_{CC3}. In addition, the V_{PIN} voltage must never exceed 4.0 V.

POWER DISSIPATION

Table 4 contains the typical and maximum power dissipation of the AMD-K6E processor during normal and reduced power states.

Table 4.   AMD-K6™E Typical and Maximum Power Dissipation

Clock Control State	233 MHz	266 MHz
Normal (Maximum Thermal Power)[1]	13.50 W	14.55 W
Normal (Typical Thermal Power)[2]	8.10 W	8.75 W
Stop Grant / Halt (Maximum)[3]	2.46 W	2.48 W
Stop Clock (Maximum)[4]	2.25 W	2.25 W

Notes:

1. *The maximum power dissipated in the normal clock control state must be taken into account when designing a solution for thermal dissipation for the AMD-K6E processor. Maximum power is determined for the worst-case instruction sequence or function for the listed clock control states with V_{CC2} = 2.2 V and V_{CC3} = 3.3 V.*

2. *Typical power is determined for the typical instruction sequences or functions associated with normal system operation with V_{CC2} = 2.2 V and V_{CC3} = 3.3 V.*

3. *The CLK signal and the internal PLL are still running but most internal clocking has stopped.*

4. *The CLK signal, the internal PLL, and all internal clocking has stopped.*

THERMAL SPECIFICATIONS

The AMD-K6E processor operating specifications call for the case temperature (T_C) to be in the range of 0°C to 70°C for the CPGA package.

The ambient temperature (T_A) is not specified as long as the case temperature is not violated. The case temperature must be measured on the top center of the package.

Table 5 shows the thermal specifications derated,

based on operating the CPU at frequencies lower than the maximum rated frequency.

For more information about the AMD-K6E thermal specifications, see Chapter 38, "Thermal Design" in the *AMD-K6 Processor Data Sheet*, order #20695. For information about thermal solutions, see the *AMD-K6 Processor Thermal Solution Design Application Note*, order #21085.

**Table 5.   AMD-K6™E Thermal Power Derating Based On Lower CPU Frequencies**

Frequency	Max. I_{CC2} (core) V_{CC2} = 2.2 V ±100 mV[1]	Max. I_{CC3} (I/O) V_{CC3} = 3.3 V +300 mV, −165 mV[2]	Max. Thermal Power[3]	Typical Thermal Power[4]	Clock Multiple	BF2–BF0
133 MHz	3.95 A	0.46 A	8.60 W	5.20 W	2.0X	110b
166 MHz	4.95 A	0.48 A	10.50 W	6.30 W	2.5X	100b
200 MHz	5.95 A	0.50 A	12.45 W	7.50 W	3.0X	101b
233 MHz	6.50 A	0.52 A	13.50 W	8.10 W	3.5X	111b
266 MHz	7.05 A	0.54 A	14.55 W	8.75 W	4.0X	010b

Notes:

1. *Max. I_{CC2} specification is taken at V_{CC2} = 2.3 V. (The maximum power supply current must be taken into account when designing a power supply.)*

2. *Max. I_{CC3} specification is taken at V_{CC3} = 3.6 V. (The maximum power supply current must be taken into account when designing a power supply.)*

3. *The maximum power dissipated in the normal clock control state must be taken into account when designing a solution for thermal dissipation for the AMD-K6E processor. Maximum power is determined for the worst-case instruction sequence or function for the listed clock control states with V_{CC2} = 2.2 V and V_{CC3} = 3.3 V.*

4. *Typical power is determined for the typical instruction sequences or functions associated with normal system operation with V_{CC2} = 2.2 V and V_{CC3} = 3.3 V.*

PHYSICAL DIMENSIONS

CGF 321, Ceramic Pin-Grid Array (CPGA)
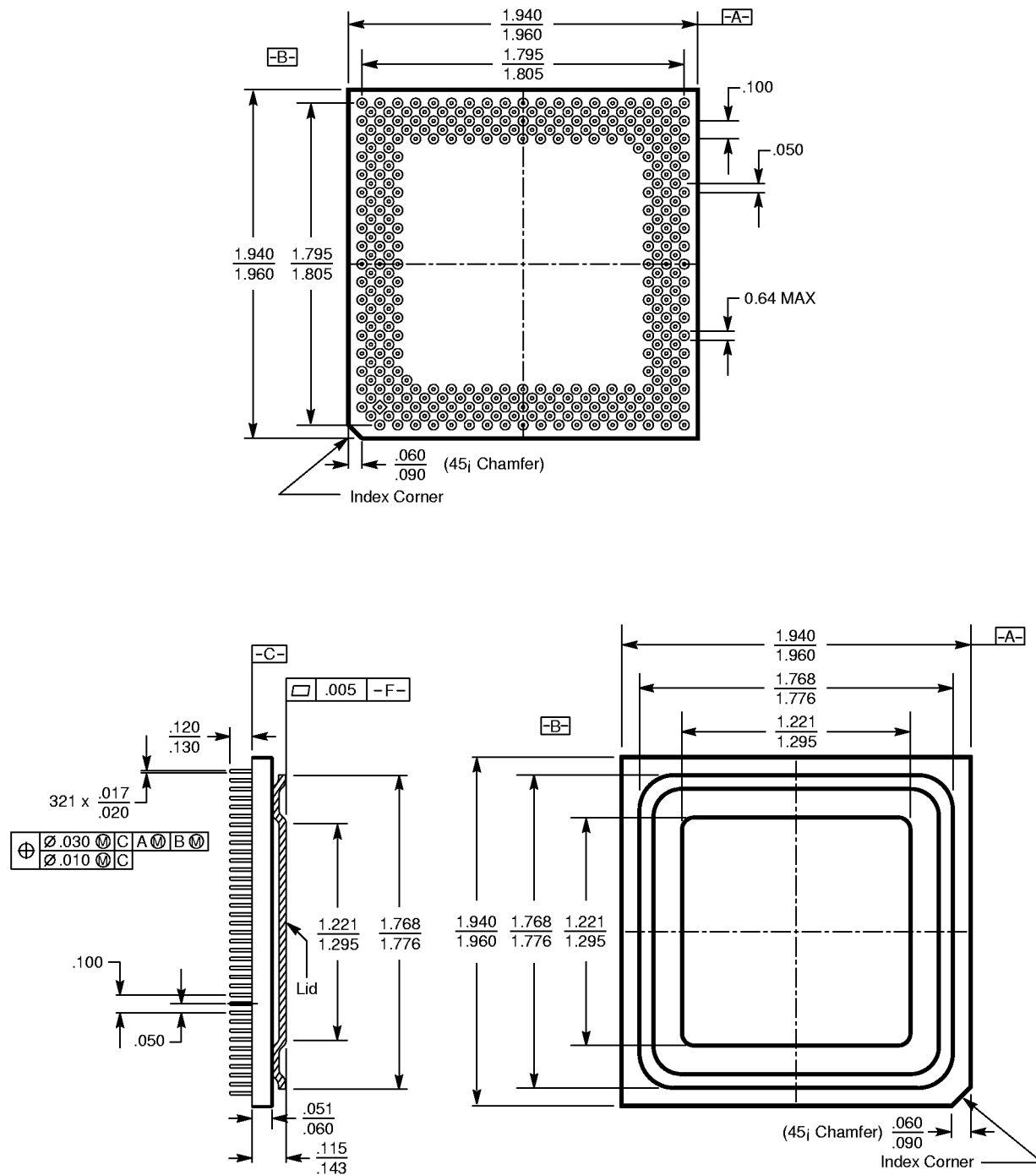
SIDE VIEW OF CGF PGA

16-038-CP-5_AC
CGF321
EU160
1.13.99 lv

Note: All dimensions are in inches.

AMD

Trademarks

AMD, the AMD logo, and combinations thereof, AMD-K6, and E86 are trademarks, and RISC86 is a registered trademark of Advanced Micro Devices, Inc.

MMX is a trademark of Intel Corporation.

Windows and Windows NT are registered trademarks of Microsoft Corporation.

Netware is a registered trademark of Novell, Inc.

Product names used in this publication are for identification purposes only and may be trademarks of their respective companies.

Disclaimer

The contents of this document are provided in connection with Advanced Micro Devices, Inc. ("AMD") products. AMD makes no representations or warranties with respect to the accuracy or completeness of the contents of this publication and reserves the right to make changes to specifications and product descriptions at any time without notice. No license, whether express, implied, arising by estoppel or otherwise, to any intellectual property rights is granted by this publication. Except as set forth in AMD's Standard Terms and Conditions of Sale, AMD assumes no liability whatsoever, and disclaims any express or implied warranty, relating to its products including, but not limited to, the implied warranty of merchantability, fitness for a particular purpose, or infringement of any intellectual property right.

AMD's products are not designed, intended, authorized or warranted for use as components in systems intended for surgical implant into the body, or in other applications intended to support or sustain life, or in any other application in which the failure of AMD's product could create a situation where personal injury, death, or severe property or environmental damage may occur. AMD reserves the right to discontinue or make changes to its products at any time without notice.