12-BIT 500KSPS ADC ADC1275X

GENERAL DESCRIPTION

The ADC1275X is a CMOS 3.3V 12-bit analog-to-digital converter (ADC). It converts the analog input signal into 12-bit binary digital codes at a maximum conversion rate of 500KSPS with 2.5MHz clock.
The device is a recycling type monolithic ADC with an on-chip sample-and-hold function. The ADC has power down mode.

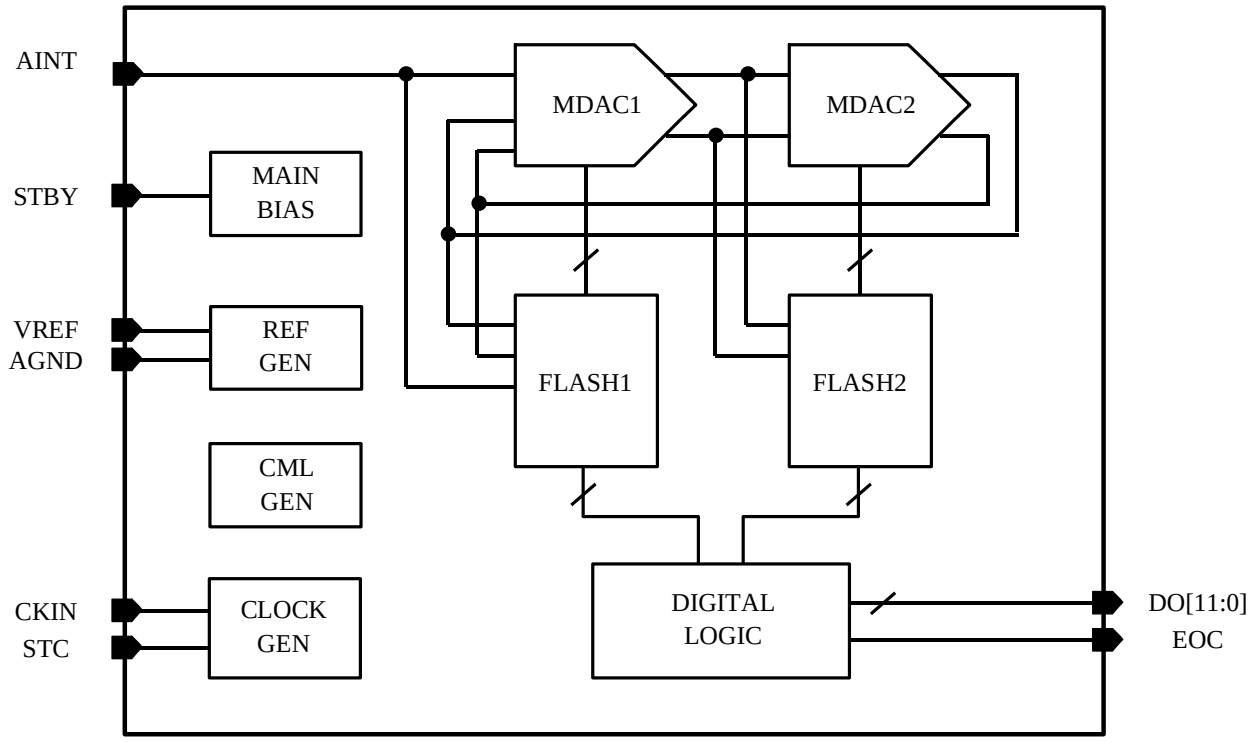
TYPICAL APPLICATIONS

MICOM Interface
Portable Equipment
Low-Voltage Low-Power Application

FEATURES

- **Resolution : 12-bit**
- **Maximum Conversion Rate : 500KSPS**
- **Main Clock : 2.5MHz**
- **Power Supply : 3.3V ±0.3V**
- **Total Current : 20uA (Standby Mode)**
  2.7mA (Normal Operation)
- **Input Range : 0.0V ~ 3.3V ($3.3V_{P-P}$)**
- **Differential Linearity Error : ±1.0 LSB (Max)**
- **Integral Linearity Error : ±3.0 LSB (Max.)**
- **Signal to Noise & Distortion Ratio : 62dB**
- **Digital Output : CMOS Level**
- **Operating Temperature Range : -40 °C ~ 85 °C**

FUNCTIONAL BLOCK DIAGRAM



Ver 1.3 (Apr. 2002)

CORE PIN DESCRIPTION

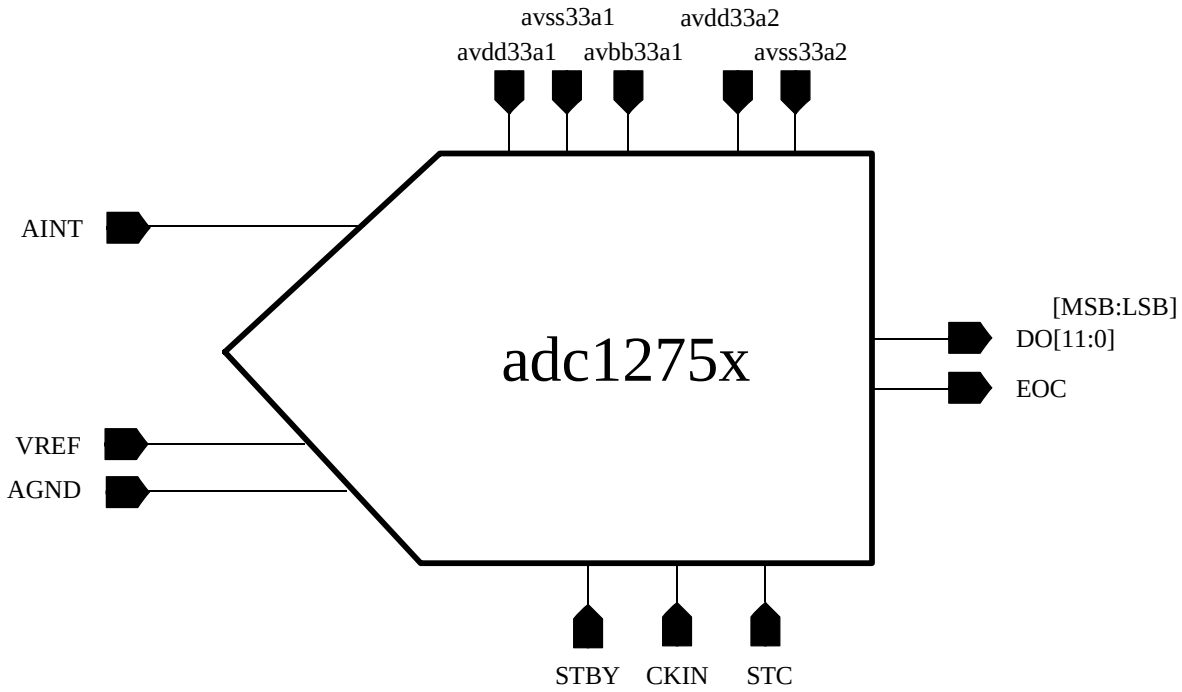
NAME	I/O TYPE	I/O PAD	PIN DESCRIPTION
VREF	AI	phia_abb	Reference Top (3.3V)
AGND	AI	phia_abb	Reference Bottom (0.0V)
AVDD33A1	AP	vdd3t_abb	Analog Power (3.3V)
AVBB33A1	AG	vbb3_abb	Analog Sub Bias (0.0V)
AVSS33A1	AG	vss3t_abb	Analog Ground (0.0V)
AINT	AI	phiar50_abb	Analog Input (Input Range : 0.0V ~ 3.3V)
STBY	DI	phicc_abb	VDD=power saving (standby), GND=normal
CKIN	DI	phicc_abb	Sampling Clock Input
D[11:0]	DO	phot4_abb	Digital Output
EOC	DO	phot4_abb	End of Conversion Signal
STC	DI	phicc_bb	Start of Conversion Signal
AVSS33A2	DG	vss3t_abb	Digital GND (0.0V)
AVDD33A2	DP	vdd3t_abb	Digital Power (3.3V)

I/O TYPE ABBR.

- AI : Analog Input
- DI : Digital Input
- AO : Analog Output
- DO : Analog Output

- AP : Analog Power
- AG : Analog Ground
- DP : Digital Power
- DG : Digital Ground

- AB : Analog Bidirection
- DB : Digital Bidirection



ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Value	Unit
Supply Voltage	VDD	3.8	V
Analog Input Voltage	AINT	VSS to VDD	V
Digital Input Voltage	CKIN	VSS to VDD	V
Reference Voltage	VREF / AGND	VSS to VDD	V
Storage Temperature Range	Tstg	-45 to 150	°C
Operating Temperature Range	Topr	-40 to 85	°C

NOTES

1. Absolute maximum rating specifies the values beyond which the device may be damaged permanently. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect reliability. Each condition value is applied with the other values kept within the following operating conditions and function operation under any of these conditions is not implied.
2. All voltages are measured with respect to VSS unless otherwise specified.
3. 100pF capacitor is discharged through a 1.5kΩ resistor (Human body model)

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Typ	Max	Unit
Supply Voltage	AVDD33A1 AVDD33A2	3.0	3.3	3.6	V
Reference Input Voltage	VREF AGND	2.0 0.0	3.3 0.0	3.6 0.0	V
Analog Input Voltage	AINT	0.0	VREF	-	V
Operating Temperature	Toper	-40	-	85	°C

NOTES

It is strongly recommended that all the supply pins (AVDD33A1, AVDD33A2) be powered from the same source to avoid power latch-up.

DC ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Unit	Test Condition
Differential Nonlinearity	DNL	-	±0.8	±1	LSB	VREF=3.3V AGND=0.0V
Integral Nonlinearity	INL	-	±1.8	±3	LSB	VREF=3.3V AGND=0.0V
Offset Voltage	OFF	-	10	16	LSB	VREF=3.3V AGND=0.0V

(Converter Specifications : AVDD33A1=AVDD33A2=3.3V, AVSS33A1=AVSS33A2=0V,
Toper=25 °C, VREF=3.3V, AGND=0.0V unless otherwise specified)

AC ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Unit	Test Condition
Maximum Conversion Rate	fc	-	-	500	KSPS	f_{CKIN} = 2.5MHz
Standby Supply Current		-	20	40	uA	STBY = VDD
Dynamic Supply Current	IVDD	-	2.3	3	mA	f_{CKIN}=2.5MHz (without system load)
Reference Current	IREF	-	0.4	0.6	mA	V_{REF} = 3.3V
Total Harmonic Distortion	THD	-	-70	-66	dB	f_{CKIN} = 2.5MHz AINT=100kHz
Signal-to-Noise & Distortion Ratio	SNDR	60	62	-	dB	f_{CKIN} = 2.5MHz AINT=100kHz

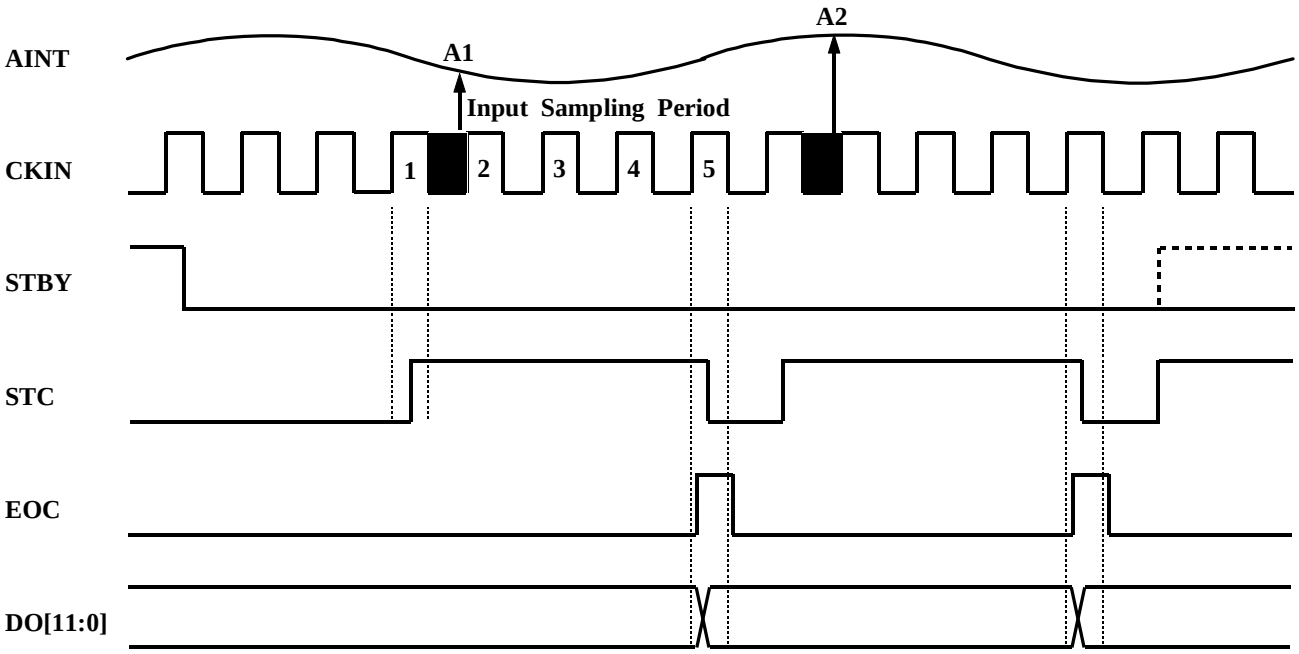
(Converter Specifications : AVDD33A1=AVDD33A2=3.3V, AVSS33A1=AVSS33A2=0V,
Toper=25 °C, VREF=3.3V, AGND=0.0V unless otherwise specified)

I/O CHART

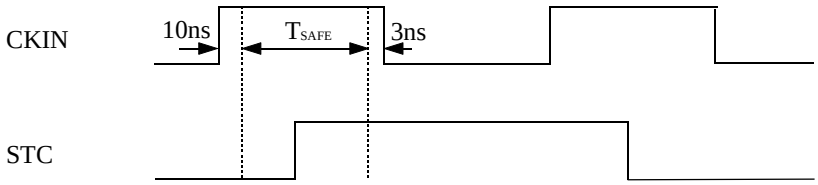
Index	AINT Input (V)	Digital Output	
0	~ 0.00081	0000 0000 0000	1LSB=0.806mV VREF=3.3V AGND=0.0V
1	0.00081 ~ 0.00161	0000 0000 0001	
2	0.00161 ~ 0.00242	0000 0000 0010	
~	~	~	
2047	1.64919 ~ 1.65000	0111 1111 1111	
2048	1.65000 ~ 1.65081	1000 0000 0000	
2049	1.65081 ~ 1.65161	1000 0000 0001	
~	~	~	
4093	3.29758 ~ 3.29839	1111 1111 1101	
4094	3.29839 ~ 3.29919	1111 1111 1110	
4095	3.29919 ~	1111 1111 1111	

TIMING DIAGRAM

1. Main Waveform



2. STC & CKIN Condition



The A/D Converter operates data conversion when STC (Start Conversion) signal is just "HIGH". Otherwise, output data (DO[11:0]) keep the current states. The STC signal should be changed during "T_{SAFE}" with the "HIGH" level of the clock to operation as shown in the main waveform.

· **ADC External Interface Signal**

AINT : Analog Input Signal (Input)

Input Range : VREF ~ AGND

STBY : Stand-by Signal, Power Save Mode (Input)

CKIN : ADC Main Clock, f_{CKIN} = 2.5MHz, 1 Clock Period = 400ns (Input)

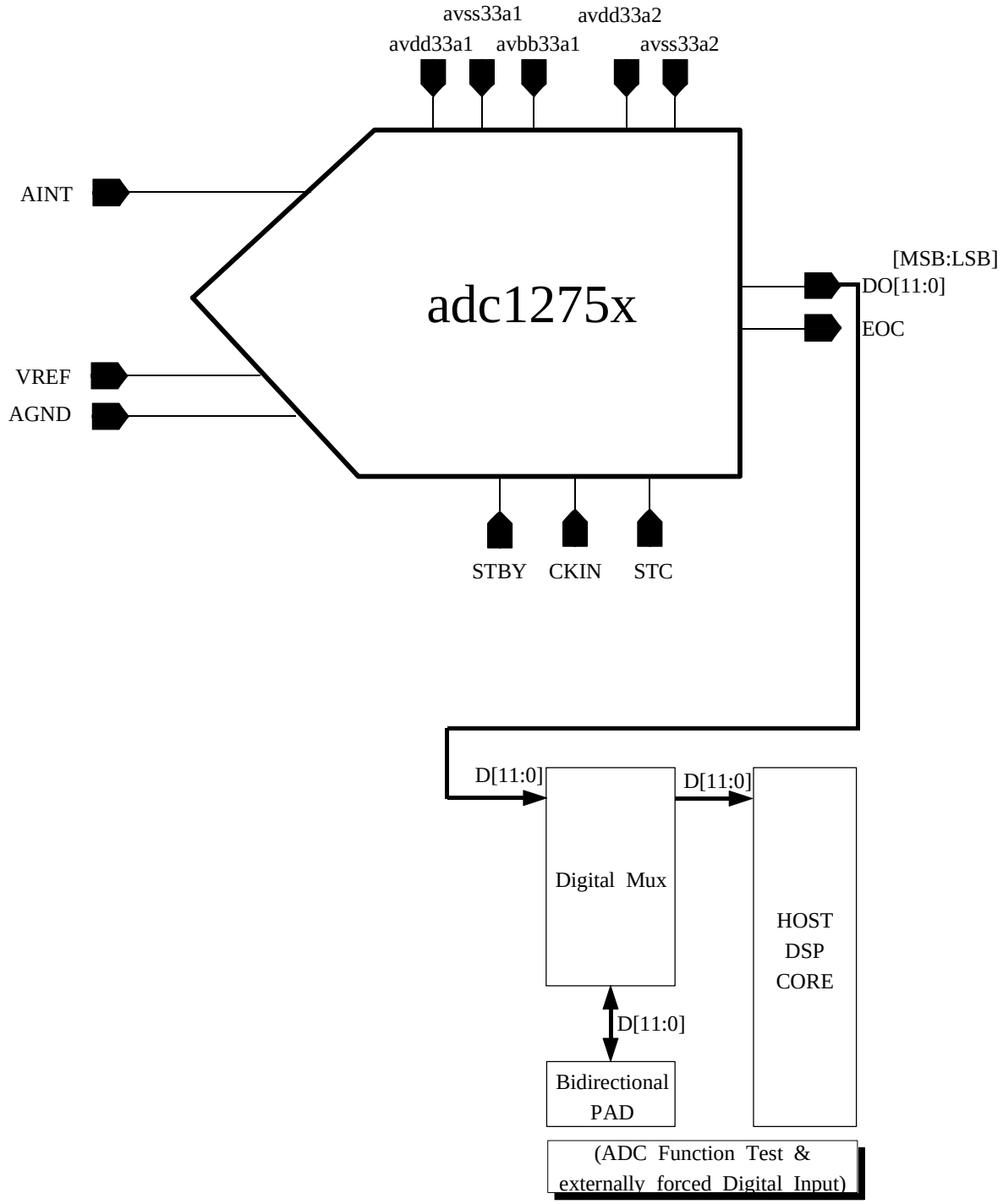
STC : Start of Conversion Signal (Input)

EOC : End of Conversion Signal (Output)

DO[11:0] : Digital Output Signal (Output)

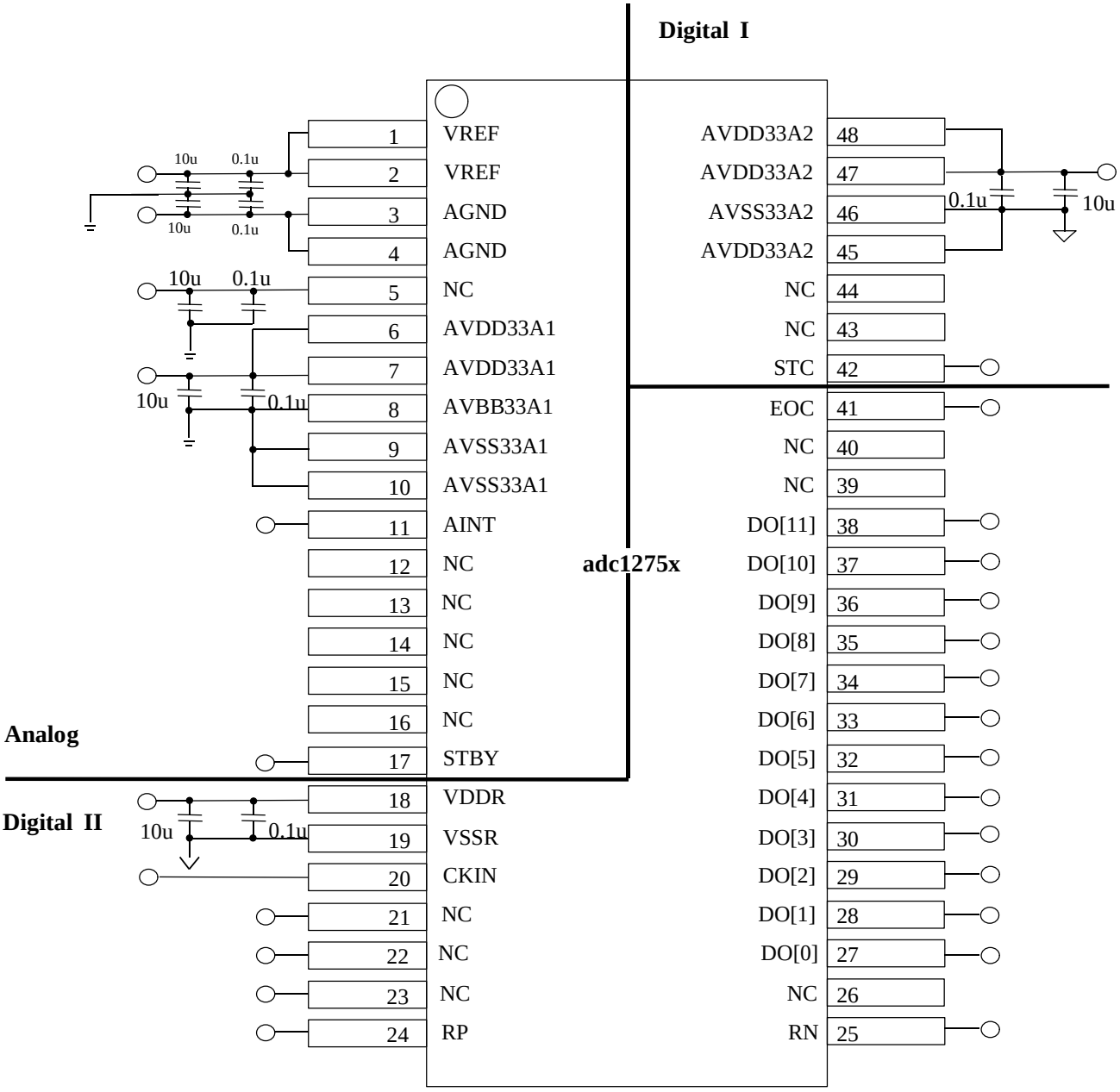
CORE EVALUATION GUIDE

1. ADC function is evaluated by external check on the bidirectional pads connected to input nodes of HOST DSP back-end circuit.
2. The reference voltages may be biased internally through resistor divider.



PACKAGE CONFIGURATION

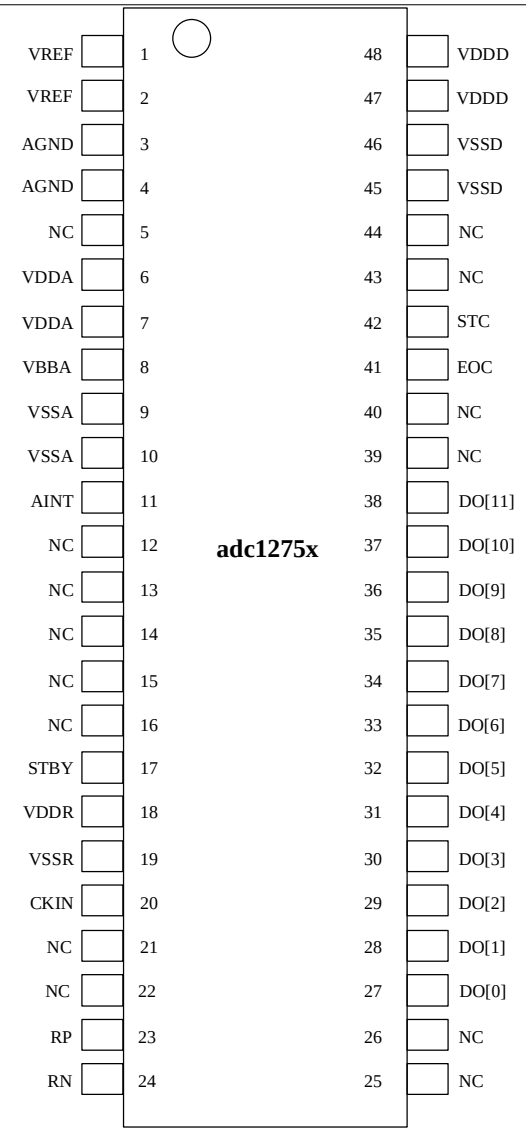
NOTES
1. NC denotes "No Connection".



PACKAGE PIN DESCRIPTION

No.	NAME	I/O TYPE	PIN DESCRIPTION
1,2	VREF	AI	Reference Voltage (3.3V)
3,4	AGND	AI	Analog Ground (0.0V)
6, 7	AVDD33A1	AP	Analog Power (3.3V)
8	AVBB33A1	AG	Analog Sub Bias
9, 10	AVSS33A1	AG	Analog Ground
11	AINT	AI	Analog Input
17	STBY	DI	VDD=Power saving (Standby), GND=Normal
18	VDDR	PP	PAD Power (3.3V)
19	VSSR	PG	PAD Ground
20	CKIN	DI	Clock Input (f_{CKIN} = 2.5MHz)
24	RP	AO	Test Pin1
25	RN	AO	Test Pin2
27	DO[0]	DO	Digital Output (LSB)
28~37	DO[1:10]	DO	Digital Output
38	DO[11]	DO	Digital Output (MSB)
41	EOC	DO	End of Conversion Signal
42	STC	DI	Start of Conversion Signal
45, 46	AVSS33A2	DG	Digital GND
47, 48	AVSS33A2	DP	Digital Power (3.3V)

CONFIGURATION



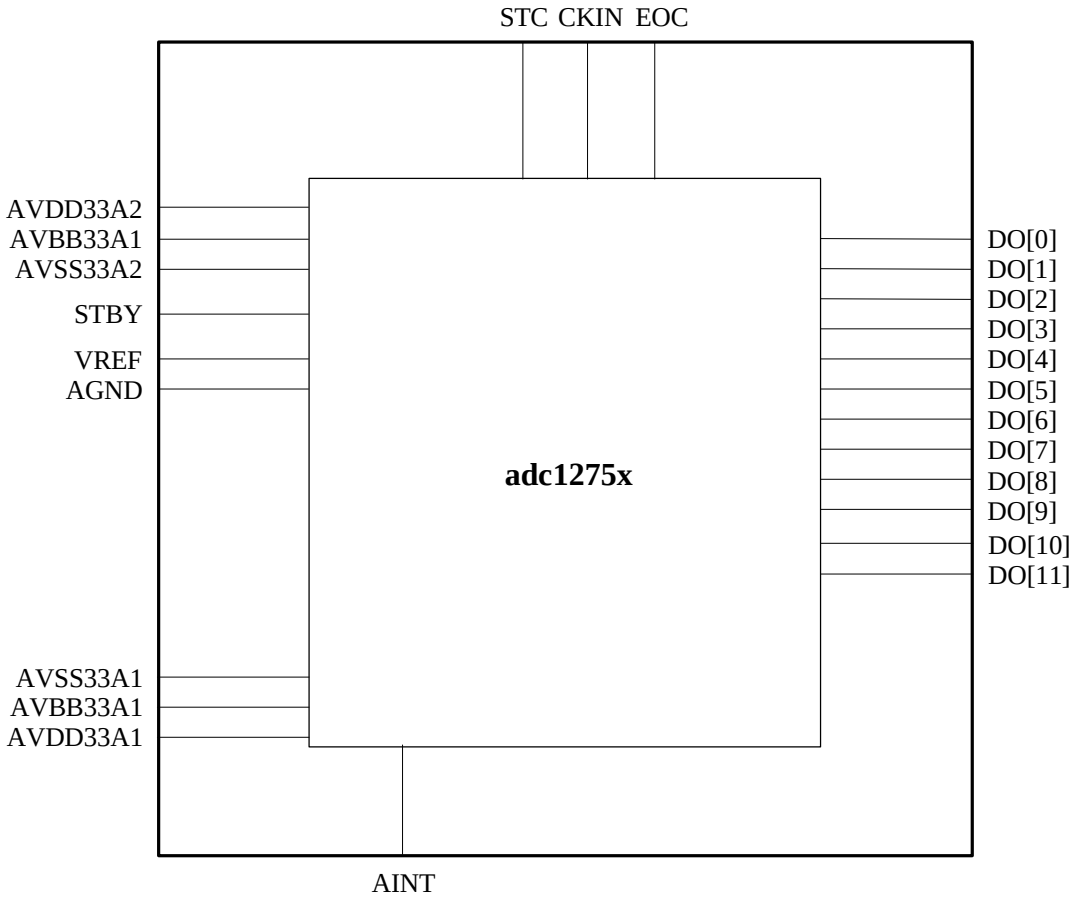
NOTES

1. I/O TYPE PP and PG denote PAD Power and PAD Ground respectively.

USER GUIDE

1. Input Range
   - The analog input is single-ended type and the range is from VREF to AGND. This AINT voltage follows reference voltage range fundamentally. So, if you want to alter into the another input range, you should change the voltage value of VREF.
   - You can use the AINT voltage whose minimum range is 2.0V. In this case, the VREF is 2.0V.

PHANTOM CELL INFORMATION



NAME	I/O TYPE	Pin Usage	PIN DESCRIPTION
AINT	AI	Internal/External	AINT signal should not be crossed by any signals and should not run next to digital signals to minimize capacitive coupling between the two signals.
STBY	DI	Internal/External	Digital Input Signal lines must have same length to reduce propagation delay.
CKIN	DI	Internal/External	
D[11:0]	DO	Internal/External	
EOC	DO	Internal/External	
STC	DI	Internal/External	
VREF	AI	External	Voltage reference lines (VREF and AGND) must be wide metal to reduce voltage drop of metal lines.
AGND	AI	External	
AVDD33A1	AP	External	1. It is recommended that you use thick analog power metal. When connected to PAD, the path should be kept as short as possible. 2. Digital power and analog power are separately used.
AVBB33A1	AG	External	
AVSS33A1	AG	External	
AVSS33A2	DG	External	
AVDD33A2	DP	External	

FEEDBACK REQUEST

ADC Specification

Parameter	Min	Typ	Max	Unit	Remarks
Supply voltage				V	
Reference Input voltage				V	
Analog Input voltage				Vpp	
Operating temperature				°C	
Integral non-linearity error				LSB	
Differential non-linearity error				LSB	
Offset voltage error (Bottom)				mV	
Offset voltage error (Top)				mV	
Maximum conversion rate				MSPS	
Dynamic supply current				mA	
Power dissipation				mW	
Signal-to-noise ratio				dB	
Digital output format (Provide detailed description & timing diagram)					

- What do you want to choose as power supply voltages? For example, the analog VDD needs to be 5V. the digital VDD can be 3.3V/5V.
- What resolution do you need for ADC?
- How about conversion speed (data in $\rightarrow$ data out)?
- How many cycles do exist during the latency of ADC (pipelined delay)?
- What's the input range? And then what do you need between single input and differential input?
- Can the bus interface be compatible with TTL?
- Could you explain external/internal pin configurations as required?

Specially requested function list :

HISTORY CARD

Version	Date	Modified Items	Comments
ver 1.0		Original version published (preliminary)	
ver 1.1			
ver 1.2	2001.02	Release the formal datasheet	
ver 1.3	02.04.27	Add the pin information to the phantom cell information Temperature range is modified	