+2.5 V to +5.5 V, 500μA, Quad Rail-to-Rail, Voltage Output 8/10/12-Bit DACs

Preliminary Technical Data — AD5304/AD5314/AD5324*

FEATURES

AD5304: Four Buffered 8-Bit DACs in One Package
AD5314: Four Buffered 10-Bit DACs in One Package
AD5324: Four Buffered 12-Bit DACs in One Package
10-Lead μSOIC Package
Micropower Operation: 500μA@3V, 600μA@5V
+2.5V to +5.5V Power Supply
Guaranteed Monotonic By Design Over All Codes
Power Down to 50nA@3V, 200nA@5V
Double-Buffered Input Logic
Output Range: 0-V_{REF}
Power-On-Reset to Zero Volts
Simultaneous Update of Outputs ($\overline{LDAC}$ Function)
Low-Power Serial Interface with Schmitt-Triggers
On-Chip Rail-to-Rail Output Buffer Amplifiers
Temperature range -40°C to 105°C.

APPLICATIONS

Portable Battery Powered Instruments
Digital Gain and Offset Adjustment
Programmable Voltage and Current Sources
Programmable Attenuators
Industrial Process Control

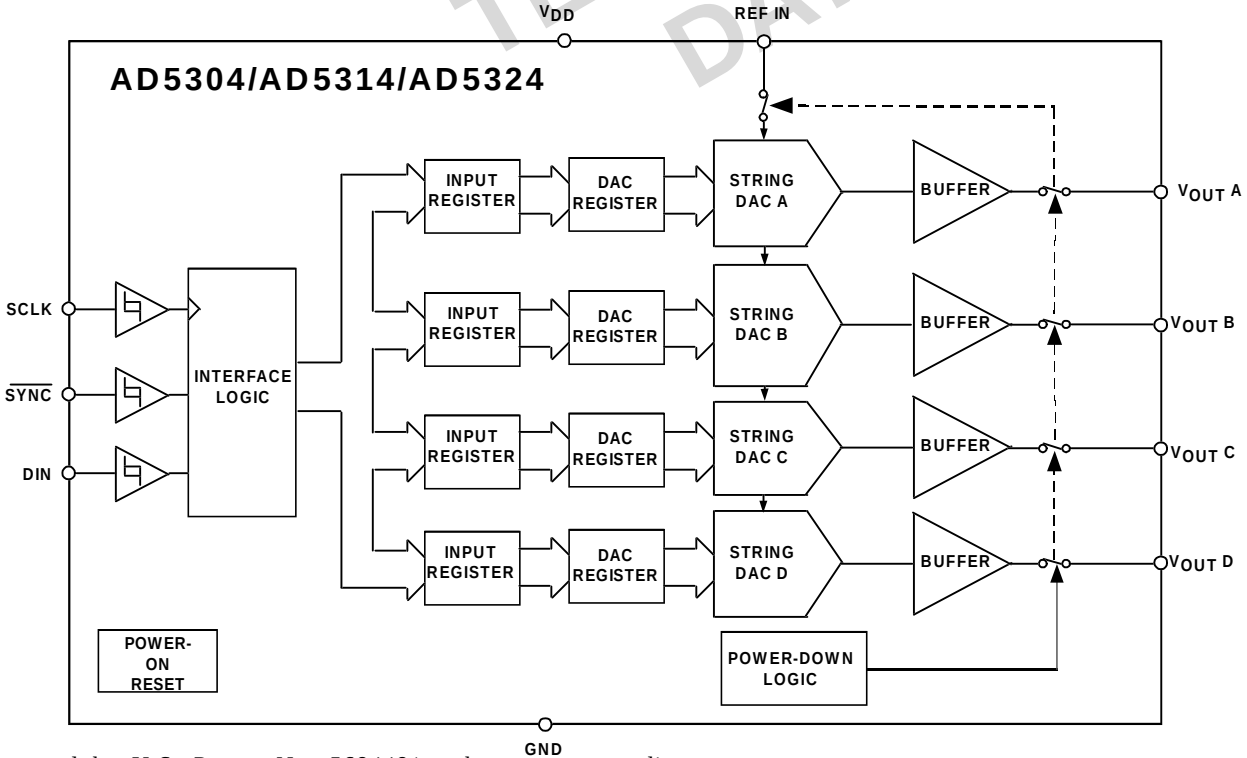
GENERAL DESCRIPTION

The AD5304/AD5314/AD5324 are quad 8, 10 and 12-bit buffered voltage output DACs in a 10-lead μSOIC package which operate from a single +2.5V to +5.5V supply consuming 500μA at 3V. Their on-chip output amplifiers allow rail-to-rail output swing to be achieved with a slew rate of 0.7V/μs. A 3-wire serial interface is used which operates at clock rates up to 30MHz and is compatible with standard SPI™, QSPI™, MICROWIRE™ and DSP interface standards.

The references for the four DACs are derived from one reference pin. The outputs of all DACs may be updated simultaneously using the software $\overline{LDAC}$ function. The parts incorporate a power-on-reset circuit that ensures that the DAC outputs power up to zero volts and remain there until a valid write takes place to the device. The parts contains a power-down feature which reduces the current consumption of the device to 200nA @5V (50nA @3V).

The low power consumption of these parts in normal operation make them ideally suited to portable battery-operated equipment. The power consumption is 3mW at 5V reducing to 1μW in power-down mode.

FUNCTIONAL BLOCK DIAGRAM



*Protected by U.S. Patent No. 5684481; other patents pending

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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 World Wide Web Site: http://www.analog.com
Fax: 781/326-8703 Analog Devices, Inc., 1999

AD5304/AD5314/AD5324–SPECIFICATIONS

(V_{DD} = +2.5V to +5.5 V; V_{REF}=+2V; R_L=2kΩ to GND; C_L=200pFto GND; All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter[1]	B Version[2] Min	Typ	Max	Units	Conditions/Comments
DC PERFORMANCE[3,4]					
AD5304					
Resolution		8		Bits	
Relative Accuracy		±0.15	±1	LSB	
Differential Nonlinearity		±0.02	±0.25	LSB	Guaranteed Monotonic by design over all codes
AD5314					
Resolution		10		Bits	
Relative Accuracy		±0.5	±3	LSB	
Differential Nonlinearity		±0.05	±0.5	LSB	Guaranteed Monotonic by design over all codes
AD5324					
Resolution		12		Bits	
Relative Accuracy		±2	±12	LSB	
Differential Nonlinearity		±0.2	±1	LSB	Guaranteed Monotonic by design over all codes
Offset Error		±0.4	±3	% of FSR	See Figures 2 and 3
Gain Error		±0.15	±1	% of FSR	See Figures 2 and 3
Lower Deadband		10	60	mV	See Figures 2 and 3
Offset Error Drift[5]		-12		ppm of FSR/°C	
Gain Error Drift[5]		-5		ppm of FSR/°C	
Power Supply Rejection Ratio[5]		-60		dB	ΔV_{DD}=±10%
DC Crosstalk[5]		30		µV	
DAC REFERENCE INPUT[5]					
V_{REF} Input Range	0		V_{DD}	V	
V_{REF} Input Impedance		45		kΩ	Normal Operation
		>10		MΩ	Power-Down Mode
Reference Feedthrough		-90		dB	Frequency=10kHz
OUTPUT CHARACTERISTICS[5]					
Minimum Output Voltage[6]		0.001		V	This is a measure of the minimum and maximum drive
Maximum Output Voltage[6]		V_{DD}-0.001		V	capability of the output amplifier
DC Output Impedance		0.5		Ω	
Short Circuit Current		50		mA	V_{DD} = +5V
		20		mA	V_{DD} = +3V
Power Up Time		2.5		µs	Coming out of Power Down Mode. V_{DD} = +5 V
		5		µs	Coming out of Power Down Mode. V_{DD} = +3 V
LOGIC INPUTS[5]					
Input Current			±1	µA	
V_{IL}, Input Low Voltage			0.8	V	V_{DD} = +5V±10%
			0.6	V	V_{DD} = +3V±10%
			0.5	V	V_{DD} = +2.5V
V_{IH}, Input High Voltage	2.4			V	V_{DD} = +5V±10%
	2.1			V	V_{DD} = +3V±10%
	2.0			V	V_{DD} = +2.5V
Pin Capacitance		3		pF	
POWER REQUIREMENTS					
V_{DD}	2.5		5.5	V	I_{DD} spec. is valid for all DAC codes. Interface inactive.
I_{DD} (Normal Mode)					All DACs active. Excluding load currents. CMOS levels.
V_{DD}= +4.5V to +5.5V		0.6	0.9	mA	V_{IH} = V_{DD} and V_{IL} = GND
V_{DD}= +2.5V to +3.6V		0.5	0.7	mA	V_{IH} = V_{DD} and V_{IL} = GND
I_{DD} (Power Down Mode)					
V_{DD} = +4.5V to +5.5V		0.2	1	µA	V_{IH} =V_{DD} and V_{IL}=GND
V_{DD} = +2.5V to +3.6V		0.05	1	µA	V_{IH} =V_{DD} and V_{IL}=GND

NOTES

[1]See Terminology

[2]Temperature ranges are as follows: B Version: -40°C to +105°C.

[3]DC specifications tested with the outputs unloaded.

[4]Linearity is tested using a reduced code range: AD5304 (code 8 to 248); AD5314 (code 28 to 995); AD5324 (code 115 to 3981)

[5]Guaranteed by Design and Characterization, not production tested

[6]In order for the amplifier output to reach its minimum voltage, Offset Error must be negative. In order for the amplifier output to reach its maximum voltage, V_{REF}=V_{DD} and "Offset plus Gain" Error must be positive.

Specifications subject to change without notice.

AC CHARACTERISTICS[1]

(V_{DD} = +2.5V to +5.5 V; R_L=2kΩ to GND; C_L=200pFto GND; All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter[2]	B Version[3] Min	Typ	Max	Units	Conditions/Comments
Output Voltage Settling Time					V_{REF}=V_{DD}=+5V
AD5304		6	8	µs	1/4 Scale to 3/4 Scale change (40 Hex to C0 Hex)
AD5314		7	9	µs	1/4 Scale to 3/4 Scale change (100 Hex to 300 Hex)
AD5324		8	10	µs	1/4 Scale to 3/4 Scale change (400 Hex to C00 Hex)
Slew Rate		0.7		V/µs	
Major-Code Change Glitch Impulse		12		nV-s	1 LSB change around major carry.
Digital Feedthrough		0.10		nV-s	
DAC-to-DAC Crosstalk		0.01		nV-s	
Multiplying Bandwidth		200		kHz	V_{REF}=2V±0.1Vpp
Total Harmonic Distortion		-70		dB	V_{REF}=2.5V±Vpp. Frequency=10kHz.

NOTES
[1]Guaranteed by Design and Characterization, not production tested
[2]See Terminology
[3]Temperature range for B Version: -40°C to +105°C.
Specifications subject to change without notice.

TIMING CHARACTERISTICS[1,2,3]

(V_{DD} = +2.5 V to +5.5 V. All specifications T_{MIN} to T_{MAX} unless otherwise noted)

Parameter	Limit at T_{MIN}, T_{MAX} (B Version)	Units	Conditions/Comments
t_1	33	ns min	SCLK Cycle Time
t_2	13	ns min	SCLK High Time
t_3	13	ns min	$\overline{\text{SCLK}}$ Low Time
t_4	0	ns min	$\overline{\text{SYNC}}$ to SCLK Rising Edge Setup Time
t_5	5	ns min	Data Setup Time
t_6	4.5	ns min	Data Hold Time
t_7	0	ns min	SCLK Falling Edge to $\overline{\text{SYNC}}$ Rising Edge
t_8	33	ns min	Minimum $\overline{\text{SYNC}}$ High Time

NOTES
[1]Guaranteed by Design and Characterization, not production tested.
[2]All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of (V_{IL} + V_{IH})/2.
[3]See Figure 1.

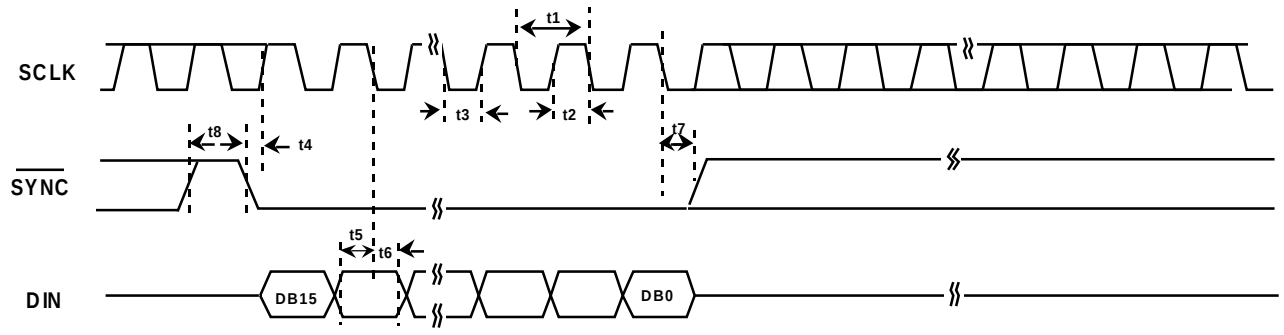


Figure 1. Serial Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS[1,2]

(T_A = +25°C unless otherwise noted)

V_{DD} to GND.....-0.3V to +7V
Digital Input Voltage to GND.....-0.3V to V_{DD} + 0.3V
Reference Input Voltage to GND.....-0.3V to V_{DD} +0.3V
V_{OUT}A-D to GND.....-0.3 V to V_{DD} + 0.3V
Operating Temperature Range
Industrial (B Version).....-40°C to +105°C
Storage Temperature Range.....-65°C to +150°C
Junction Temperature (T_J max) .....+150°C

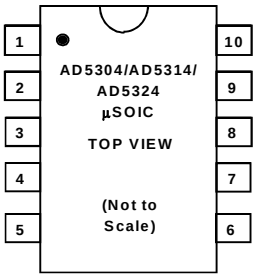
10-Lead MicroSOIC Package
Power Dissipation.....(T_J max - T_A) / θ_{JA}
θ_{JA} Thermal Impedance .....206°C /W
Lead Temperature, Soldering
Vapor Phase (60 sec) ..... +215°C
Infrared (15 sec) ..... +220°C

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Transient currents of up to 100mA will not cause SCR latch-up

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD5304/AD5314/AD5324 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION



ORDERING GUIDE

Model	Temperature Range	Package Option*	Branding Information
AD5304BRM	-40°C to +105°C	RM-10	DBB
AD5314BRM	-40°C to +105°C	RM-10	DCB
AD5324BRM	-40°C to +105°C	RM-10	DDB

*RM = MicroSOIC.

PIN FUNCTION DESCRIPTION

PIN NUMBERS

Pin No.	Mnemonic	Function
1	V_{DD}	Power Supply Input. These parts can be operated from +2.5V to +5.5V and the supply should be decoupled to GND.
2	V_{OUT}A	Buffered analog output voltage from DAC A. The output amplifier has rail-to-rail operation.
3	V_{OUT}B	Buffered analog output voltage from DAC B. The output amplifier has rail-to-rail operation.
4	V_{OUT}C	Buffered analog output voltage from DAC C. The output amplifier has rail-to-rail operation.
5	V_{REF}	Reference Input pin for all four DACs. It has an input range from 0V to V_{DD}.
6	V_{OUT}D	Buffered analog output voltage from DAC D. The output amplifier has rail-to-rail operation.
7	GND	Ground reference point for all circuitry on the part.
8	DIN	Serial Data Input. This device has a 16-bit shift register. Data is clocked into the register on the falling edge of the serial clock input. The DIN input buffer is powered-down after each write cycle.
9	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at rates up to 30MHz. The SCLK input buffer is powered-down after each write cycle.
10	$\overline{SYNC}$	Active Low Control Input. This is the frame synchronization signal for the input data. When $\overline{SYNC}$ goes low, it enables the input shift register and data is transferred in on the falling edges of the fol lowing 16 clocks. If $\overline{SYNC}$ is taken high before the 16th falling edge of SCLK, the rising edge of $\overline{SYNC}$ acts as an interrupt and the write sequence is ignored by the device.

TERMINOLOGY

RELATIVE ACCURACY

For the DAC, Relative Accuracy or Integral Nonlinearity (INL) is a measure of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function. A typical INL vs. Code plot can be seen in Figure x.

DIFFERENTIAL NONLINEARITY

Differential Nonlinearity (DNL) is the difference between the measured change and the ideal 1LSB change between any two adjacent codes. A specified differential nonlinearity of ±1LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design. A typical DNL vs. Code plot can be seen in Figure x.

OFFSET ERROR

This is a measure of the offset error of the DAC and the output amplifier. It is expressed as a percentage of the full-scale range.

GAIN ERROR

This is a measure of the span error of the DAC. It is the deviation in slope of the actual DAC transfer characteristic from the ideal expressed as a percentage of the full-scale range.

OFFSET ERROR DRIFT

This is a measure of the change in Offset Error with changes in temperature. It is expressed in (ppm of Full-Scale Range)/°C.

GAIN ERROR DRIFT

This is a measure of the change in gain error with changes in temperature. It is expressed in (ppm of Full-Scale Range)/°C.

POWER-SUPPLY REJECTION RATIO (PSRR)

This indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is the ratio of the change in V_{OUT} to a change in V_{DD} for full-scale output of the DAC. It is measured in dBs. V_{REF} is held at +2V and V_{DD} is varied ± 10%.

DC CROSSTALK

This is the DC change in the output level of one DAC in response to a change in the output of the other DAC. It is measured with a full-scale output change on one DAC while monitoring the other DAC. It is expressed in mV.

REFERENCE FEEDTHROUGH

This is the ratio of the amplitude of the signal at the DAC output to the reference input when the DAC output is not being updated. It is expressed in dBs.

MAJOR-CODE TRANSITION GLITCH ENERGY

Major-Code Transition Glitch Energy is the energy of the impulse injected into the analog output when the code in the DAC register changes state. It is normally specified as the area of the glitch in nV-secs and is measured when the digital code is changed by 1LSB at the major carry transition (011...11 to 100...00 or 100...00 to 011...11).

DIGITAL FEEDTHROUGH

Digital Feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital input pins of the device when the DAC output is not being updated. It is specified in nV-secs and is measured with a worst-case change on the digital input pins, e.g. from all 0s to all 1s and vice versa.

DAC-TO-DAC CROSSTALK

This is the glitch impulse transferred to the output of one DAC due to a digital code change and subsequent output change of another DAC. This includes both digital and analog crosstalk. It is measured by loading one of the DACs with a full-scale code change (all 0s to all 1s and vice versa) with the $\overline{\text{LDAC}}$ bit set low and monitoring the output of another DAC. The energy of the glitch is expressed in nV-secs.

MULTIPLYING BANDWIDTH

The amplifiers within the DAC have a finite bandwidth. The Multiplying Bandwidth is a measure of this. A sine wave on the reference (with full-scale code loaded to the DAC) appears on the output. The Multiplying Bandwidth is the frequency at which the output amplitude falls to 3dB below the input.

TOTAL HARMONIC DISTORTION

This is the difference between an ideal sine wave and its attenuated version using the DAC. The sine wave is used as the reference for the DAC and the THD is a measure of the harmonics present on the DAC output. It is measured in dBs.

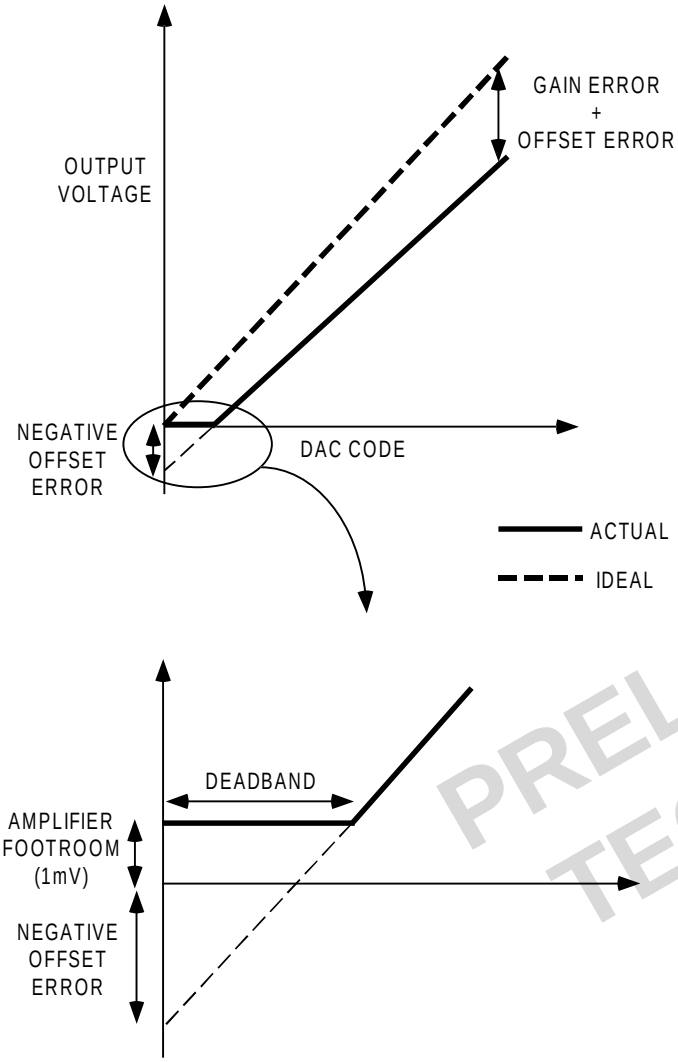


Figure 2. Transfer Function with Negative Offset

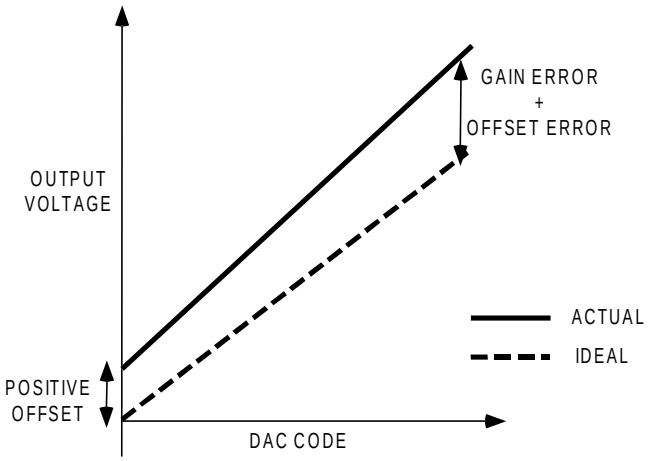


Figure 3. Transfer Function with Positive Offset

FUNCTIONAL DESCRIPTION

The AD5304/AD5314/AD5324 are quad resistor-string DACs fabricated on a CMOS process with resolutions of 8, 10 and 12 bits respectively. Each contains four output buffer amplifiers and each is written to via a 3-wire serial interface. They operate from single supplies of +2.5V to +5.5V and the output buffer amplifiers provide rail-to-rail output swing with a slew rate of 0.7V/µs. The four DACs share a single reference input pin. The devices have a programmable power-down mode, in which all DACs may be turned off completely with a high-impedance output.

Digital-to-Analog Section

The architecture of one DAC channel consists of a resistor-string DAC followed by an output buffer amplifier. The voltage at the V_{REF} pin provides the reference voltage for the DAC. Figure 4 shows a block diagram of the DAC architecture. Since the input coding to the DAC is straight binary, the ideal output voltage is given by:

$$V_{OUT} = \frac{V_{REF} * D}{2^N}$$

where D=decimal equivalent of the binary code which is loaded to the DAC register;

0-255 for AD5304 (8-bits)
0-1023 for AD5314 (10-bits)
0-4095 for AD5324 (12-bits)

N = DAC resolution

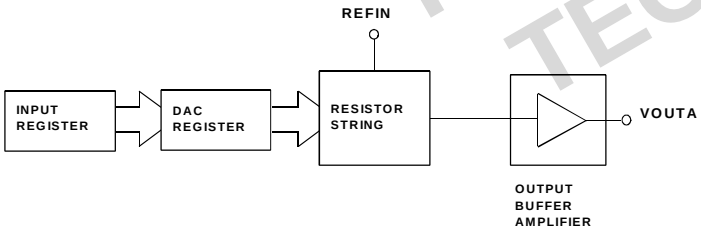


Figure 4. DAC channel architecture

Resistor String

The resistor string section is shown in Figure 5. It is simply a string of resistors, each of value R. The digital code loaded to the DAC register determines at what node on the string the voltage is tapped off to be fed into the output amplifier. The voltage is tapped off by closing one of the switches connecting the string to the amplifier. Because it is a string of resistors, it is guaranteed monotonic.

DAC Reference Inputs

There is a single reference input pin for the four DACs. The reference input is unbuffered. The user can have a reference voltage as low as GND and as high as V_{DD} since there is no restriction due to headroom and footroom of the reference amplifier.

It is recommended to use a buffered reference in the external circuit (e.g. REF192). The input impedance is typically 180kΩ.

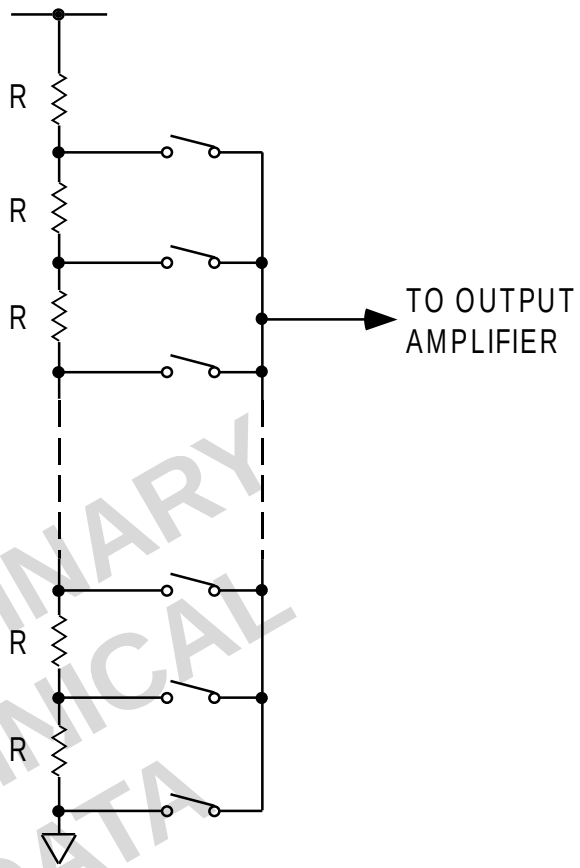


Figure 5. Resistor String

Output Amplifier

The output buffer amplifier is capable of generating rail-to-rail voltages on its output which gives an output range of 0V to V_{DD} when the reference is V_{DD}. It is capable of driving a load of 2kΩ to GND or $V_{DD,}$ in parallel with 500pF to an AC GND. The source and sink capabilities of the output amplifier can be seen in Figure x. The slew rate is 0.7V/µs with a half-scale settling time to +/-0.5 LSB (at 8 bits) of 6µs.

POWER-ON RESET

The A5304/AD5314/AD5324 are provided with a power-on reset function, so that they power up in a defined state. The power-on state is:

- Normal operation
- Output voltage set to 0V

Both input and DAC registers are filled with zeros and remain so until a valid write sequence is made to the device. This is particularly useful in applications where it is important to know the state of the DAC outputs while the device is powering-up.

SERIAL INTERFACE

The AD5304/AD5314/AD5324 are controlled over a versatile, 3-wire serial interface, which operates at clock rates up to 30MHz and is compatible with SPI™, QSPI™, MICROWIRE™ and DSP interface standards.

Input Shift Register

The input shift register is 16-bits wide. Data is loaded into the device as a 16-bit word under the control of a serial clock input, SCLK. The timing diagram for this operation is shown in Figure 1 on page 3. The 16-bit word consists of four control bits followed by 8, 10 or 12 bits of DAC data, depending on the device type. The first two bits loaded are the Bit 15 (MSB) and Bit 14. These determine whether the data is for DAC A, DAC B, DAC C or DAC D. Bit 13 is $\overline{PD}$ which determines whether the part is in Normal or Power-Down mode. Bit 12 is $\overline{LDAC}$ which controls when DAC registers and outputs are updated. Bits 13 and 12 control the operating mode of the DAC.

TABLE 1. ADDRESS BITS FOR THE AD53X4

A1	A0	DAC Addressed
0	0	DAC A
0	1	DAC B
1	0	DAC C
1	1	DAC D

Address and Control bits

$\overline{PD}$: 0: All four DACs go into Power-Down mode consuming only 200nA @ 5V. The DAC outputs enter a high-impedance state.
1:Normal operation.

$\overline{LDAC}$: 0:All four DAC registers and hence all DAC outputs updated simultaneously on completion of the write sequence.
1: Addressed input register only is updated. There is no change in the contents of the DAC registers.

The AD5324 uses all 12 bits of DAC data, the AD5314 uses 10 bits and ignores the two LSBs. The AD5304 uses 8 bits and ignores the last 4 bits. The data format is straight binary, with all zeros corresponding to 0V output and all ones corresponding to full-scale output (V_{REF} - 1LSB).

The $\overline{SYNC}$ input is a level-triggered input that acts as a frame synchronization signal and chip enable. Data can only be transferred into the device whilst $\overline{SYNC}$ is low. To start the serial data transfer, $\overline{SYNC}$ should be taken low observing the minimum $\overline{SYNC}$ to SCLK active edge setup time, t_4. After $\overline{SYNC}$ goes low, serial data will be shifted into the device's input shift register on the falling edges of SCLK for 16 clock pulses. Any data and clock pulses after the 16th falling edge of SCLK will be ignored because the SCLK and DIN input buffers are powered down. No further serial data transfer will occur until $\overline{SYNC}$ is taken high and low again.

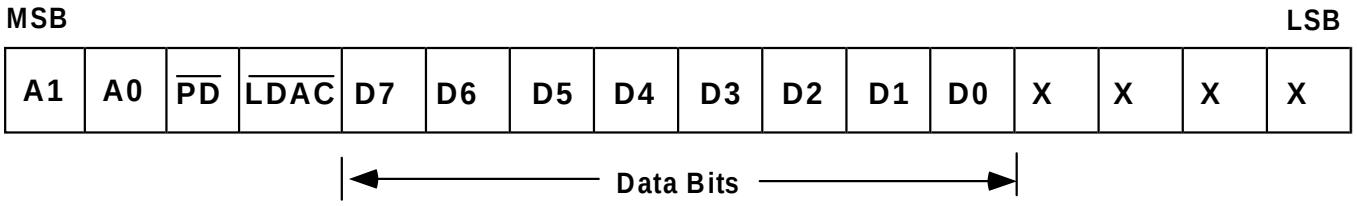


Figure 6. AD5304 Input Shift Register Contents

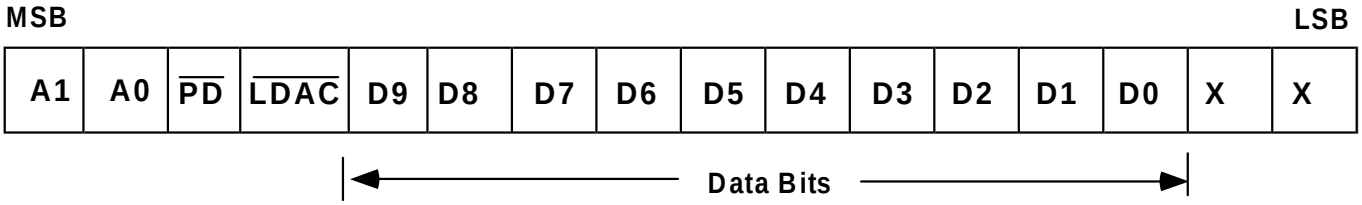


Figure 7. AD5314 Input Shift Register Contents

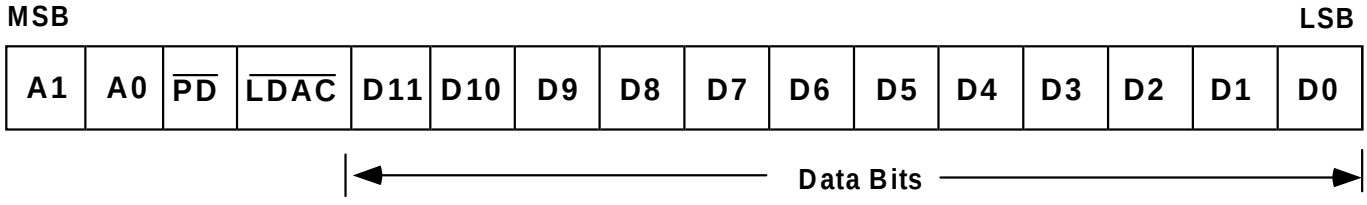


Figure 8. AD5324 Input Shift Register Contents

$\overline{SYNC}$ may be taken high after the falling edge of the 16th SCLK pulse, observing the minimum SCLK falling edge to $\overline{SYNC}$ rising edge time, t_7.

After the end of serial data transfer, data will automatically be transferred from the input shift register to the input register of the selected DAC. If $\overline{SYNC}$ is taken high before the 16th falling edge of SCLK, the data transfer will be aborted and the DAC input registers will not be updated.

When data has been transferred into three of the DAC input registers, all DAC registers and all DAC outputs may be updated simultaneously, by setting $\overline{LDAC}$ low when writing to the remaining DAC input register.

Low-Power Serial Interface

To reduce the power consumption of the device even further, the interface only powers-up fully when the device is being written to. As soon as the 16-bit control word has been written to the part, the SCLK and DIN input buffers are powered-down. They only power-up again following a falling edge of $\overline{SYNC}$.

Double-Buffered Interface

The AD5304/AD5314/AD5324 DACs all have double-buffered interfaces consisting of two banks of registers - input registers and DAC registers. The input register is connected directly to the input shift register and the digital code is transferred to the relevant input register on completion of a valid write sequence. The DAC register contains the digital code which the resistor string uses.

Access to the DAC register is controlled by the $\overline{LDAC}$ bit. When the $\overline{LDAC}$ bit is set high, the DAC register is latched and hence the input register may change state without affecting the contents of the DAC register. However, when the $\overline{LDAC}$ bit is set low, all DAC registers are updated after a complete write sequence.

This is useful if the user requires simultaneous updating of all DAC outputs. The user may write to three of the input registers individually and then, by setting the $\overline{LDAC}$ bit low when writing to the remaining DAC input register, all outputs will update simultaneously.

These parts contain an extra feature whereby the DAC register is not updated unless its input register has been updated since the last time that $\overline{LDAC}$ was brought low. Normally, when $\overline{LDAC}$ is brought low, the DAC registers are filled with the contents of the input registers. In the case of the AD5304/AD5314/AD5324, the part will only update the DAC register if the input register has been changed since the last time the DAC register was updated thereby removing unnecessary digital crosstalk.

POWER-DOWN MODE

The AD5304/AD5314/AD5324 have low power consumption, dissipating only 1.5mW with a 3V supply and 3mW with a 5V supply. Power consumption can further be reduced when the DACs are not in use by putting them into power-down mode, which is selected by bit 13 ($\overline{PD}$) of the control word.

When the $\overline{PD}$ bit is set to 1, the relevant DAC works normally with its normal power consumption of approx 150µA at 5V. However, in power-down mode, the supply current falls to 200nA at 5V (50nA at 3V) when all DACs are powered-down. Not only does the supply current drop but the output stage is also internally switched from the output of the amplifier to a resistor network of known values. This has the advantage that the output impedance of the part is known while the part is in power-down mode and provides a defined input condition for whatever is connected to the output of the DAC amplifier. The output stage is illustrated in Figure x.

The bias generator, the output amplifier, the resistor string and all other associated linear circuitry are all shut down when the power-down mode is activated. However, the contents of the registers are unaffected when in power-down. The time to exit power-down is typically 2.5µs for V_{DD}=5V and 5µs when V_{DD}=3V.

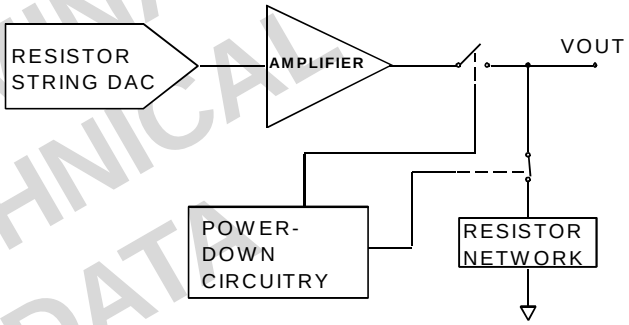
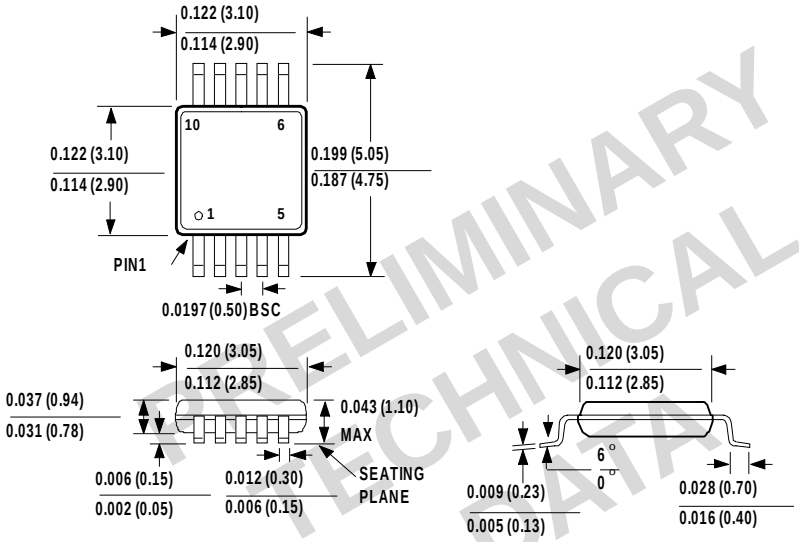


Figure 9. Output Stage during Power-Down

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

10-Lead MicroSOIC (RM-10)



OVERVIEW OF ALL AD53xx SERIAL DEVICES

Part no.	Resolution	No. of DACS	DNL	Interface	Settling Time	Package	Pins
				SINGLES			
AD5300	8	1	±0.25	SPI	4 µs	SOT-23,µSOIC	6,8
AD5310	10	1	±0.5	SPI	6 µs	SOT-23,µSOIC	6,8
AD5320	12	1	±1.0	SPI	8 µs	SOT-23,µSOIC	6,8
AD5301	8	1	±0.25	2-wire	6 µs	SOT-23,µSOIC	6,8
AD5311	10	1	±0.5	2-wire	7 µs	SOT-23,µSOIC	6,8
AD5321	12	1	±1.0	2-wire	8 µs	SOT-23,µSOIC	6,8
				DUALS			
AD5302	8	2	±0.25	SPI	6 µs	µSOIC	8
AD5312	10	2	±0.5	SPI	7 µs	µSOIC	8
AD5322	12	2	±1.0	SPI	8 µs	µSOIC	8
AD5303	8	2	±0.25	SPI	6 µs	TSSOP	16
AD5313	10	2	±0.5	SPI	7 µs	TSSOP	16
AD5323	12	2	±1.0	SPI	8 µs	TSSOP	16
				QUADS			
AD5304	8	4	±0.25	SPI	6 µs	µSOIC	10
AD5314	10	4	±0.5	SPI	7 µs	µSOIC	10
AD5324	12	4	±1.0	SPI	8 µs	µSOIC	10
AD5305	8	4	±0.25	2-wire	6 µs	µSOIC	10
AD5315	10	4	±0.5	2-wire	7 µs	µSOIC	10
AD5325	12	4	±1.0	2-wire	8 µs	µSOIC	10
AD5306	8	4	±0.25	2-wire	6 µs	TSSOP	16
AD5316	10	4	±0.5	2-wire	7 µs	TSSOP	16
AD5326	12	4	±1.0	2-wire	8 µs	TSSOP	16
AD5307	8	4	±0.25	SPI	6 µs	TSSOP	16
AD5317	10	4	±0.5	SPI	7 µs	TSSOP	16
AD5327	12	4	±1.0	SPI	8 µs	TSSOP	16