Octal D-type transparent latch with 5-volt tolerant inputs/outputs; 3-State

74LVC373A
74LVCH373A

FEATURES

- 5-volt tolerant inputs/outputs, for interfacing with 5-volt logic
- Supply voltage range of 2.7V to 3.6V
- Complies with JEDEC standard no. 8-1A
- CMOS low power consumption
- Direct interface with TTL levels
- High impedance when V_{CC} = 0V
- Bushold on all data inputs (LVCH373A only)

DESCRIPTION

The 74LVC(H)373A is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3V or 5V devices. In 3-State operation, outputs can handle 5V. This feature allows the use of these devices as translators in a mixed 3.3V/5V environment.

The 74LVC(H)373A is an octal D-type transparent latch featuring separate D-type inputs for each latch and 3-State outputs for bus-oriented applications. A latch enable (LE) input and an output enable ($\overline{OE}$) input are common to all internal latches.

The '373' consists of eight D-type transparent latches with 3-State true outputs. When LE is HIGH, data at the D_n inputs enters the latches. In this condition, the latches are transparent, i.e. a latch output will change each time its corresponding D-input changes. When LE is LOW, the latches store the information that was present at the D-inputs one setup time preceding the HIGH-to-LOW transition of LE. When $\overline{OE}$ is LOW, the contents of the eight latches are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the latches.

The '373' is functionally identical to the '573', but the '573' has a different pin arrangement.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay D_n to Q_n; LE to Q_n	C_L = 50pF V_{CC} = 3.3V	 4.2 4.6	ns
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per latch	Notes 1 and 2	20	pF

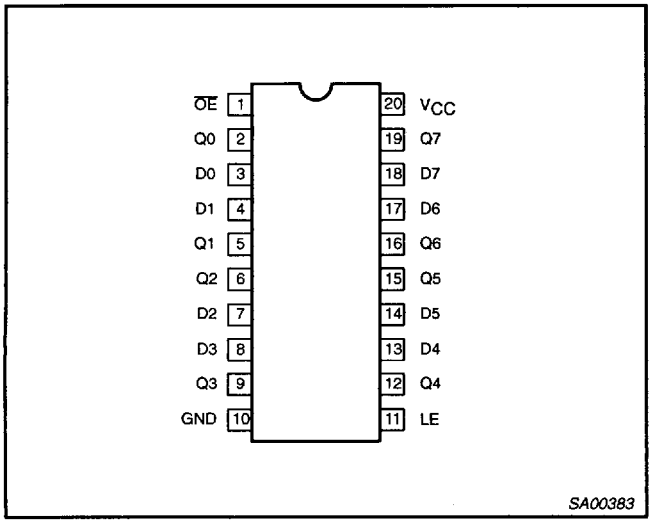
NOTE:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}

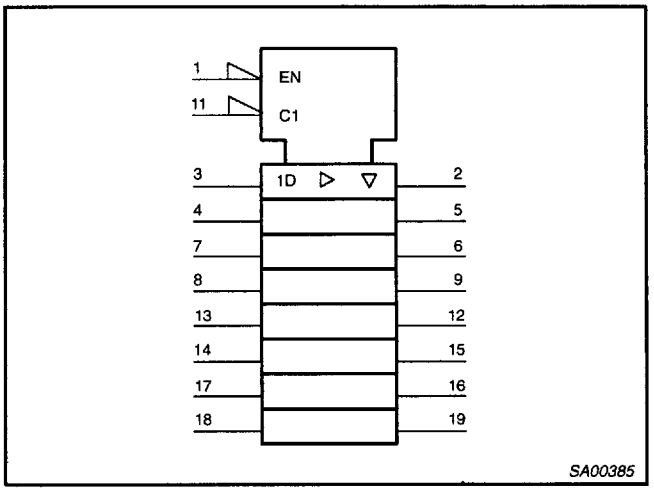
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
20-Pin Plastic Shrink Small Outline (SO)	–40°C to +85°C	74LVC373AD	74LVC373AD	SOT163-1
20-Pin Plastic Shrink Small Outline (SSOP) Type II	–40°C to +85°C	74LVC373ADB	74LVC373ADB	SOT339-1
20-Pin Plastic Thin Shrink Small Outline (TSSOP) Type I	–40°C to +85°C	74LVC373APW	7LVC373APW DH	SOT360-1
20-Pin Plastic Shrink Small Outline (SO)	–40°C to +85°C	74LVCH373AD	74LVCH373A D	SOT163-1
20-Pin Plastic Shrink Small Outline (SSOP) Type II	–40°C to +85°C	74LVCH373ADB	74LVCH373A DB	SOT339-1
20-Pin Plastic Thin Shrink Small Outline (TSSOP) Type I	–40°C to +85°C	74LVCH373APW	LVCH373APW DH	SOT360-1

PIN CONFIGURATION



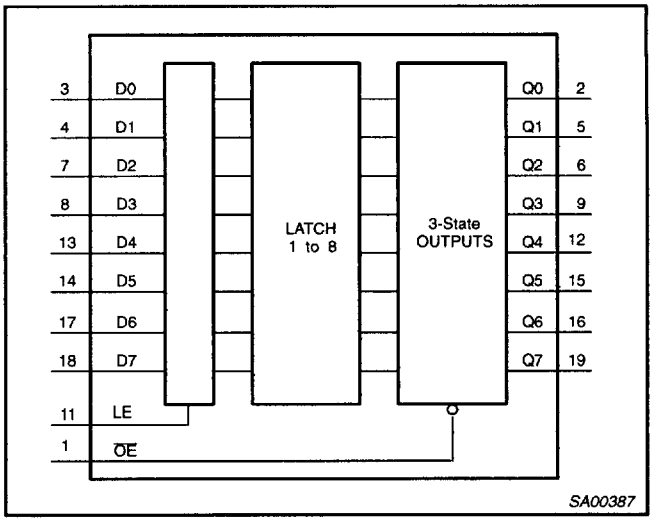
LOGIC SYMBOL (IEEE/IEC)



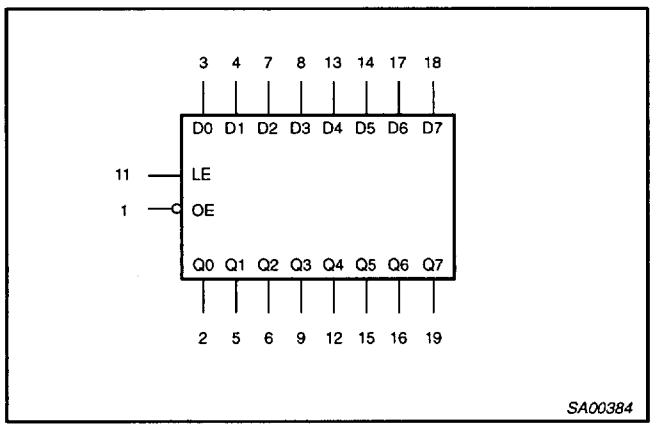
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{OE}$	Output enable input (active-Low)
3, 4, 7, 8, 13, 14, 17, 18	D0-D7	Data inputs
2, 5, 6, 9, 12, 15, 16, 19	Q0-Q7	Data outputs
11	LE	Latch enable input (active-High)
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

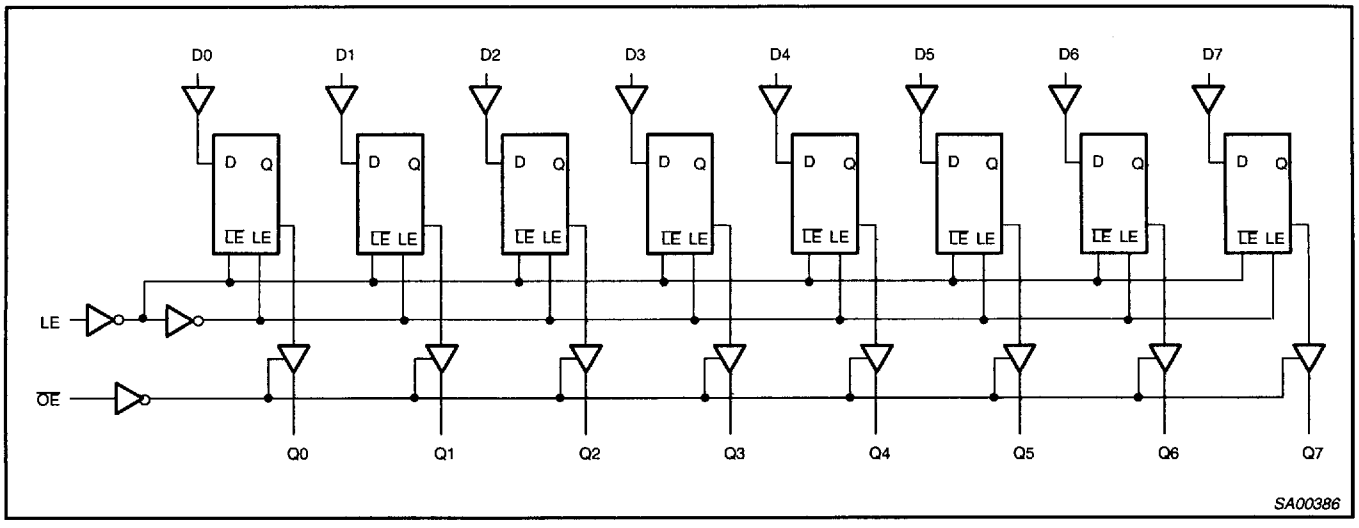
FUNCTIONAL DIAGRAM



LOGIC SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL LATCHES	OUTPUTS
	$\overline{OE}$	LE	D_n		Q_0 to Q_7
Enable and read register (transparent mode)	L L	H H	L H	L H	L H
Latch and read register	L L	L L	l h	L H	H H
Latch register and disable outputs	H H	L L	l h	L H	Z Z

H = HIGH voltage level
h = HIGH voltage level one setup time prior to the HIGH-to-LOW LE transition
L = LOW voltage level
l = LOW voltage level one setup time prior to the HIGH-to-LOW LE transition
X = Don't care
Z = High impedance OFF-state

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
V_{CC}	DC supply voltage (for low-voltage applications)		1.2	3.6	V
V_I	DC Input voltage range		0	5.5	V
V_O	DC Output voltage range; output HIGH or LOW state		0	V_{CC}	V
V_O	DC output voltage range; output 3-State		0	5.5	V
T_{amb}	Operating ambient temperature range in free-air		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.2 to 2.7V V_{CC} = 2.7 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS[1]

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +6.5	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage	Note 2	–0.5 to +6.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
V_{OUT}	DC output voltage; output HIGH or LOW state	Note 2	–0.5 to V_{CC} +0.5	V
V_{OUT}	DC output voltage; output 3-State	Note 2	–0.5 to 6.5	V
I_{OUT}	DC output source or sink current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		–60 to +150	°C
P_{TOT}	Power dissipation per package –plastic mini-pack (SO) –plastic shrink mini-pack (SSOP and TSSOP)	 above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 500 500	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	V_{CC}			V
		V_{CC} = 2.7 to 3.6V	2.0			
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			GND	V
		V_{CC} = 2.7 to 3.6V			0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = –12mA	V_{CC} – 0.5			V
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –100µA	V_{CC} – 0.2	V_{CC}		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –18mA	V_{CC} – 0.6			
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –24mA	V_{CC} – 0.8			
V_{OL}	LOW level output voltage	V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA			0.40	V
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		GND	0.20	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 24mA			0.55	
I_I	Input leakage current[6]	V_{CC} = 3.6V; V_I = 5.5V or GND; Not for I/O pins		±0.1	±5	µA
I_{IHZ}/I_{ILZ}	Input current for common I/O pins[6]	V_{CC} = 3.6V; V_I = 5.5V or GND		±0.1	±15	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 3.6V; $V_I = V_{IH}$ or V_{IL}; V_O = 5.5V or GND		0.1	±10	µA
I_{off}	Power off leakage supply	V_{CC} = 0.0V; V_I or V_O = 5.5V		0.1	±10	µA
I_{CC}	Quiescent supply current	V_{CC} = 3.6V; $V_I = V_{CC}$ or GND; I_O = 0		0.1	20	µA
ΔI_{CC}	Additional quiescent supply current per input pin	V_{CC} = 2.7V to 3.6V; $V_I = V_{CC}$ –0.6V; I_O = 0		5	500	µA
I_{BHL}	Bushold LOW sustaining current[2, 3, 4]	V_{CC} = 3.0V; V_I =0.8V	75	–	–	µA
I_{BHH}	Bushold HIGH sustaining current[2, 3, 4]	V_{CC} = 3.0V; V_I =2.0V	–75	–	–	µA
I_{BHLO}	Bushold LOW overdrive current[2, 3, 5]	V_{CC} = 3.6V	500	–	–	µA
I_{BHHO}	Bushold HIGH overdrive current[2, 3, 5]	V_{CC} = 3.6V	–500	–	–	µA

NOTES:

1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. Valid for data inputs of bushold parts (LVCH-A) only.
3. For data inputs only, control inputs do not have a bushold circuit.
4. The specified sustaining current at the data inputs do not have a bushold circuit.
5. The specified overdrive current at the data input forces the data input to the opposite logic input state.
6. For bushold parts, the bushold circuit is switched off when V_I exceeds V_{CC} allowing 5.5V on the input terminal.

AC CHARACTERISTICS

GND = 0V; $t_r = t_f \leq 2.5$ns; $C_L = 50$pF; $R_L = 500\Omega$; $T_{amb} = -40°C$ to $+85°C$.

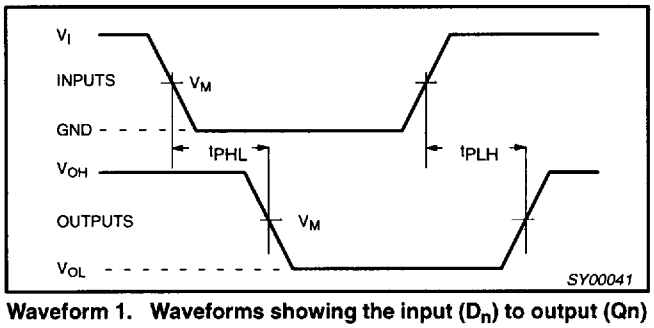
SYMBOL	PARAMETER	WAVEFORM	LIMITS						UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V		V_{CC} = 1.2V	
			MIN	TYP[1]	MAX	MIN	MAX	TYP	
t_{PHL} t_{PLH}	Propagation delay D_n to Q_n	1, 5	1.5	4.2	6.8	1.5	7.8	19	ns
t_{PHL} t_{PLH}	Propagation delay LE to Q_n	2, 5	1.5	4.6	7.2	1.5	8.2	21	ns
t_{PZH} t_{PZL}	3-State output enable time $\overline{OE}$ to Q_n	3, 5	1.5	4.8	7.7	1.5	8.7	22	ns
t_{PHZ} t_{PLZ}	3-State output disable time $\overline{OE}$ to Q_n	3, 5	1.5	4.3	6.1	1.5	7.1	15	ns
t_W	LE pulse width HIGH	2	3.0	1.5	–	3.0	–	–	ns
t_{SU}	Setup time D_n to LE	4	2.0	0	–	2.0	–	–	ns
t_h	Hold time D_n to LE	4	1.5	0.3	–	1.5	–	–	ns

NOTE:

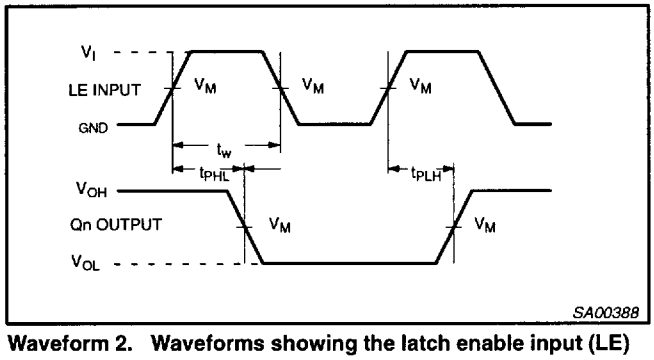
1. Unless otherwise stated, all typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

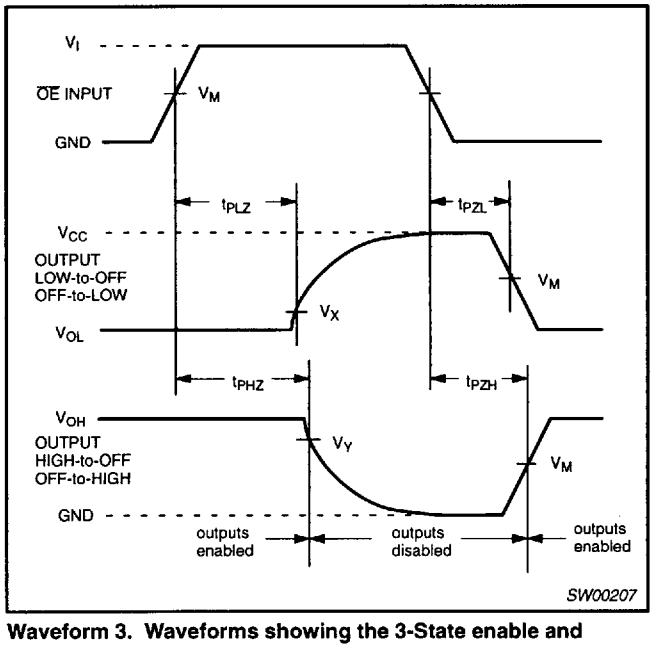
V_M = 1.5V at $V_{CC} \geq 2.7$V; $V_M = 0.5\ V_{CC}$ at $V_{CC} < 2.7$V.
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
$V_X = V_{OL} + 0.3$V at $V_{CC} \geq 2.7$V; $V_X = V_{OL} + 0.1\ V_{CC}$ at $V_{CC} < 2.7$V
$V_Y = V_{OH} - 0.3$V at $V_{CC} \geq 2.7$V; $V_Y = V_{OH} - 0.1\ V_{CC}$ at $V_{CC} < 2.7$V



Waveform 1. Waveforms showing the input (D_n) to output (Qn) propagation delays.

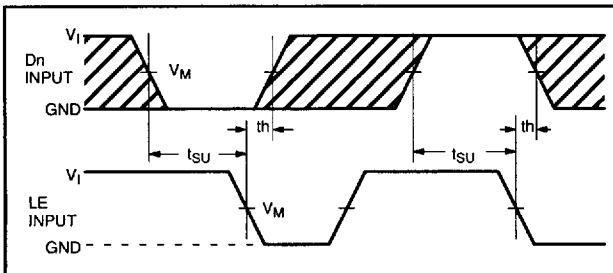


Waveform 2. Waveforms showing the latch enable input (LE) pulse width, the latch enable input to output (Q_n) propagation delays



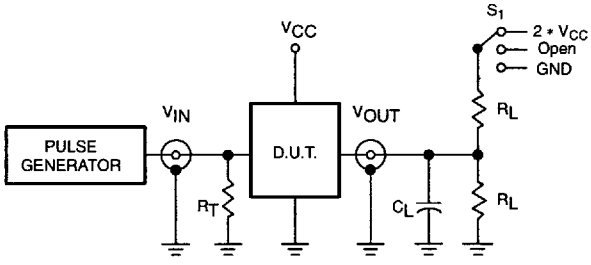
Waveform 3. Waveforms showing the 3-State enable and disable times.

AC WAVEFORMS



Waveform 4. Waveforms showing the data setup and hold times for the D_n input to the LE input. (The shaded areas indicate when the input is permitted to change for predictable output performance).

TEST CIRCUIT



Test Circuit for 3-State Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 * V_{CC}
t_{PHZ}/t_{PZH}	GND

V_{CC}	V_I
< 2.7V	V_{CC}
2.7 – 3.6V	2.7V

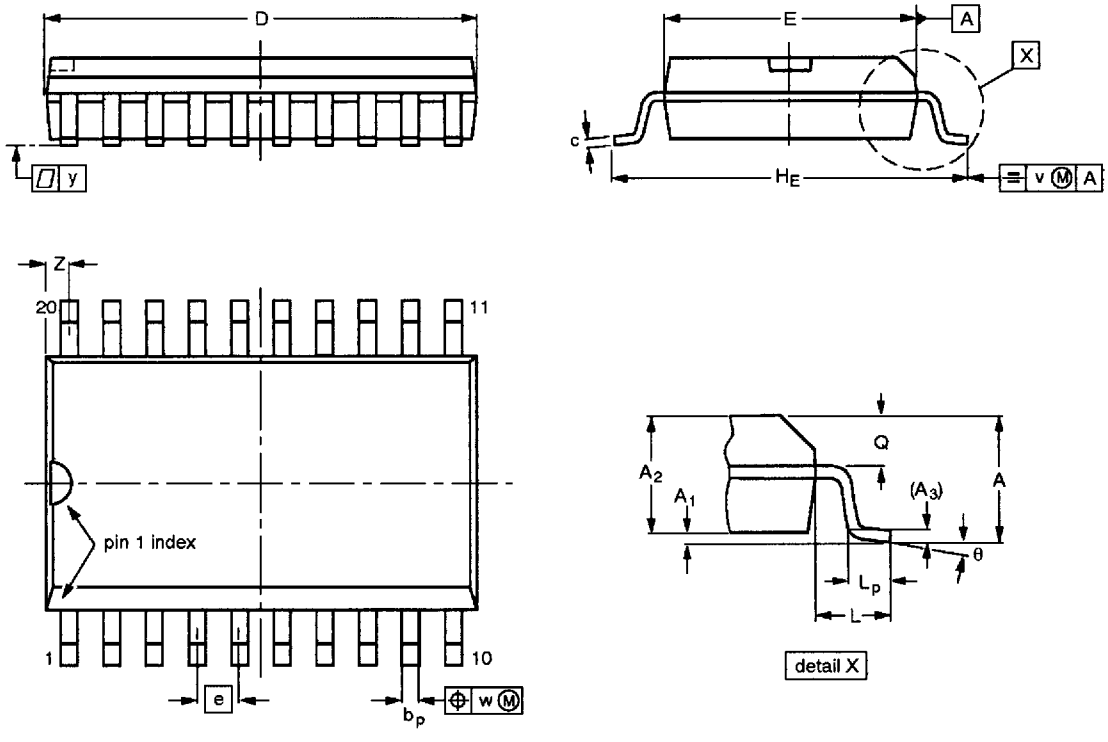
DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SW00047

Waveform 5. Load circuitry for switching times.

SO20: plastic small outline package; 20 leads; body width 7.5 mm SOT163-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

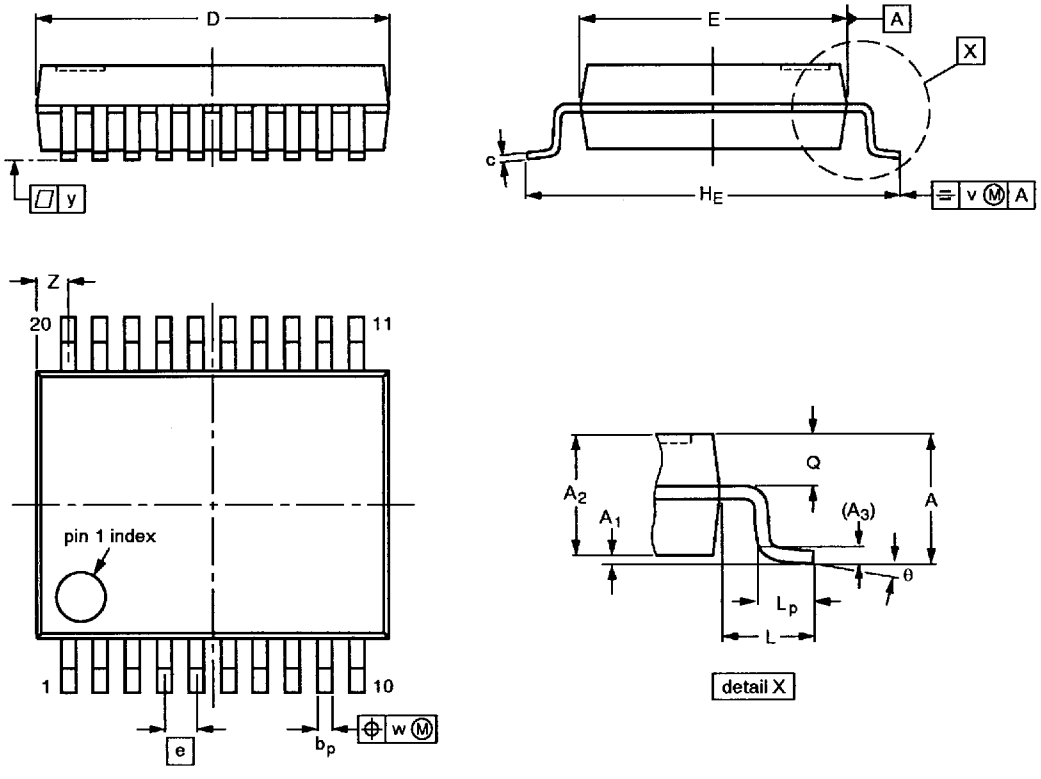
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

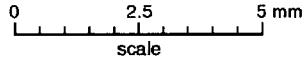
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				~~92-11-17~~ 95-01-24

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm SOT339-1





DIMENSIONS (mm are the original dimensions)

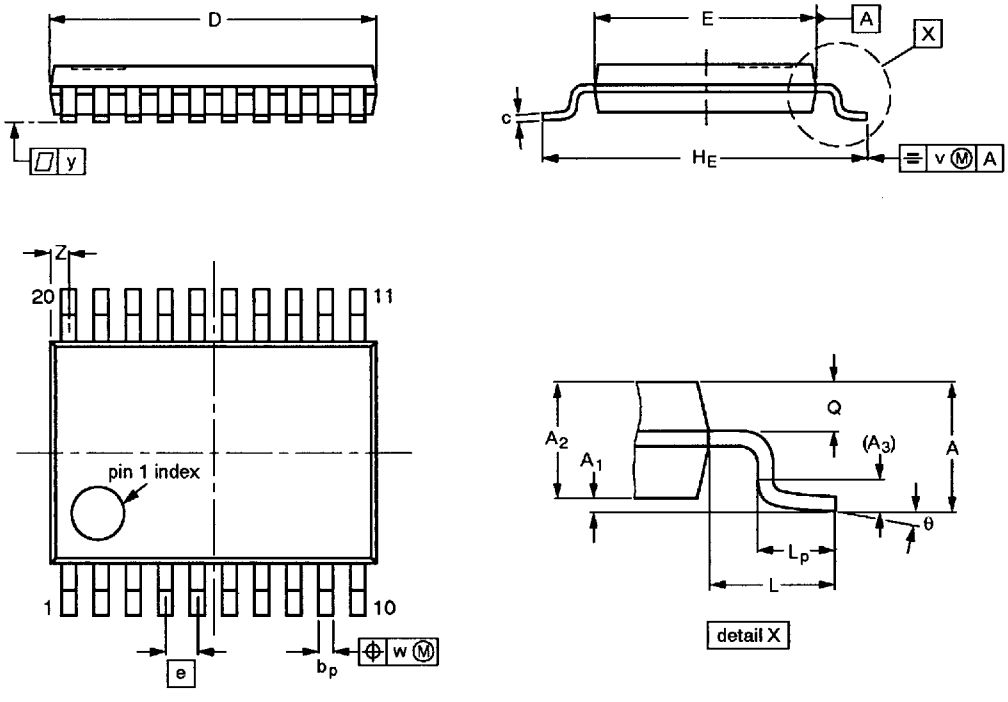
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	7.4 7.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.9 0.5	8° 0°

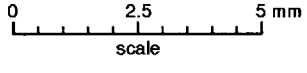
Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT339-1		MO-150AE				~~93-09-08~~ 95-02-04

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm **SOT360-1**





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT360-1		MO-153AC				~~93-06-16~~ 95-02-04