REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
C	Added case outline Z. Corrected the true dimensioning table feature for case outlines U, X, and Y. -sld	98-08-13	K.A. Cottongim
D	Added case outline 9. Added vendor cage 0EU86 for device types 01 through 03 in the Standard Microcircuit Drawing Source Approval Bulletin. -sld	00-04-19	Raymond L. Monnin

REV																				
SHEET																				
REV	D	D	D	D	D	D	D	D	D	D	D	D	D	D						
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28						

REV STATUS	REV	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

PREPARED BY
Gary Zahn

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216

STANDARD MICROCIRCUIT DRAWING

CHECKED BY
Michael C. Jones

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

APPROVED BY
Kendall A. Cottongim

MICROCIRCUIT, HYBRID, MEMORY, DIGITAL, 32K x 32-BIT, ELECTRICALLY ERASABLE AND PROGRAMMABLE READ ONLY MEMORY

DRAWING APPROVAL DATE
94-08-26

AMSC N/A

REVISION LEVEL	SIZE	CAGE CODE	
D	A	**67268**	**5962-94614**

SHEET 1 OF 28

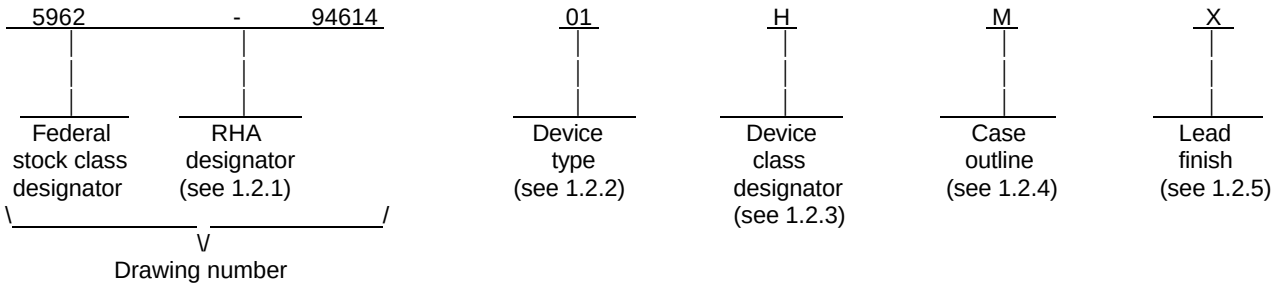
DSCC FORM 2233
APR 97

5962-E175-00

1. SCOPE

1.1 Scope. This drawing documents five product assurance classes, class D (lowest reliability), class E, (exceptions), class G (lowered high reliability), class H (high reliability), and class K, (highest reliability) and a choice of case outlines and lead finishes which are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of radiation hardness assurance levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 Radiation hardness assurance (RHA) designator. RHA marked devices shall meet the MIL-PRF-38534 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	WE32K32-150Q, AS8E32K32Q-150/883C	EEPROM, 32K x 32-bit	150 ns
02	WE32K32-120Q, AS8E32K32Q-120/883C	EEPROM, 32K x 32-bit	120 ns
03	WE32K32-90Q, AS8E32K32Q-90/883C	EEPROM, 32K x 32-bit	90 ns

1.2.3 Device class designator. This device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device performance documentation
D, E, G, H, or K	Certification and qualification to MIL-PRF-38534

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
M	See figure 1	68	Ceramic, dual cavity, quad flatpack
U	See figure 1	66	1.075", hex-in-line, single cavity, with standoffs
X	See figure 1	66	Hex-in-line, single cavity, with standoffs
Y 1/	See figure 1	66	Hex-in-line, single cavity, without standoffs
Z	See figure 1	68	Co-fired ceramic, single cavity, ultra low profile, quad flatpack
9	See figure 1	68	Co-fired ceramic, single cavity, quad flatpack

1.2.5 Lead finish. The lead finish shall be as specified in MIL-PRF-38534.

1/ The case outline Y is inactive for new design.

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.6 V dc to +6.25 V dc
Input voltage range	-0.6 V dc to +6.25 V dc
Power dissipation (P_D)	1.5 W
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance junction-to-case (θ_{JC}):	
Case outlines M and Z	11.3°C/W
Case outlines U, X, and Y	2.8°C/W
Case outline 9	4.57°C/W
Data retention	10 years minimum
Endurance	10,000 cycles minimum

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Input low voltage range (V_{IL})	-0.5 V dc to +0.8 V dc
Input high voltage range (V_{IH})	+2.0 V dc to V_{CC} + 0.3 V dc
Output voltage, High minimum (V_{OH})	+2.4 V dc
Output voltage, low maximum (V_{OL})	+0.45 V dc
Case operating temperature range (T_C)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38534 - Hybrid Microcircuits, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard for Microcircuit Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbook are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

1/ Stresses above the absolute maximum ratings may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item performance requirements for device classes D, E, G, H, and K shall be in accordance with MIL-PRF-38534. Compliance with MIL-PRF-38534 may include the performance of all tests herein or as designated in the device manufacturer's Quality Management (QM) plan or as designated for the applicable device class. Therefore, the tests and inspections herein may not be performed for the applicable device class (see MIL-PRF-38534). Furthermore, the manufacturer may take exceptions or use alternate methods to the tests and inspections herein and not perform them. However, the performance requirements as defined in MIL-PRF-38534 shall be met for the applicable device class.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38534 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 3.

3.2.4 Timing diagram(s). The timing diagram(s) shall be as specified on figure 4, 5, 6, and 7.

3.2.5 Block diagram. The block diagram shall be as specified on figure 8 .

3.2.6 Output test circuit. The output test circuit shall be as specified on figure 9 .

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full specified operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Programming procedure. The programming procedure shall be as specified by the manufacturer and shall be available upon request.

3.6 Marking of Device(s). Marking of device(s) shall be in accordance with MIL-PRF-38534. The device shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's vendor similar PIN may also be marked.

3.7 Data. In addition to the general performance requirements of MIL-PRF-38534, the manufacturer of the device described herein shall maintain the electrical test data (variables format) from the initial quality conformance inspection group A lot sample, for each device type listed herein. Also, the data should include a summary of all parameters manually tested, and for those which, if any, are guaranteed. This data shall be maintained under document revision level control by the manufacturer and be made available to the preparing activity (DSCC-VA) upon request.

3.8 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to supply to this drawing. The certificate of compliance (original copy) submitted to DSCC-VA shall affirm that the manufacturer's product meets the performance requirements of MIL-PRF-38534 and herein.

3.9 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38534 shall be provided with each lot of microcircuits delivered to this drawing.

3.10 Endurance. A reprogrammability test shall be completed as part of the vendor's reliability monitors. This reprogrammability test shall be done for the initial characterization and after any design process changes which may affect the reprogrammability of the device. The methods and procedures may be vendor specific, but shall guarantee the number of program/erase cycles listed in section 1.3 herein over the full military temperature range. The vendor's procedure shall be kept under document control and shall be made available upon request of the acquiring or preparing activity.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $+4.5\ V\ dc \le V_{CC} \le +5.5\ V\ dc$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
DC Parameters							
Supply current	I_{CC}	$\overline{CS} = V_{IL}$, $\overline{OE} = \overline{WE} = V_{IH}$, $I_{OUT} = 0$ mA, $V_{CC} = 5.5$ V dc, A0 through A14 and D0 through D31 change at 5 MHz CMOS levels.	1, 2, 3	01 02 03		150 200 250	mA
Standby current	I_{SB}	$\overline{CS} = \overline{OE} = V_{IH}$, $I_{OUT} = 0$ mA, $V_{CC} = 5.5$ V dc, A0 through A14 and D0 through D31 change at 5 MHz CMOS levels.	1, 2, 3	All		2.5	mA
Input leakage current	I_{LI}	$V_{IN} = V_{SS}$ or V_{CC}	1, 2, 3	All		10	µA
Output leakage current	I_{LO}	$V_{OUT} = V_{SS}$ or V_{CC}, $\overline{CS} = V_{IH}$	1, 2, 3	All		10	µA
Output low voltage	V_{OL}	$I_{OL} = 2.1$ mA, $V_{CC} = +4.5$ V	1, 2, 3	All		0.45	V
Output high voltage	V_{OH}	$I_{OH} = -400$ µA, $V_{CC} = +4.5$ V	1, 2, 3	All	2.4		V
Functional testing							
Functional tests		See 4.3.1c	7, 8A, 8B				
Dynamic characteristics							
A0 - A14 2/ OE capacitance	C_{AD} C_{OE}	$V_{IN} = 0$ V, f = 1.0 MHz, $T_A = +25°C$	4	All		50	pF
$\overline{CS}$1-4 capacitance 2/	C_{CS}	$V_{IN} = 0$ V, f = 1.0 MHz, $T_A = +25°C$	4	All		20	pF
$\overline{WE}$1-4 capacitance 2/	C_{WE}	$V_{IN} = 0$ V, f = 1.0 MHz, $T_A = +25°C$	4	All		20	pF
I/O0-I/O31 capacitance 2/	$C_{I/O}$	$V_{I/O} = 0$ V, f = 1.0 MHz, $T_A = +25°C$	4	All		20	pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $+4.5\ V\ dc \le V_{CC} \le +5.5\ V\ dc$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Read cycle AC timing characteristics							
Read cycle time	t_{RC}	See figure 4	9,10,11	01 02 03	150 120 90		ns
Address access time	t_{ACC}	See figure 4	9, 10, 11	01 02 03		150 120 90	ns
Chip select access time	t_{ACS}	See figure 4	9, 10, 11	01 02 03		150 120 90	ns
Output hold from address change OE or CS	t_{OH}	See figure 4	9, 10, 11	All	0		ns
Output enable to output valid	t_{OE}	See figure 4	9, 10, 11	01 02 03		70 60 50	ns
Chip select or Output enable to Output high Z 2/	t_{DF}	See figure 4	9, 10, 11	01 02 03		70 60 50	ns
Byte write AC timing characteristics							
Address setup time	t_{AS}	See figure 5	9, 10, 11	All	0		ns
Write pulse width	t_{WP}	See figure 5	9, 10, 11	01 ,02	150		ns
				03	100		
Chip select setup time	t_{CS}	See figure 5	9, 10, 11	All	0		ns
Address hold time	t_{AH}	See figure 5	9, 10, 11	01, 02	100		ns
				03	50		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $+4.5\ V\ dc \le V_{CC} \le +5.5\ V\ dc$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Byte write AC timing characteristics - Continued							
Output enable setup time	t_{OES}	See figure 5	9, 10, 11	01, 02	10		ns
				03	4		
Data hold time	t_{DH}	See figure 5	9, 10, 11	01, 02	10		ns
				03	0		
Output enable hold time	t_{OEH}	See figure 5	9, 10, 11	All	10		ns
Data setup time	t_{DS}	See figure 5	9, 10, 11	01, 02	100		ns
				03	50		
Chip select hold time	t_{CSH}	See figure 5	9, 10, 11	All	0		ns
Write pulse width high	t_{WPH}	See figure 5	9, 10, 11	All	50		ns
Write cycle time	t_{WC}	See figure 5	9, 10, 11	All		10	ms
Page mode write AC timing characteristics							
Data setup time	t_{DS}	See figure 6	9, 10, 11	01, 02	100		ns
				03	50		
Data hold time	t_{DH}	See figure 6	9, 10, 11	01, 02	10		ns
				03	0		
Write pulse width	t_{WP}	See figure 6	9, 10, 11	01, 02	150		ns
				03	100		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $+4.5\ V\ dc \le V_{CC} \le +5.5\ V\ dc$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Page mode write AC timing characteristics - continued							
Byte load cycle time	t_{BLC}	See figure 6	9, 10, 11	All		150	µs
Write pulse width high	t_{WPH}	See figure 6	9, 10, 11	All	50		ns
Write cycle time	t_{WC}	See figure 6	9, 10, 11	All		10	ms
Data polling AC timing characteristics							
Data hold time	t_{DH}	See figure 7	9, 10, 11	All	10		ns
Output enable hold time	t_{OEH}	See figure 7	9, 10, 11	All	10		ns
Output enable to output delay	t_{OE}	See figure 7	9, 10, 11	All		100	ns
Write recovery time	t_{WR}	See figure 7	9, 10, 11	All	0		ns

1/ Unless otherwise specified:
The DC test conditions are as follows:
Input low voltage, V_{IL} = 0.3 V.
Input high voltage, $V_{IH} = V_{CC}$ - 0.3 V.

The AC test conditions are as follows:
Input pulse levels: V_{IL} = 0 V and V_{IH} = 3.0 V.
Input rise and fall times: 5 nanoseconds.
Input and output timing reference levels: 1.5 V.

2/ Guaranteed by design, but not tested.

Case outline M.

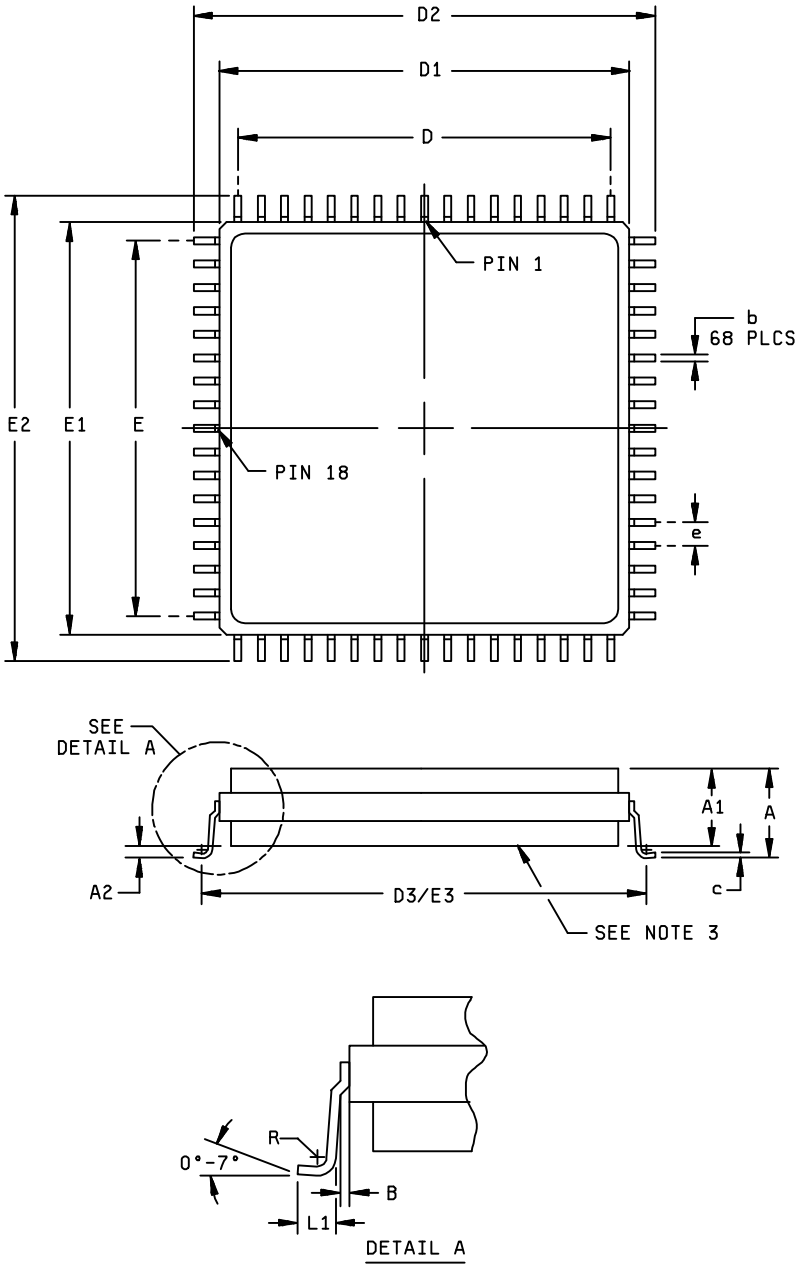


FIGURE 1. Case outline(s).

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE **A**		**5962-94614**
		REVISION LEVEL **D**	SHEET **9**

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	4.01	5.10	.158	.200
A1	3.91	4.72	.154	.186
A2	0.13	0.38	.005	.015
b	0.33	0.43	.013	.017
c	0.23	0.30	.009	.012
B	0.25 REF		.010 REF	
D/E	20.3 BSC		.800 BSC	
D1/E1	22.10	22.61	.870	.890
D2/E2	24.89	25.40	.980	1.000
D3/E3	23.77	24.28	.936	.956
e	1.27 BSC		.050 BSC	
R	0.13		.005	
L1	0.89	1.14	.035	.045

NOTES:
1. The U.S. preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. Pin numbers are for reference only.
3. Case outline M is a dual cavity package.

FIGURE 1. Case outline(s) - Continued.

Case outlines U and X.

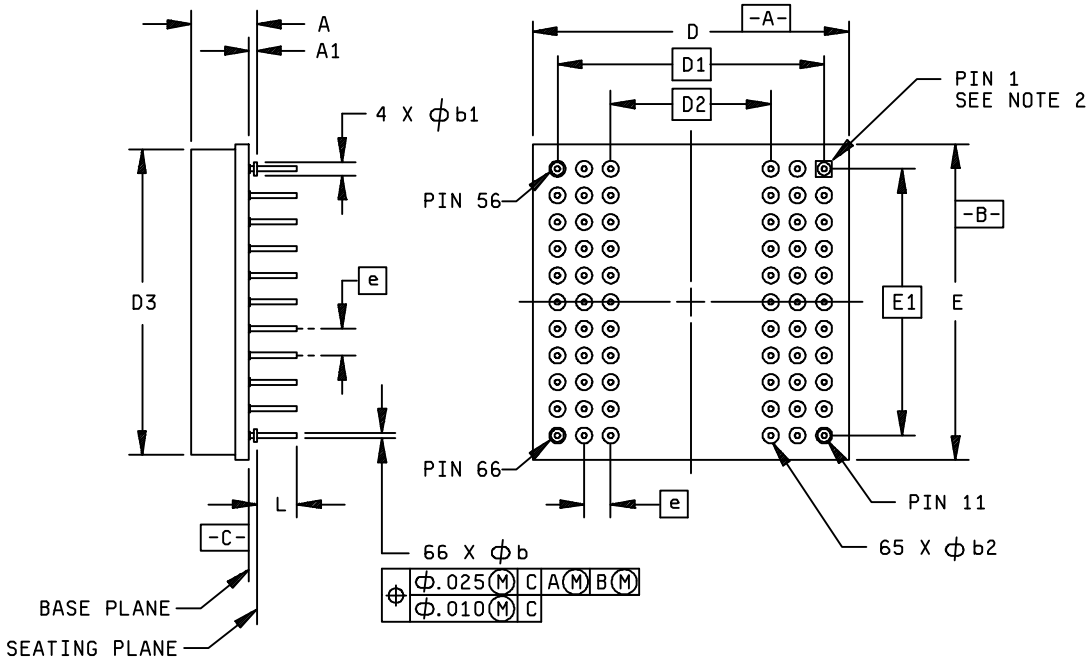


FIGURE 1. Case outline(s) - Continued.

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	3.43	4.34	.135	.171
A1	0.64	0.89	.025	.035
ϕb	0.41	0.51	.016	.020
ϕb1	1.14	1.40	.045	.055
ϕb2	1.65	1.91	.065	.075
D/E	27.05	27.56	1.065	1.085
D1/E1	25.40 BSC		1.000 BSC	
D2	15.24 BSC		.600 BSC	
D3	25.90	26.92	1.020	1.060
e	2.54 BSC		.100 BSC	
L	3.35	3.94	.132	.155

NOTES:
1. The U.S. preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. Pin 1 is identified by a 0.070 square pad.
3. Pin numbers are for reference only.

FIGURE 1. Case outlines - Continued.

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	5.08	6.22	.200	.245
A1	0.64	0.89	.025	.035
ϕb	0.41	0.51	.016	.020
ϕb1	1.14	1.40	.045	.055
ϕb2	1.65	1.91	.065	.075
D/E	29.72	30.48	1.170	1.200
D1/E1	25.40 BSC		1.000 BSC	
D2	15.24 BSC		.600 BSC	
D3	28.96	29.21	1.140	1.150
e	2.54 BSC		.100 BSC	
L	3.68	3.94	.145	.155

NOTES:
1. The U.S. preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. Pin 1 is identified by a 0.070 square pad.
3. Pin numbers are for reference only.

FIGURE 1. Case outlines - Continued.

Case outline Y.

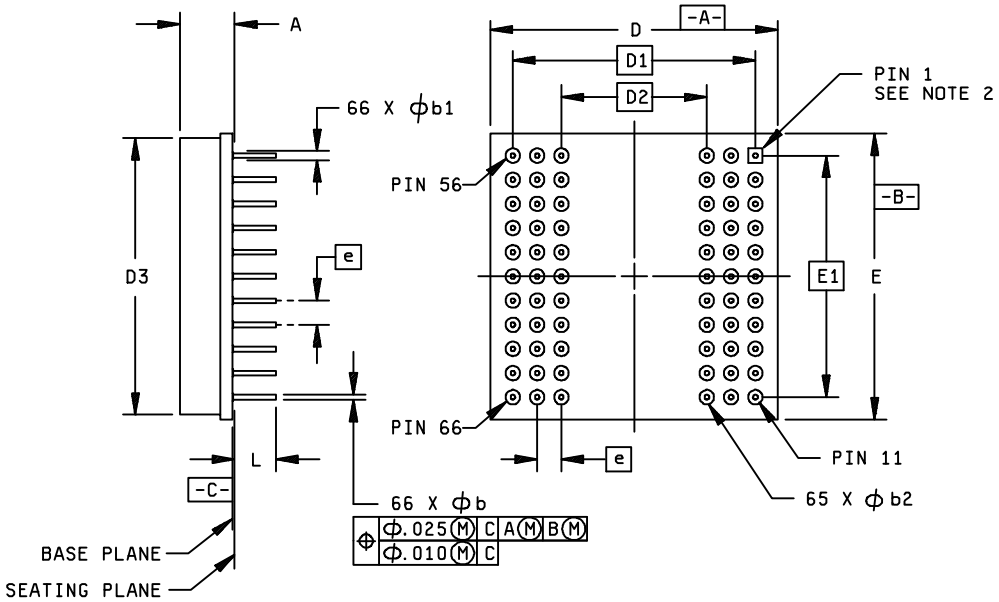


FIGURE 1. Case outline(s) - Continued.

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	4.69	5.84	.185	.230
ϕb	0.41	0.51	.016	.020
ϕb1	0.76 REF		.030 REF	
ϕb2	1.65	1.91	.065	.075
D/E	29.72	30.48	1.170	1.200
D1/E1	25.40 BSC		1.000 BSC	
D2	15.24 BSC		.600 BSC	
D3	28.96	29.21	1.140	1.150
e	2.54 BSC		.100 BSC	
L	4.19	4.69	.165	.185

NOTES:
1. The U.S. preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. Pin 1 is identified by a 0.070 square pad.
3. Pin numbers are for reference only.

FIGURE 1. Case outline(s) - Continued.

Case outline Z.

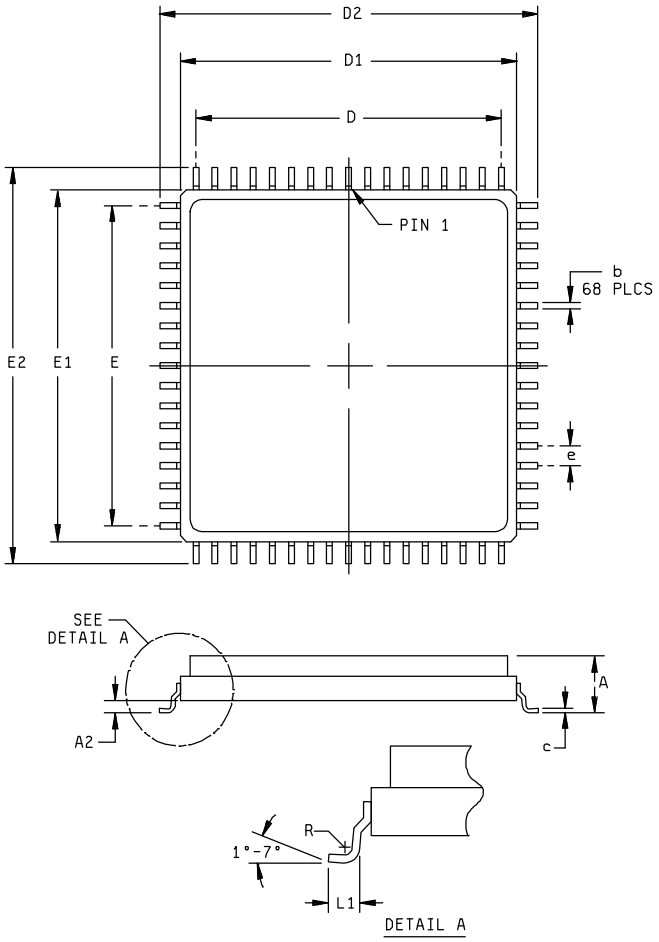


FIGURE 1. Case outline(s) - Continued.

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A		3.56		.140
A2	0.36	0.71	.014	.028
b	0.33	0.43	.013	.017
c	0.23	0.30	.009	.012
D/E	20.32 BSC		.800 BSC	
D1/E1	22.10	22.61	.870	.890
D2/E2	24.89	25.35	.980	1.000
e	1.27 TYP		.050 TYP	
R	0.13 MIN		.005 MIN	
L1	0.89	1.14	.035	.045

NOTES:
1. The U.S. preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. Pin numbers are for reference only.

FIGURE 1. Case outline(s) - Continued.

Case outline 9.

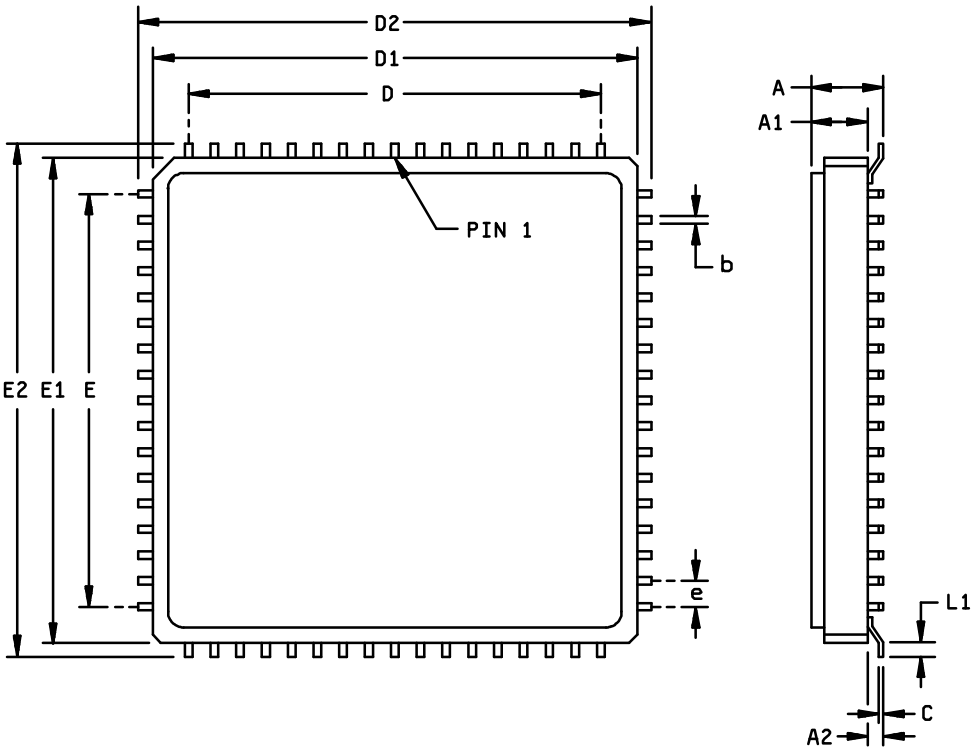


FIGURE 1. Case outline(s) - Continued.

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A		3.56		.140
A1		2.79		.110
A2	0.46	0.76	.018	.030
b	0.33	0.43	.013	.017
C	0.15	0.25	.006	.010
D/E	20.32 TYP		.800 TYP	
D1/E1	23.65	24.10	.931	.949
D2/E2	25.15	25.40	.990	1.000
e	1.27 TYP		.050 TYP	
L1	0.51	1.14	.020	.045

NOTES:
1. The U.S. preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. Pin numbers are for reference only.

FIGURE 1. Case outlines - Continued.

Device types	All	Device types	All	Device types	All	Device types	All
Case outlines	M, Z, 9	Case outlines	M, Z, 9	Case outlines	M, Z, 9	Case outlines	M, Z, 9
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	GND	18	GND	35	$\overline{OE}$	52	GND
2	$\overline{CS3}$	19	I/O8	36	$\overline{CS2}$	53	I/O23
3	A5	20	I/O9	37	NC	54	I/O22
4	A4	21	I/O10	38	$\overline{WE2}$	55	I/O21
5	A3	22	I/O11	39	$\overline{WE3}$	56	I/O20
6	A2	23	I/O12	40	$\overline{WE4}$	57	I/O19
7	A1	24	I/O13	41	NC	58	I/O18
8	A0	25	I/O14	42	NC	59	I/O17
9	NC	26	I/O15	43	NC	60	I/O16
10	I/O0	27	V_{CC}	44	I/O31	61	V_{CC}
11	I/O1	28	A11	45	I/O30	62	A10
12	I/O2	29	A12	46	I/O29	63	A9
13	I/O3	30	A13	47	I/O28	64	A8
14	I/O4	31	A14	48	I/O27	65	A7
15	I/O5	32	NC	49	I/O26	66	A6
16	I/O6	33	NC	50	I/O25	67	$\overline{WE1}$
17	I/O7	34	$\overline{CS1}$	51	I/O24	68	$\overline{CS4}$

NOTE:
1. NC is a no connect.

FIGURE 2. Terminal connections.

Device type	All	Device type	All	Device type	All	Device type	All
Case outlines	U,X,Y	Case outlines	U,X,Y	Case outlines	U,X,Y	Case outlines	U,X,Y
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	I/O8	18	A12	35	I/O25	52	$\overline{WE3}$
2	I/O9	19	V_{CC}	36	I/O26	53	$\overline{CS3}$
3	I/O10	20	$\overline{CS1}$	37	A6	54	GND
4	A13	21	NC	38	A7	55	I/O19
5	A14	22	I/03	39	NC	56	I/O31
6	NC	23	I/015	40	A8	57	I/O30
7	NC	24	I/O14	41	A9	58	I/O29
8	NC	25	I/O13	42	I/O16	59	I/O28
9	I/O0	26	I/O12	43	I/O17	60	A0
10	I/O1	27	$\overline{OE}$	44	I/O18	61	A1
11	I/O2	28	NC	45	V_{CC}	62	A2
12	$\overline{WE2}$	29	$\overline{WE1}$	46	$\overline{CS4}$	63	I/O23
13	$\overline{CS2}$	30	I/O7	47	$\overline{WE4}$	64	I/O22
14	GND	31	I/O6	48	I/O27	65	I/O21
15	I/O11	32	I/O5	49	A3	66	I/O20
16	A10	33	I/O4	50	A4		
17	A11	34	I/O24	51	A5		

NOTE:
1. NC is a no connect.

FIGURE 2. Terminal connections - Continued.

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	A0-A14	MODE	Data I/O	Device current
H	X	X	X	Standby	High Z	Standby
L	L	H	Stable	Read	Data out	Active
L	H	L	Stable	Write	Data in	Active
X	H	X	X	Out Disable	High Z	Active
X	X	H	X	Write Inhibit		Active
X	L	X	X	Write Inhibit		Active

NOTES:

1. H = V_{IH} = High Logic Level
2. L = V_{IL} = Low Logic Level
3. X = Do not care (either high or low)
4. High Z = High Impedance State

FIGURE 3. Truth table.

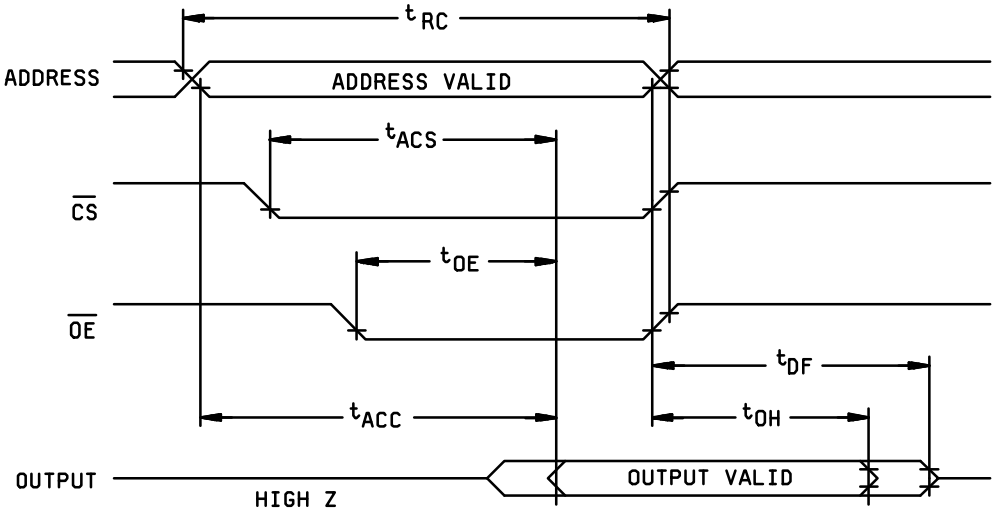


FIGURE 4. Read cycle timing diagram.

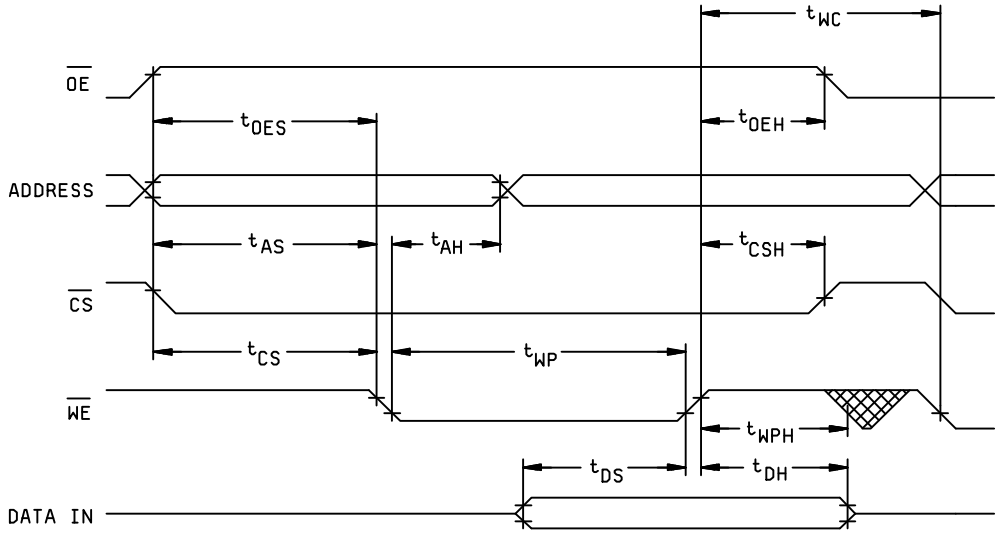


FIGURE 5. Write cycle timing diagram $\overline{WE}$ controlled.

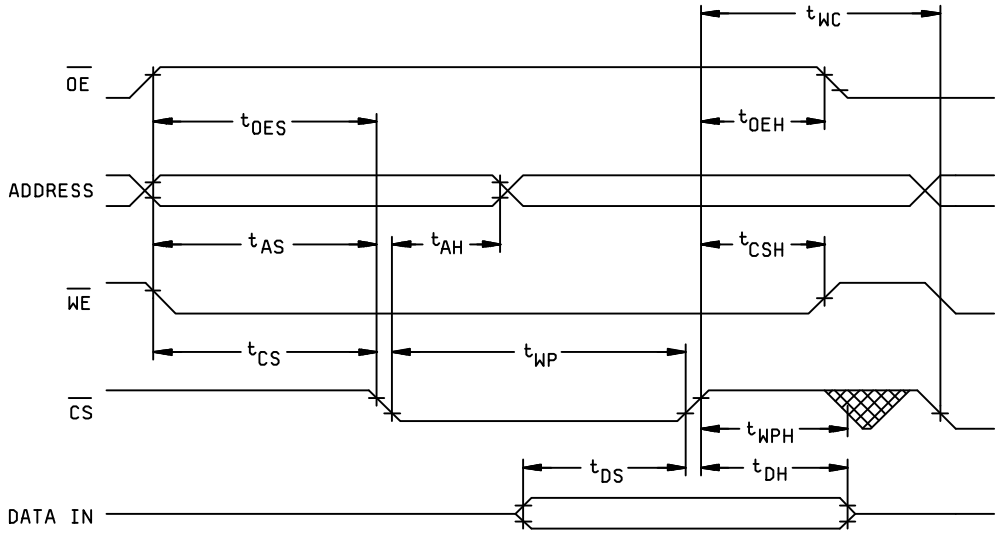
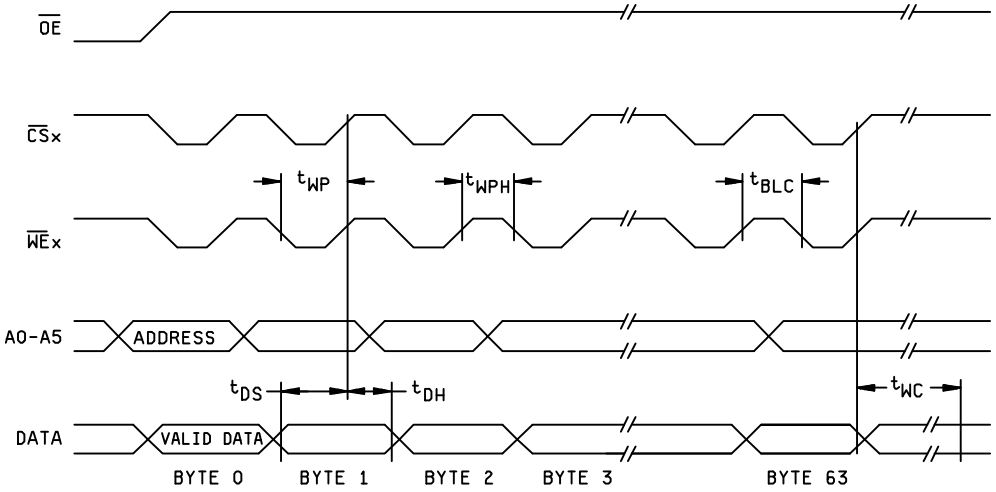


FIGURE 5. Write cycle timing diagram $\overline{CS}$ controlled - Continued.



NOTES:
1. A0 through A5 are used to address specific bytes within a page.
2. A6 through A14 must specify the same page address during each high to low transition of write enable or chip select.

FIGURE 6. Page mode write timing diagram.

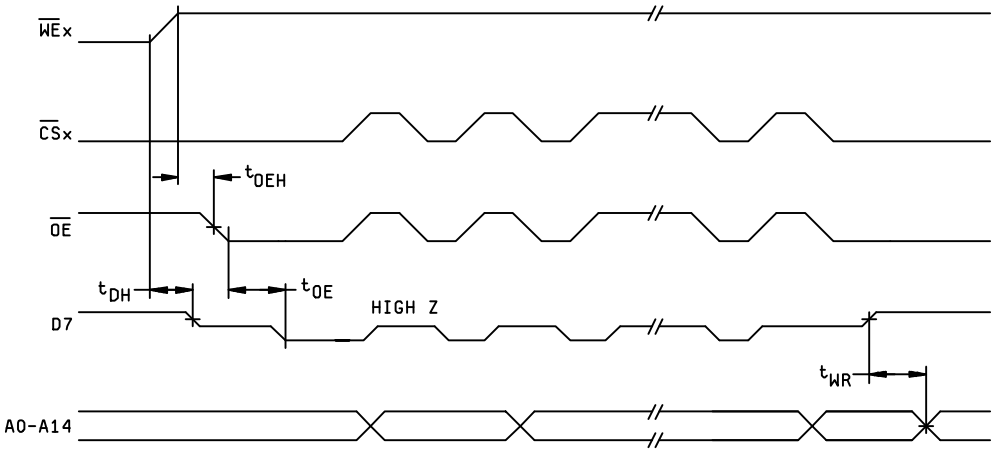


FIGURE 7. Data polling AC timing diagram.

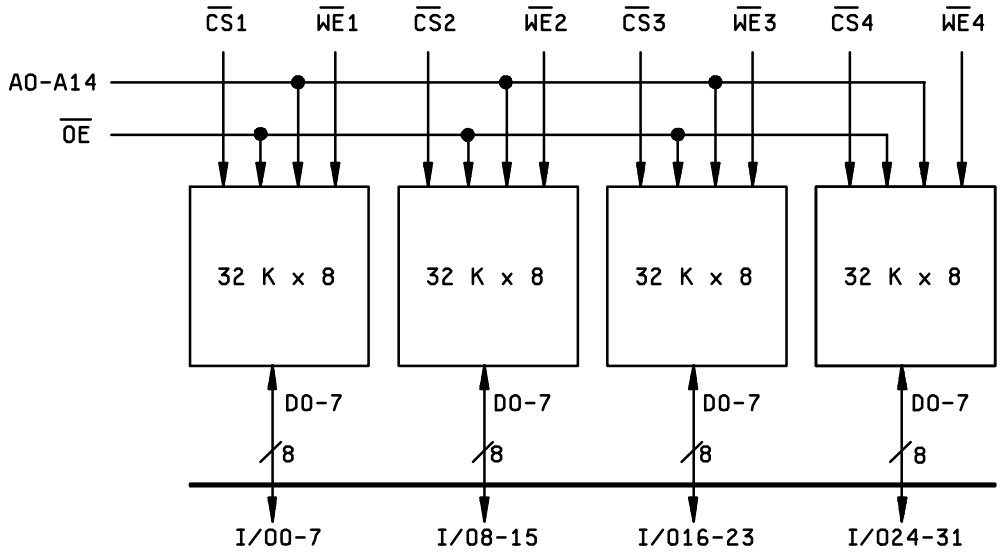
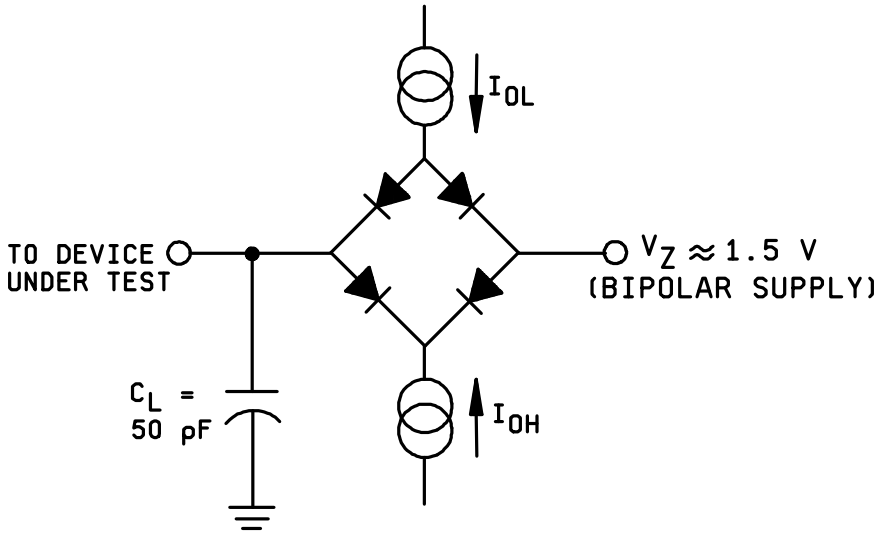


FIGURE 8. Block diagram.



NOTES:

1. V_Z is programmed from -2.0 V to +7.0 V. I_{OH} and I_{OL} are programmable from 0 to 16 mA.
2. Tester impedance Z_O = 75 Ohms.
3. V_Z is typically the midpoint of V_{OH} and V_{OL}.
4. C_L includes tester jig capacitance.

FIGURE 9. Typical output test circuit.

TABLE II. Electrical test requirements.

MIL-PRF-38534 test requirements	Subgroups (in accordance with MIL-PRF-38534, group A test table)
Interim electrical parameters	1, 4, 7, 9
Final electrical parameters	1*, 2, 3, 4, 7, 8A, 8B, 9, 10, 11
Group A test requirements	1, 2, 3, 4, 7, 8A, 8B, 9, 10, 11
Group C end-point electrical parameters	1, 2, 3, 4, 7, 8A, 8B, 9, 10, 11
End-point electrical parameters for Radiation Hardness Assurance (RHA) devices	Not applicable

* PDA applies to subgroup 1.

3.11 Data retention. A data retention stress test shall be completed as part of the vendor's reliability monitors. This test shall be done for initial characterization and after any design process change which may affect data retention. The methods and procedures may be vendor specific, but shall guarantee the number of years listed in section 1.3 herein over the full military temperature range. The vendor's procedure shall be kept under document control and shall be made available upon request of the acquiring or preparing activity.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38534 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. Screening shall be in accordance with MIL-PRF-38534. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition B. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A as specified in accordance with table I of method 1015 of MIL-STD-883.

(3) Prior to burn-in all devices shall be programmed with a 00 hex data pattern to the entire memory array. The resulting pattern shall be verified before and after burn-in. Devices having bits not in the proper state after burn-in shall constitute a device failure and shall not be delivered.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Conformance and periodic inspections. Conformance inspection (CI) and periodic inspection (PI) shall be in accordance with MIL-PRF-38534 and as specified herein.

4.3.1 Group A inspection (CI). Group A inspection shall be in accordance with MIL-PRF-38534 and as follows:

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 shall be omitted.

c. Subgroups 7, 8A, and 8B shall include verification of the truth table in table 3.

d. The following data patterns shall be verified during subgroups 7, 8A, and 8B.

(1) 0's to all memory cell locations.

(2) 1's to all memory cell locations.

(3) Checkerboard pattern to entire memory array.

(4) Checkerboard compliment to entire memory array.

4.3.2 Group B inspection (PI). Group B inspection shall be in accordance with MIL-PRF-38534.

4.3.3 Group C inspection (PI). Group C inspection shall be in accordance with MIL-PRF-38534 and as follows:

a. End-point electrical parameters shall be as specified in table II herein.

b. All devices requiring end-point electrical testing shall be programmed with a checkerboard pattern of alternate rows of AA hex and 55 hex.

c. Steady-state life test, method 1005 of MIL-STD-883.

(1) Test condition B. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A as specified in accordance with table I of method 1005 of MIL-STD-883.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

(4) The checkerboard data pattern shall be verified after burn-in as part of end-point electrical testing.

4.3.4 Group D inspection (PI). Group D inspection shall be in accordance with MIL-PRF-38534.

4.3.5 Radiation Hardness Assurance (RHA) inspection. RHA inspection is not currently applicable to this drawing.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38534.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated as specified in MIL-PRF-38534..

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0512.

6.6 Sources of supply. Sources of supply are listed in MIL-HDBK-103 and QML-38534. The vendors listed in MIL-HDBK-103 and QML-38534 have submitted a certificate of compliance (see 3.8 herein) to DSCC-VA and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 00-04-19

Approved sources of supply for SMD 5962-94614 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38534 during the next revisions. MIL-HDBK-103 and QML-38534 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revisions of MIL-HDBK-103 and QML-38534.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9461401HUA	0EU86	AS8E32K32P-150/883C
5962-9461401HUA	54230	WE32K32-150H1Q
5962-9461401HUC	0EU86	AS8E32K32P-150/883C
5962-9461401HUC	54230	WE32K32-150H1Q
5962-9461401HMA	54230	WE32K32-150G2Q
5962-9461401HMC	54230	WE32K32-150G2Q
5962-9461401HXA	54230	WE32K32N-150HQ
5962-9461401HXC	54230	WE32K32N-150HQ
5962-9461401HYA	3/	WE32K32N-150HSQ
5962-9461401HYC	3/	WE32K32N-150HSQ
5962-9461401HZA	0EU86	AS8E32K32Q-150/883C
5962-9461401HZA	54230	WE32K32-150G2UQ
5962-9461401HZC	0EU86	AS8E32K32Q-150/883C
5962-9461401HZC	54230	WE32K32-150G2UQ
5962-9461401H9A	54230	WE32K32-150G1UQ
5962-9461401H9C	54230	WE32K32-150G1UQ
5962-9461402HUA	0EU86	AS8E32K32P-120/883C
5962-9461402HUA	54230	WE32K32-120H1Q
5962-9461402HUC	0EU86	AS8E32K32P-120/883C
5962-9461402HUC	54230	WE32K32-120H1Q
5962-9461402HMA	54230	WE32K32-120G2Q
5962-9461402HMC	54230	WE32K32-120G2Q
5962-9461402HXA	54230	WE32K32N-120HQ
5962-9461402HXC	54230	WE32K32N-120HQ
5962-9461402HYA	3/	WE32K32N-120HSQ
5962-9461402HYC	3/	WE32K32N-120HSQ
5962-9461402HZA	0EU86	AS8E32K32Q-120/883C
5962-9461402HZA	54230	WE32K32-120G2UQ
5962-9461402HZC	0EU86	AS8E32K32Q-120/883C
5962-9461402HZC	54230	WE32K32-120G2UQ
5962-9461402H9A	54230	WE32K32-120G1UQ
5962-9461402H9C	54230	WE32K32-120G1UQ

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9461403HUA	0EU86	AS8E32K32P-90/883C
5962-9461403HUA	54230	WE32K32-90H1Q
5962-9461403HUC	0EU86	AS8E32K32P-90/883C
5962-9461403HUC	54230	WE32K32-90H1Q
5962-9461403HMA	54230	WE32K32-90G2Q
5962-9461403HMC	54230	WE32K32-90G2Q
5962-9461403HXA	54230	WE32K32N-90HQ
5962-9461403HXC	54230	WE32K32N-90HQ
5962-9461403HYA	3/	WE32K32N-90HSQ
5962-9461403HYC	3/	WE32K32N-90HSQ
5962-9461403HZA	0EU86	AS8E32K32Q-90/883C
5962-9461403HZA	54230	WE32K32-90G2UQ
5962-9461403HZC	0EU86	AS8E32K32Q-90/883C
5962-9461403HZC	54230	WE32K32-90G2UQ
5962-9461403H9A	54230	WE32K32-90G1UQ
5962-9461403H9C	54230	WE32K32-90G1UQ

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ No longer available from a QML source.

Vendor CAGE number	Vendor name and address
0EU86	Austin Semiconductor Incorporated 8701 Cross Park Drive Austin, TX 78584-4566
54230	White Electronic Designs Corporation 3601 East University Drive Phoenix, AZ 85034-7217