REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																									
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REV STATUS OF SHEETS	REV																								
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13											

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
11 AUGUST 1988

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, LINEAR, 6-BIT VIDEO A/D CONVERTER, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-87786

SHEET 1 OF 13

DESC FORM 193
SEP 87

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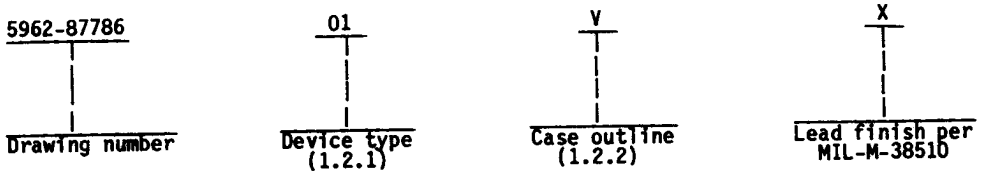
5962-E681

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:



1.2.1 Device type. The device type shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	TDC1046	6-bit flash A/D converter

1.2.2 Case outline. The case outline shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
V	D-6 (18-lead, .960" x .310" x .200"), dual-in-line package

1.3 Absolute maximum ratings.

V_{CC} to D_{GND}	-0.5 V dc to +7.0 V dc
V_{EE} to A_{GND}	+0.5 V dc to -7.0 V dc
A_{GND} to D_{GND}	-0.5 V dc to +0.5 V dc
CONV, NMINV, or NLINV to D_{GND}	-0.5 V dc to +5.5 V dc
V_{IN}, V_{RT}, or V_{RB} to A_{GND}	+0.5 V dc to V_{EE}
V_{RT} to V_{RB}	+1.2 V dc to -1.2 V dc
Applied output voltage to D_{GND}	-0.5 V dc to +5.5 V dc 1/
Applied output current, externally forced	-1.0 mA to +6.0 mA 2/ 3/
Output short-circuit duration	1.0 s 4/
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Power dissipation (P_D)	1.0 W
Thermal resistance, junction-to-case (θ_{JC})	See MIL-M-38510, appendix C
Thermal resistance, junction-to-ambient (θ_{JA})	66°C/W

1/ Applied voltage must be current limited to specified range.
2/ Forcing voltage must be limited to specified range.
3/ Current is specified as positive when flowing into the device.
4/ Single output in high state to ground.

1.4 Recommended operating conditions.

Positive supply voltage (V_{CC})	4.5 V dc to 5.5 V dc
Negative supply voltage (V_{EE})	-4.9 V dc to -5.5 V dc
Analog ground voltage to D_{GND} (V_{AGND})	-0.1 V dc to +0.1 V dc
CONV pulse width, low (t_{PWL})	15 ns minimum
CONV pulse width, high (t_{PWH})	17 ns minimum
Input voltage, logic low (V_{IL})	0.8 V dc maximum
Input voltage, logic high (V_{IH})	2.0 V dc minimum
Output current, logic low (I_{OL})	2.0 mA maximum
Output current, logic high (I_{OH})	-0.4 mA maximum
Most positive reference input (V_{RT}) 5/	-0.1 V dc to 0.1 V dc
Most negative reference input (V_{RB}) 5/	-0.9 V dc to -1.1 V dc
Voltage reference differential (V_{RT}-V_{RB})	0.8 V dc to 1.2 V dc
Input voltage (V_{IN})	V_{RB} to V_{RT}
Case operating temperature range (T_C)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in the issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883 "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, contruction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Block diagram. The block diagram shall be as specified on figure 2.

5/ V_{RT} must be more positive than V_{RB}, and V_{RT}-V_{RB} must be within the specified range.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified		Group A subgroups	Limits		Unit
					Min	Max	
Positive supply current, static	I_{CC}	V_{EE} = -4.9 V, V_{CC} = 5.5 V		1, 2, 3		25	mA
Negative supply current, static	I_{EE}	V_{EE} = -5.5 V		1, 2, 3		-150	mA
Reference current	I_{REF}	V_{RT} = 0 V, V_{RB} = -1.0 V, V_{EE} = -4.9 V		1, 2, 3		15	mA
Input constant bias current	I_{CB}	V_{EE} = -5.5 V, V_{CC} = 5.5		1, 2, 3		180	µA
Input low current	I_{IL}	V_I = 0.4 V, V_{EE} = -4.9 V, V_{CC} = 5.5 V	CONV	1, 2, 3		-0.6	mA
			NMINV, NLINV			-0.8	
Input high current	I_{IH}	V_I = 2.4 V, V_{CC} = 5.5 V, V_{EE} = -4.9 V		1, 2, 3		50	µA
Input current at maximum input voltage	I_I	V_I = 5.5 V, V_{CC} = 5.5 V, V_{EE} = -4.9 V		1, 2, 3		1.0	mA
Output low voltage	V_{OL}	I_{OL} = 2 mA, V_{CC} = 4.5 V, V_{EE} = -5.5 V		1, 2, 3		0.5	V
Output high voltage	V_{OH}	I_{OH} = -400 µA, V_{CC} = 4.5 V		1, 2, 3	2.4		V
Output short circuit current 2/	I_{OS}	V_{EE} = -4.9 V, V_{CC} = 5.5 V		1, 2, 3		-30	mA
Digital output delay	t_D	V_{EE} = -4.9 V, V_{CC} = 5.5 V See figures 4 and 5		9, 10, 11		35	ns
Linearity error integral, independent	E_{LI}	V_{RT} = 0 V, V_{RB} = -1.0 V FS = 100 kHz		4, 5, 6		0.4	%
Linearity error, differential	E_{LD}	V_{RT} = 0 V, V_{RB} = -1.0 V FS = 100 kHz		4, 5, 6		0.4	%
Functional tests		V_{EE} = -4.9 V, V_{CC} = 4.5 V, f = 1.0 MHz, see 4.3.1b		7, 8			

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test 3/	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified		Group A subgroups	Limits Min	Limits Max	Unit
Offset error, top	E_{OT}	V_{IN} = midpoint of code 0		1, 2, 3		+50	mV
Offset error, bottom	E_{OB}	V_{IN} = midpoint of code 63		1, 2, 3		-30	mV
Total reference resistance	R_{REF}	V_{RT} = 0 V, V_{RB} = -1.0 V		1, 2, 3	66		Ω
Input equivalent resistance	R_{IN}	V_{RT} = 0 V, V_{RB} = -1.0 V		1, 2, 3	40		kΩ
Input capacitance	C_{IN}	V_{RT} = 0 V, V_{RB} = -1.0 V		4, 5, 6		30	pF
Digital input capacitance	C_I	T_C = +25°C, F = 1 MHz		4		15	pF
Maximum conversion rate	FS			4, 5, 6	25		MSPS
Sampling time offset	t_{STO}	See figures 4 and 5		9, 10, 11		15	ns
Output hold time	t_{HO}	See figures 4 and 5		9, 10, 11	5		ns
Code size	Q				50	150	% of nominal
Temperature coefficient offset voltage	T_{CO}			1, 2, 3		±20	µV/°C
Bandwidth, full power input	BW			4, 5, 6	12.5		MHz
Signal-to-noise ratio (25 MSPS conversion rate, 12.5 MHz bandwidth)	SNR	Peak signal/ RMS noise	1 MHz input	4, 5, 6	42		dB
			12.5 MHz input		38		
		RMS signal/ RMS noise	1 MHz input		33		
			12.5 MHz input		29		

1/ Unless otherwise specified, characteristics apply over the recommended operating conditions specified in 1.4 herein.
2/ Output high, one pin to ground, one second duration maximum.
3/ These tests are guaranteed if not tested.

3.2.3 Truth table. The truth table shall be as specified in figure 3.

3.2.4 Timing diagram. The timing diagram shall be as specified in figure 4.

3.2.5 Load circuit. The load circuit shall be as specified in figure 5.

3.2.6 Case outline. The case outline shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein.

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

Terminal number	Terminal symbol
1	V_{IN}
2	R_T
3	D_{GND}
4	NMINV
5	MSB D_1
6	D_2
7	D_3
8	V_{CC}
9	V_{EE}
10	V_{CC}
11	NLINV
12	D_4
13	D_5
14	D_6 (LSB)
15	CONV
16	D_{GND}
17	A_{GND}
18	R_B

FIGURE 1. Terminal connections.

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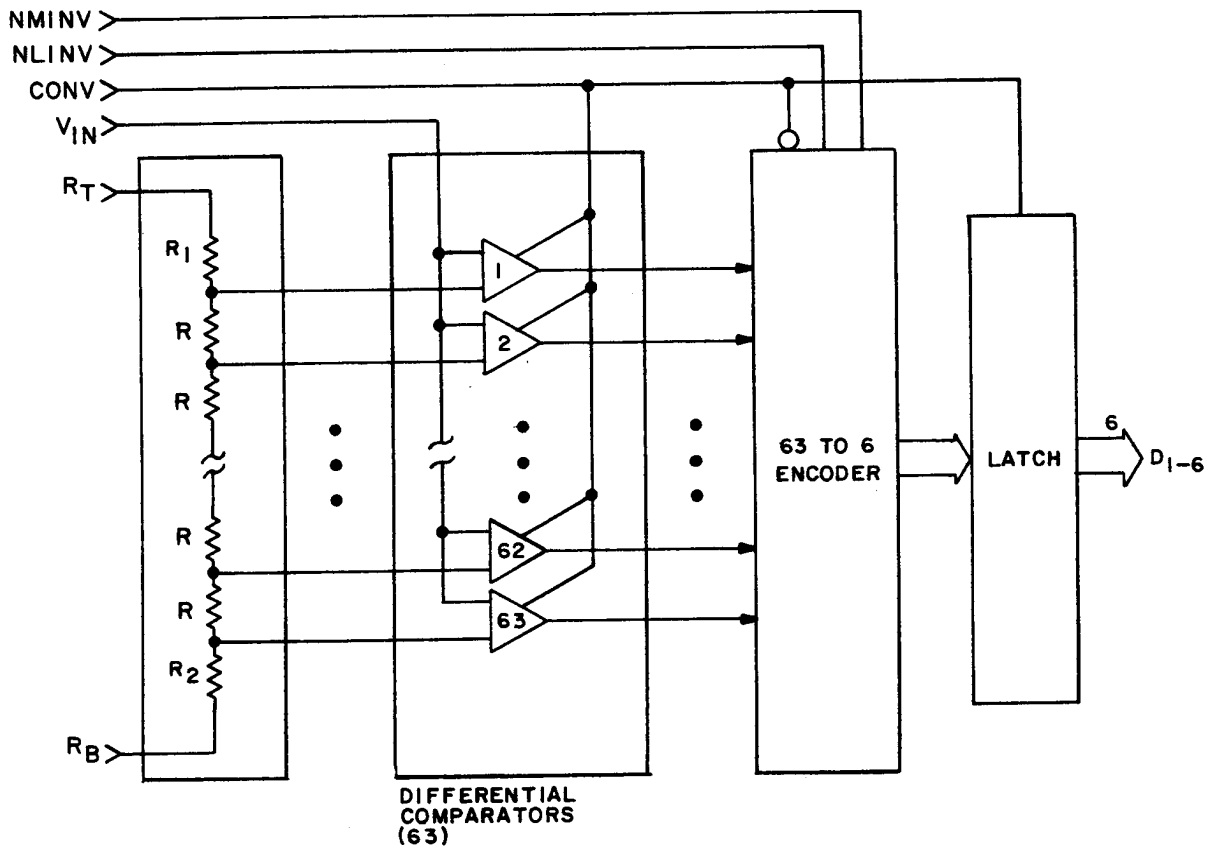

FIGURE 2. Block diagram.

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Step	Range	Binary		Offset two's complement	
		True	Inverted	True	Inverted
	-1.0000 V F_S 15.8730 mV step	NMINV = 1 NLINV = 1	0 0	0 1	1 0
00	0.0000 V	000000	111111	100000	011111
01	-0.0159 V	000001	111110	100001	011110
"	"	"	"	"	"
"	"	"	"	"	"
31	-0.4921 V	011111	100000	111111	000000
32	-0.5079 V	100000	011111	000000	111111
33	-0.5238 V	100001	011110	000001	111110
"	"	"	"	"	"
"	"	"	"	"	"
"	"	"	"	"	"
62	-0.9841 V	111110	000001	011110	100001
63	-1.0000 V	111111	000000	011111	100000

NOTES:
1. NMINV and NLINV are to be considered dc controls. They may be tied to +5.0 V for a logical "1" and tied to ground for a logical "0".
2. Voltages are code midpoints when calibrated by adjusting V_{RT} and V_{RB} to set the 1st and 63rd thresholds to the desired voltages. Note that R_1 is greater than R (refer to block diagram on figure 2 herein), ensuring calibration with a positive voltage on R_T. Assuming a 0 V to -1.0 V desired range, continuously strobe the converter with -0.0079 V (1/2 LSB from 0 V) on the analog input, and adjust V_{RT} for output toggling between 00 and 01. Then apply -0.9921 V (1/2 LSB from -1.0 V) and adjust V_{RB} for toggling between codes 62 and 63.
The degree of required adjustment is indicated by the offset error, E_{OT} and E_{OB}. Offset errors are generated by the inherent parasitic resistance between the package pin and the actual resistor chain on the integrated circuit. These parasitic resistors are shown as R_1 and R_2 in the block diagram shown on figure 2. Calibration will cancel all offset voltages, eliminating offset and gain errors.
This method of calibration requires that both ends of the resistor chain, R_T and R_B are driven by buffered operational amplifiers. Instead of adjusting V_{RT}, R_T can be connected to analog ground and the 0 V end of the range calibrated with a buffer offset control. The offset error at the bottom of the resistor chain results in a slight gain error, which can be compensated for by varying the voltage applied to R_B. The bottom reference is a convenient point for gain adjust that is not in the analog signal path.

FIGURE 3. Truth table.

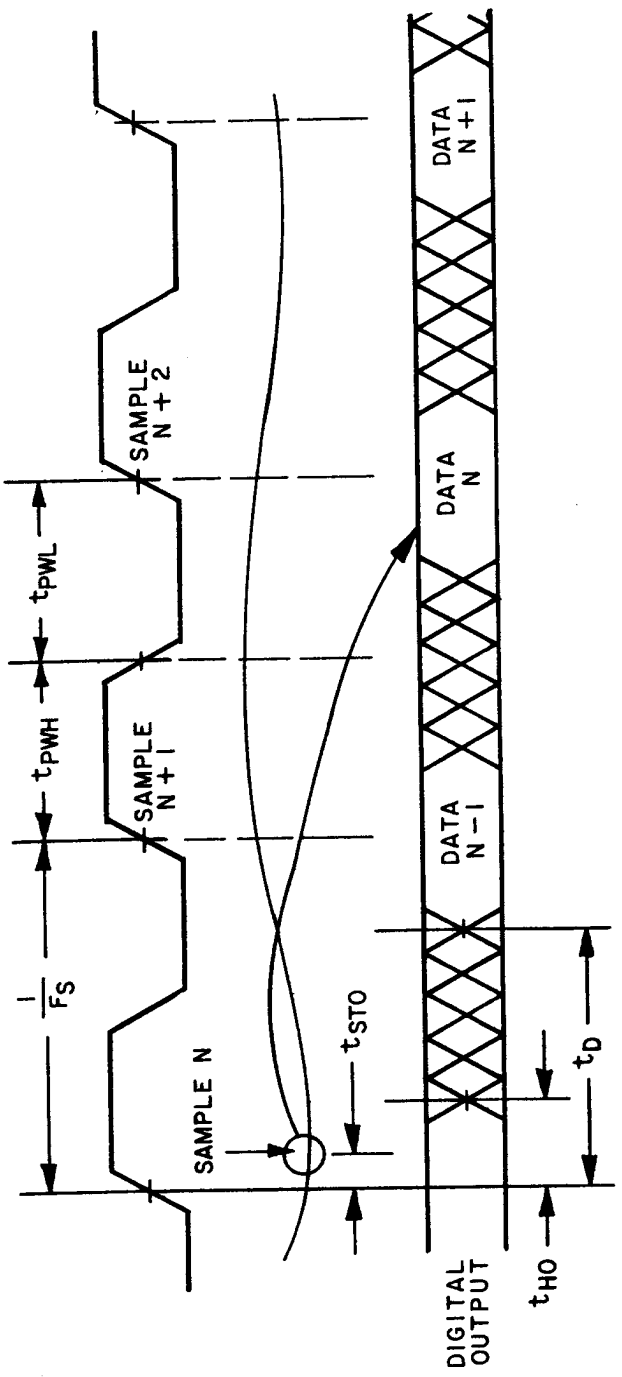

FIGURE 4. Timing diagram.

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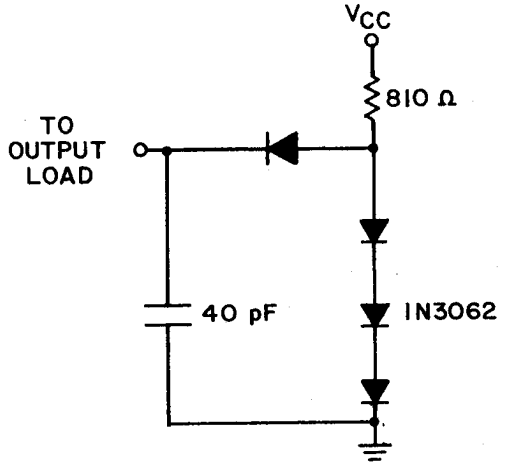

FIGURE 5. Load circuit for delay measurements.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	1,4,7,9
Final electrical test parameters (method 5004)	1*,2,3,4,5, 6,7*,8,9,10,11
Group A test requirements (method 5005)	1,2,3,4,5,6 7,8,9,10,11
Groups C and D end-point electrical parameters (method 5005)	1,4,7,9

* PDA applies to subgroups 1 and 7.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, 6, 7, and 8 tests shall be sufficient to verify the truth table.

4.3.2 Groups C and D inspection.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.4 Approved source of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/
5962-8778601VX	59621	TDC1046J8V

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
59621	TRW LSI Products Incorporated 4243 Campus Point Court San Diego, CA 92126