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Defense Electronics Supply Center
Dayton, Ohio

Original date of drawing:
20 April 1987

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SIZE	CODE IDENT. NO.
	14933

REV

MILITARY DRAWING

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TITLE: MICROCIRCUIT, MONOLITHIC SILICON, BIPOLAR DYNAMIC MEMORY CONTROLLER

DWG NO. 5962-87574

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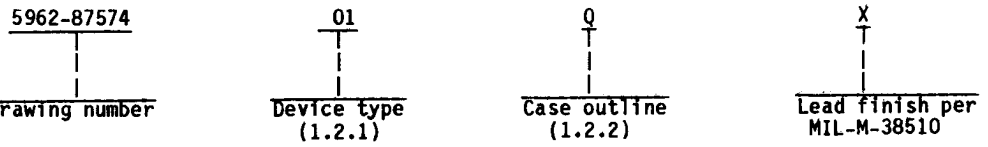
1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:



1.2.1 Device type. The device type shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	2964B	Dynamic memory controller

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
Q	D-5 (40-lead, 9/16" x 2 1/16"), dual-in-line package
U	C-5 (44-terminal. 650" x .650"), chip carrier package

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 V dc to +7.0 V dc
Input voltage range	-0.5 V dc to +5.5 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation, P_D 1/	0.9 W at T_C = 125°C
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (Q_{JC})	
Case Q	See MIL-M-38510, appendix C
Case U 2/	30°C/W
Junction temperature (T_J)	+155°C
DC voltage applied to outputs for high output state	-0.5 V dc to V_{CC} maximum
DC output current, into outputs	+20 mA
DC input current	-30 mA to +5.0 mA

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	+4.5 V dc minimum to +5.5 V dc maximum
Minimum high-level input voltage (V_{IH})	+2.0 V dc
Maximum low-level input voltage (V_{IL})	+0.8 V dc
Case operating temperature range (T_C)	-55°C to +125°C

1/ Must withstand the added P_D due to short circuit test (e.g., I_{SC}).
2/ When a thermal resistance value for this case is included in MIL-M-38510, appendix C, that value shall supersede the value indicated herein.

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth tables. The truth tables shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.2.4 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full recommended case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.5 herein.

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.5. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

Ceramic dual-in-line package

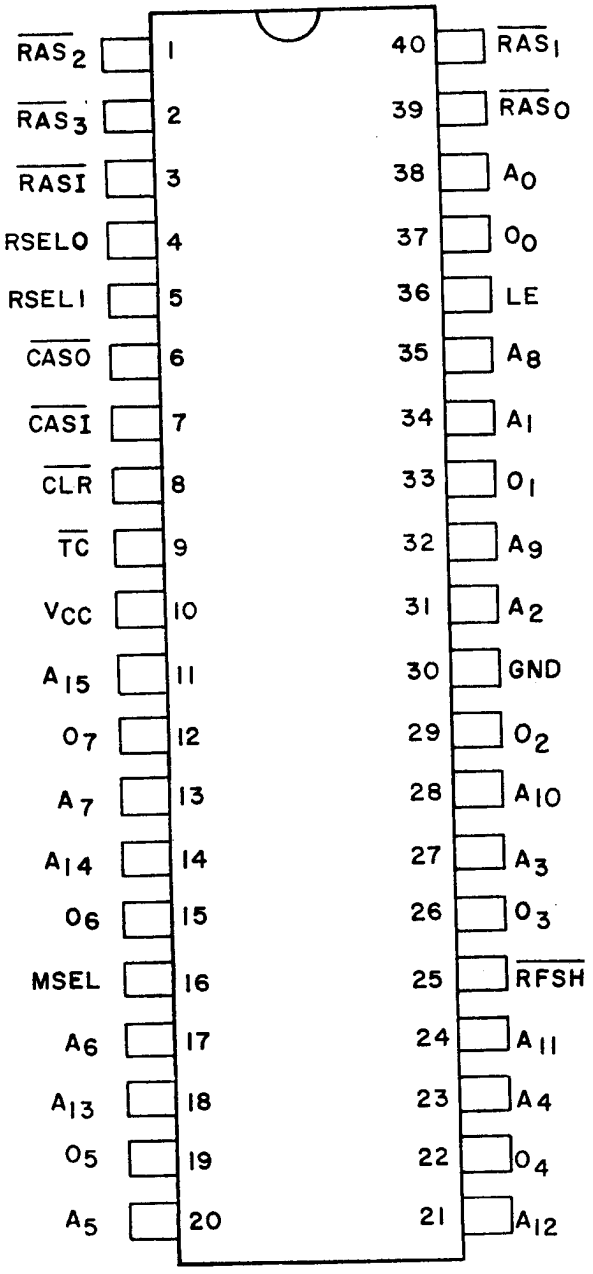


FIGURE 1. Terminal connections.

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Leadless chip carrier package

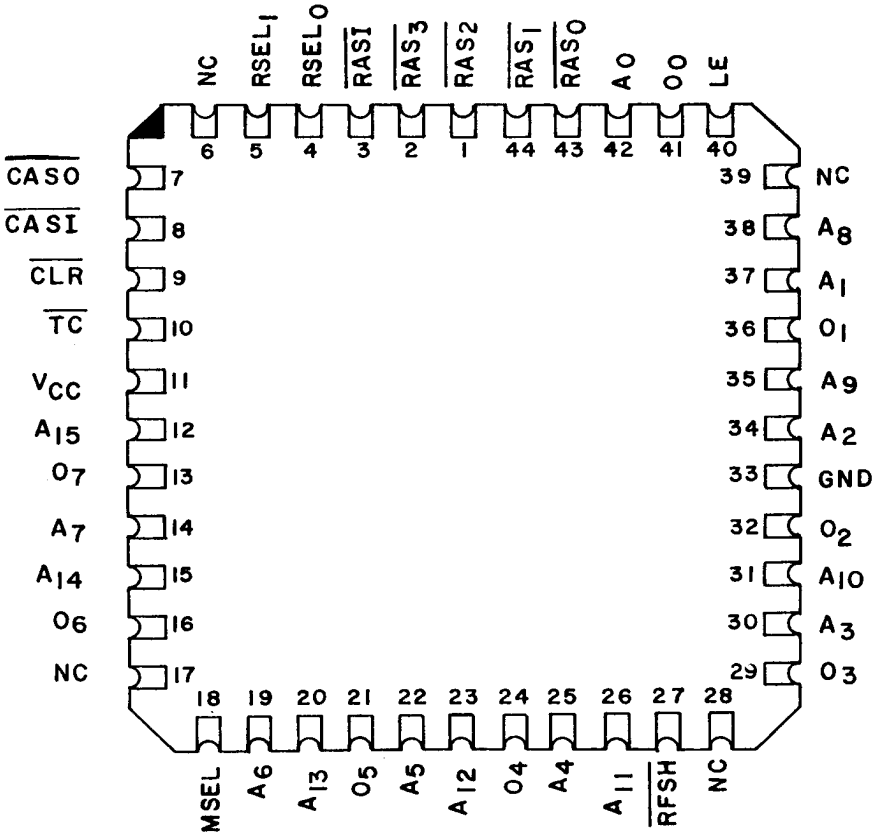

FIGURE 1. Terminal connections - Continued.

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$\overline{RAS}$ Output function table

$\overline{RFSH}$	$\overline{RASI}$	$RSEL_1$	$RSEL_0$	$\overline{RAS_0}$	$\overline{RAS_1}$	$\overline{RAS_2}$	$\overline{RAS_3}$
L	H	X	X	H	H	H	H
L	L	X	X	L	L	L	L
H	H	X	X	H	H	H	H
H	L	L	L	L	H	H	H
H	L	L	H	H	L	H	H
H	L	H	L	H	H	L	H
H	L	H	H	H	H	H	L

$\overline{CASO}$ function table

$\overline{RFSH}$	$\overline{CASI}$	$\overline{CASO}$
H	L	L
H	H	H
L	X	H

Address output function table

MSEL	$\overline{RFSH}$	O_0-O_7
H	H	A_0-A_7
L	H	A_8-A_{15}
X	L	Refresh address

FIGURE 2. Truth tables.

Refresh address counter function table

A_{15}	$\overline{CLR}$	$\overline{RFSH}$	$\overline{RASI}$	$\overline{TC}$	Refresh count	Function
X	L	X	X	X	FF_H	Clear counter
X	H	↓	X	X	NC	Output refresh address no change for counter
X	H	∫	L	X	Count - 1	Return to memory cycle mode and decrement counter
X	H	L	↓	X	NC	Output all $\overline{RAS}_i$ to RAM no change for counter
X	H	L	∫	X	Count - 1	Return $\overline{RAS}_i$ to HIGH and decrement counter
L or H	H	X	X	L	00_H	Terminal count for 256 line refresh
+12 V*	H	X	X	L	00_H and 80_H	Terminal count for 128 line refresh

*Through 1kΩ resistor.

FIGURE 2. Truth tables - Continued.

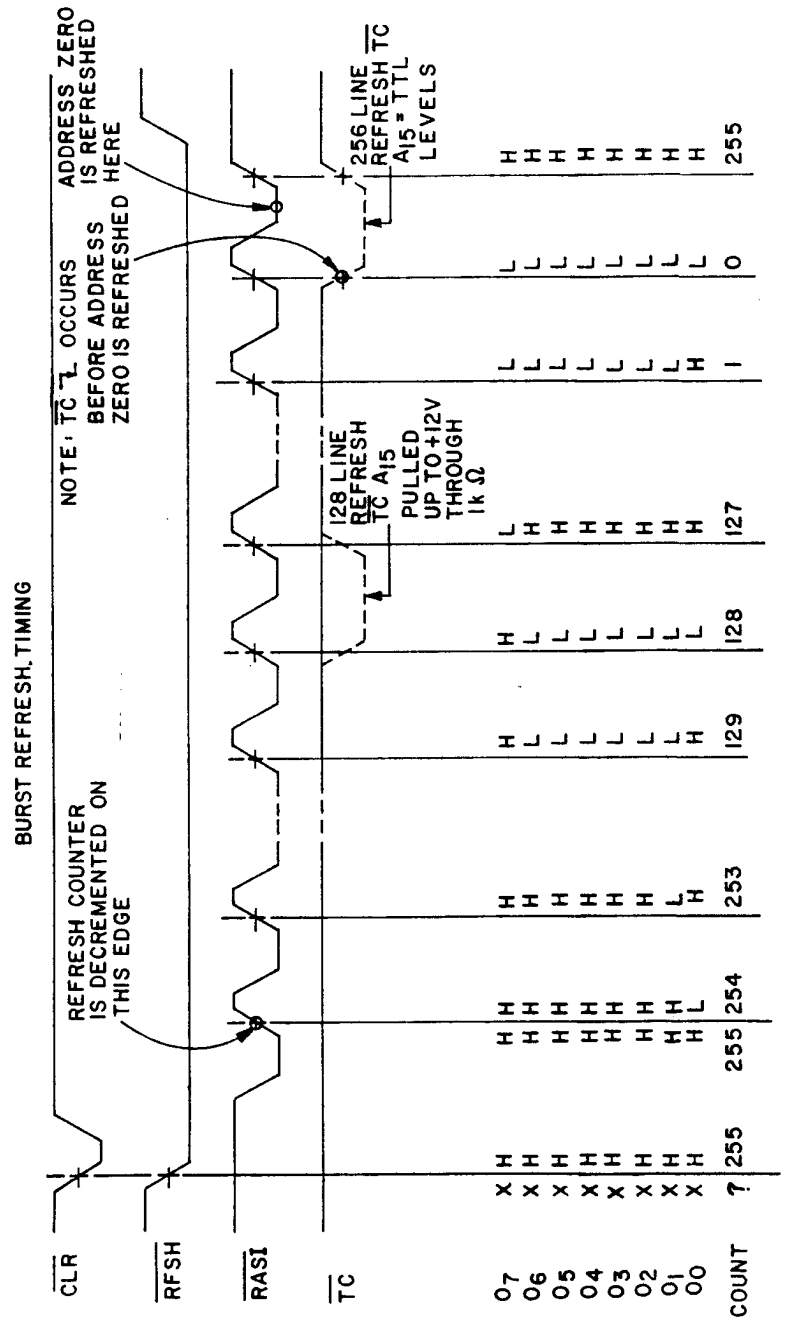

FIGURE 2. Truth tables - Continued.

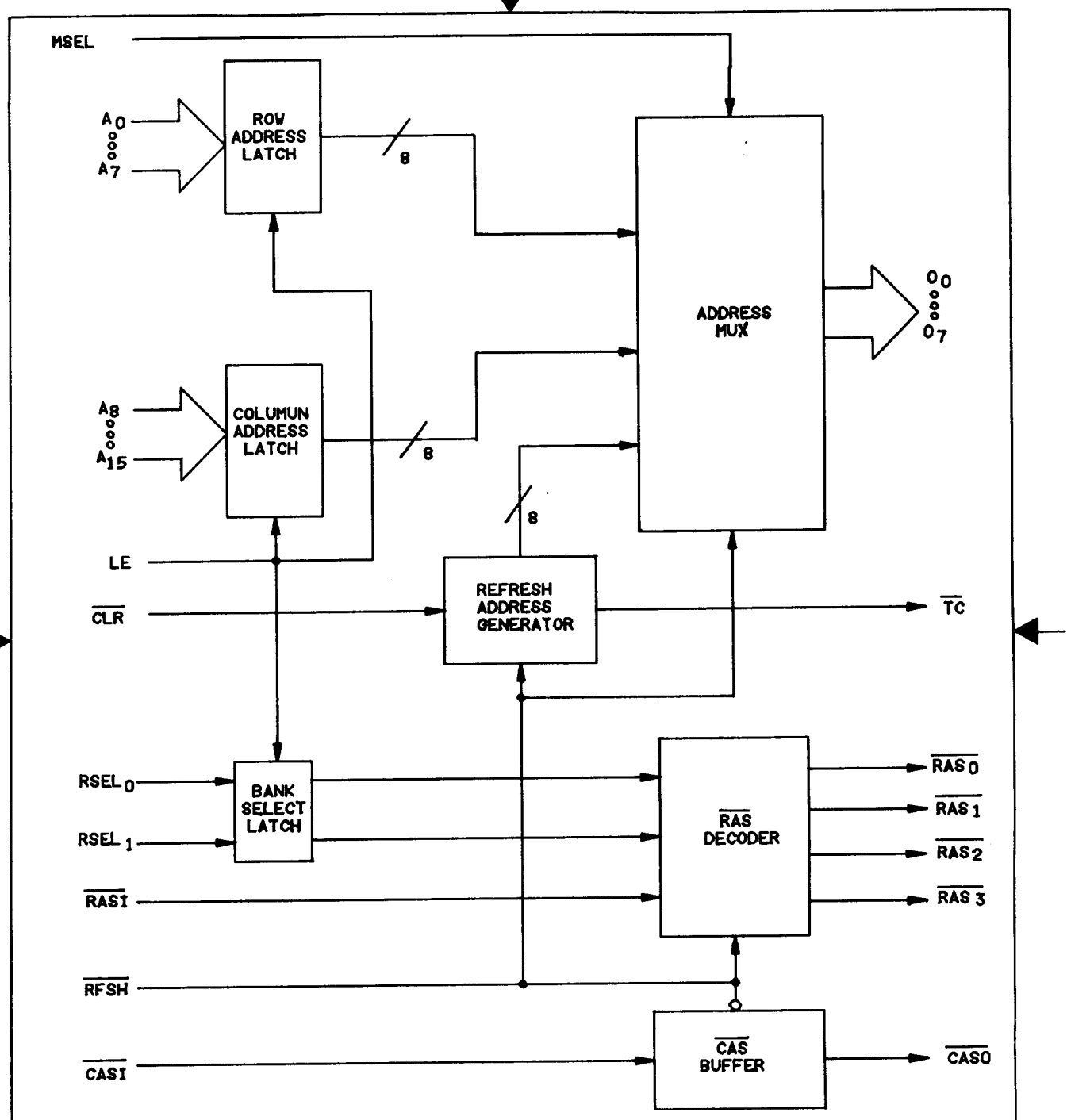

FIGURE 3. Block diagram.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified		Group A subgroups	Limits		Unit
					Min	Max	
Output high voltage	V_{OH}	V_{CC} = 4.5 V V_{IN} = V_{IH} or V_{IL} I_{OH} = -1 mA	$\overline{TC}$	1, 2, 3	2.5		V
			Others	1, 2, 3	3.0		V
Output high voltage	V_{OH}	V_{CC} = 4.5 V V_{IN} = V_{IH} or V_{IL} I_{OH} = -15 mA	All outputs except $\overline{TC}$	1, 2, 3	2.0		V
Output low voltage	V_{OL}	V_{CC} = 4.5 V V_{IN} = V_{IH} or V_{IL}	All outputs except $\overline{TC}$, I_{OL} = 16 mA	1, 2, 3		0.5	V
			$\overline{TC}$, I_{OL} = 8 mA	1, 2, 3		0.5	V
Input high level	V_{IH}	Guaranteed input logical high voltage for all inputs		1, 2, 3	2.0		V
Input low level	V_{IL}	Guaranteed input logical low voltage for all inputs		1, 2, 3		0.8	V
Input clamp voltage	V_I	V_{CC} = 4.5 V; I_{IN} = -18 mA		1, 2, 3		-1.5	V
Input low current	I_{IL}	V_{CC} = 5.5 V V_{IN} = 0.4 V	$\overline{RAS}$	1, 2, 3		-3.2	mA
			$\overline{CAS}$, MSEL, $\overline{RFSH}$	1, 2, 3		-1.6	mA
			A_0-A_{15}, $\overline{CLR}$ $RSEL_{0, 1}$, LE	1, 2, 3		-0.4	mA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified		Group A subgroups	Limits		Unit
					Min	Max	
Input high current	I_{IH}	V_{CC} = 5.5 V V_{IN} = 2.7 V	$\overline{RAS}$	1, 2, 3		100	µA
			$\overline{CAS}$, MSEL, $\overline{RFSH}$	1, 2, 3		50	µA
			A_0-A_{15}, $\overline{CLR}$ $RSEL_{0, 1,}$ LE	1, 2, 3		20	µA
Input high current	I_I	V_{CC} = 5.5 V V_{IN} = 5.5 V	$\overline{RAS}$	1, 2, 3		2.0	mA
			$\overline{CAS}$, MSEL, $\overline{RFSH}$	1, 2, 3		1.0	mA
			A_0-A_{15}, $\overline{CLR}$ $RSEL_{0, 1,}$ LE	1, 2, 3		0.1	mA
Output short circuit current	I_{SC}	V_{CC} = 5.5 V 1/		1, 2, 3	-40	-100	mA
Power supply current 2/	I_{CC}	-55°C and +25°C		1, 3		164	mA
		+125°C		2		150	mA
A_{15} Enable current	I_T	A_{15} Connected to +12 V through 1 Kohm ±10%		1, 2, 3		5	mA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} < 5.5\ V$ 3/, 4/, 5/	Parameter reference number (see figure 4)	Group A subgroups	Limits CL = 50 pF		Limits CL = 150 pF 6/		Unit
					Min	Max	Min	Max	
A_i to O_i Delay	t_{PD}		1	9, 10, 11		23		30	ns
$\overline{RASI}$ TO $\overline{RAST}$ ($\overline{RFSH}$ = H)	t_{PHL}		2	9, 10, 11		23		27	ns
$\overline{RASI}$ TO $\overline{RASI}$ ($\overline{RFSH}$ = L)	t_{PHL}		3	9, 10, 11		23		27	ns
MSEL to Oi	t_{PD}		4	9, 10, 11	5		7		ns
MSEL to Oi	t_{PD}		5	9, 10, 11		25		31	ns
$\overline{CASI}$ to $\overline{CASO}$ ($\overline{RFSH}$ = H)	t_{PHL}		6	9, 10, 11		19		26	ns
$\overline{RSELI}$ to $\overline{RAST}$ (LE = H, $\overline{RASI}$ = L)	t_{PHL}		7	9, 10, 11		24		30	ns
$\overline{RFSH}$ to $\overline{TC}$ ($\overline{RASI}$ = L)	t_{PLH}		8	9, 10, 11		50		55	ns
$\overline{RASI}$ to $\overline{TC}$ ($\overline{RFSH}$ = L)	t_{PLH}		9	9, 10, 11		40		55	ns
$\overline{RASI}$ = L ($\overline{RFSH}$ = L)	t_{PW}		10	9, 10, 11	50		50		ns
$\overline{RASI}$ = H ($\overline{RFSH}$ = L)	t_{PW}		11	9, 10, 11	50		50		ns
$\overline{RFSH}$ to Oi ($\overline{RASI}$ = X)	t_{PD}		12	9, 10, 11		25		30	ns
$\overline{RFSH}$ TO $\overline{RAST}$ ($\overline{RASI}$ = L)	t_{PHL}		13	9, 10, 11		29		36	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ 3/, 4/, 5/	Parameter reference number (see figure 4)	Group A subgroups	Limits CL = 50 pF		Limits CL = 150 pF 6/		Unit
					Min	Max	Min	Max	
$\overline{CLR}$ = L	t_{PW}		14	9, 10, 11	35		35		ns
$\overline{RFSH}$ to $\overline{CASO}$ 7/ $\overline{RAST}$ = L, $\overline{CAST}$ = L	t_{PLH}		15	9, 10, 11		25		31	ns
LE TO Oi	t_{PD}		16	9, 10, 11		40		50	ns
LE to $\overline{RAST}$	t_{PHL}		17	9, 10, 11		45		54	ns
$\overline{CLR}$ TO $\overline{TC}$	t_{PLH}		18	9, 10, 11		56		60	ns
$\overline{CLR}$ TO Oi ($\overline{RFSH}$ = L)	t_{PLH}		19	9, 10, 11		54		62	ns
Ai to LE Set-up time 8/	t_S		20	9, 10, 11	5		5		ns
Ai to LE Hold time 8/	t_H		21	9, 10, 11	15		12		ns
RSELi to LE Set-up time 8/	t_S		22	9, 10, 11	5		5		ns
RSELi to LE Hold time 8/	t_H		23	9, 10, 11	25		25		ns
$\overline{CLR}$ Recover time	t_S		24	9, 10, 11	18		18		ns
Oi to $\overline{RAST}$ ($\overline{RFSH}$ = H) 9/	t_{SKEW}		25	9, 10, 11		6		7	ns
Oi to $\overline{CASO}$ 9/	t_{SKEW}		26	9, 10, 11		8		8	ns
Oi to $\overline{RAST}$ ($\overline{RFSH}$ = L) 10/	t_{SKEW}		27	9, 10, 11		10		10	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} < 5.5\ V$ 3/, 4/, 5/	Parameter reference number (see figure 4)	Group A subgroups	Limits CL = 50 pF		Limits CL = 150 pF 6/		Unit
					Min	Max	Min	Max	
Oi to $\overline{RAS}$ i MSEL = 7 11/	t_{SKEW}		28	9, 10, 11		5		5	ns

1/ Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

2/ I_{CC} is worst case when the address inputs are latched high, the refresh counter is at terminal count (255). $\overline{RAS}$i and $\overline{CAS}$i are high and all other inputs are low.

3/ Minimum spec limits for T_{PW}, t_S and t_H are minimum system operating requirements. Limits for t_{SKEW} and t_{PD} are guaranteed test limits for the device.

4/ All ac parameters are specified at the 1.5 V level.

5/ AC and function testing are performed at V_{IL} = 0 V and V_{IH} = 3.5 V.

6/ AC testing is performed to a 50 pF typical capacitive load. The ac limits for 150 pF are not tested, but are correlated to 50 pF measurements.

7/ $\overline{RFSH}$ inhibits $\overline{CAS}$o during refresh. Specification is for $\overline{CAS}$o inhibit time.

8/ Set-up and hold tests are not performed. These parameters are guaranteed by correlation and characterization.

9/ Oi to $\overline{RAS}$i ($\overline{RFSH}$ = high) skew is guaranteed maximum difference between fastest $\overline{RAS}$i to $\overline{RAS}$i delay and slowest Ai to Oi delay within a single device. Oi to $\overline{CAS}$o skew is maximum difference between fastest $\overline{CAS}$i to $\overline{CAS}$o delay and slowest MSEL to Oi delay within a single device.

10/ Oi to $\overline{RAS}$i ($\overline{RFSH}$ = low) skew is guaranteed maximum difference between fastest $\overline{RAS}$i to $\overline{RAS}$i delay and slowest $\overline{RFSH}$ to Oi delay within a single device.

11/ Oi to $\overline{RAS}$i (MSEL = 7) skew is guaranteed maximum difference between fastest MSEL 7 to Oi delay and slowest $\overline{RAS}$i to $\overline{RAS}$i delay within a single device.

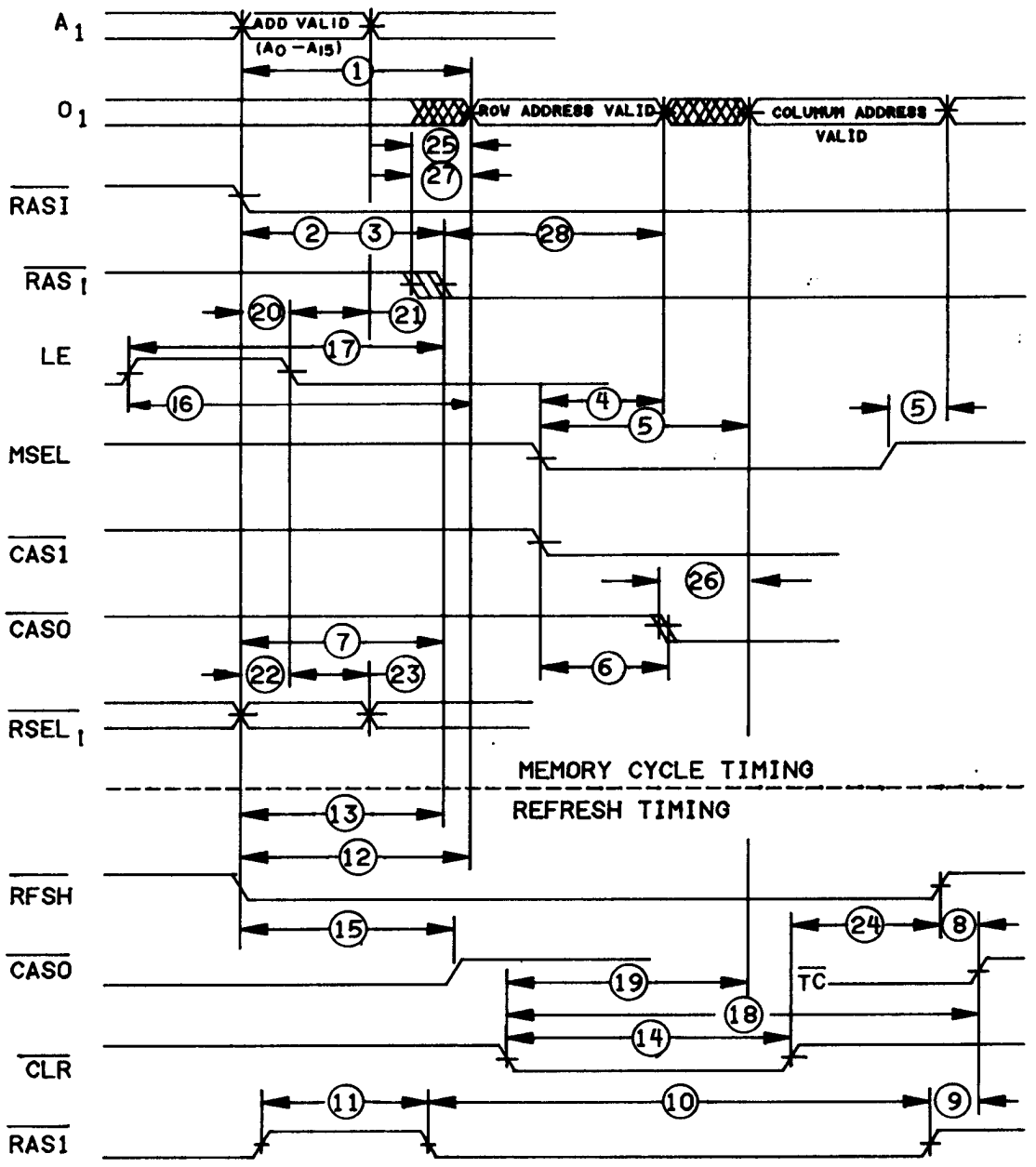

FIGURE 4. Dynamic memory controller timing.

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3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test (method 1015 of MIL-STD-883).

(1) Test condition A, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 7 and 8 tests shall verify the function table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test (method 1005 of MIL-STD-883) conditions:

(1) Test condition A, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by appendix B of MIL-M-38510 and method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Initial electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 7, 8 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 7, 9
Additional electrical subgroups for group C periodic inspections	---

* PDA applies to subgroup 1.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.4 Pin description.

Pin number	Name	I/O	Description
	A_0 - A_7	I	The low order address inputs are used to latch eight row address inputs for the RAM. These inputs drive the outputs O_0 - O_7 when MSEL is high.
	A_8 - A_{15}	I	The high order Address inputs are used to latch eight column address inputs for the RAM. These inputs drive the outputs O_0 -O_7 when MSEL is low.
11	A_{15}	I	A_{15} is a dual input. With normal TTL level inputs A_{15} acts as address input for 64K RAMs. If A_{15} is pulled up to +12 V through a 1 kilohm resistor, the terminal count output, $\overline{TC}$ will go low every 128 counts (for 16K RAMs) instead of every 256 counts.
	O_0 - O_7	O	The RAM address output. The eight-bit width is designed for dynamic RAMs up to 64K.
16	MSEL	I	The multiplexer-select input determines whether low order or high order address input appear at the multiplexer outputs O_0 - O_7. When MSEL is high, the low order address latches (A_0 -A_7) are connected to the outputs. When MSEL is low the high order address latches are connected to the outputs.
25	$\overline{RFSH}$	I	The refresh control input. When active low the $\overline{RFSH}$ input switches the address output multiplexer to output the inverted contents of the eight-bit refresher counter. $\overline{RFSH}$ low also inhibits the $\overline{CAS}$ buffer and changes the mode of the $\overline{RAS}$ decoder from one-of-four to four of four so that all four $\overline{RAS}$ decoder outputs, $\overline{RAS_0}$, $\overline{RAS_1}$, $\overline{RAS_2}$, and $\overline{RAS_3}$ go low in response to a low input at $\overline{RASI}$. This action refreshes one row address in each of the four $\overline{RAS}$ decoded memory banks. The refresh counter is advanced at the end of each refresh cycle by the low-to-high transition of $\overline{RFSH}$ or $\overline{RASI}$ (whichever occurs first). In burst mode refresh, $\overline{RFSH}$ may be held low and refresh accomplished by toggling $\overline{RASI}$.
9	$\overline{TC}$	O	The terminal count output. A low output at $\overline{TC}$ indicates that the refresh counter has been sequenced through either 128 or 256 refresh addresses depending on the A_{15}. The $\overline{TC}$ output remains active low until the refresh counter is advanced by the rising edge of $\overline{RASI}$ or $\overline{RFSH}$.

Pin number	Name	I/O	Description
8	$\overline{CLR}$	I	The refresh counter clear input. An active low input at $\overline{CLR}$ resets the refresh counter to all low (refresh address output to all high).
36	LE	I	The adress latch enable input. An active high input at LE causes the two 8-bit address latches and the 2-bit $\overline{RAS}$ select input latch to go transparent, accepting new input data. A low input on LE latches the input data which meet set-up and hold time requirements.
4, 5	$RSEL_0$ and $RSEL_1$	I	The $\overline{RAS}$ decoder Select inputs. Data (latched) at these inputs normally higher order addresses) is decoded by the $\overline{RAS}$ decoder to "$\overline{RAS}$ select" one of four banks of memory with $\overline{RAS_0}$, $\overline{RAS_1}$, $\overline{RAS_2}$ or $\overline{RAS_3}$.
3	$\overline{RAST}$	I	The row address strobe input. During normal memory cycles the selected $\overline{RAS}$ decoder output $\overline{RAS_0}$, $\overline{RAS_1}$, $\overline{RAS_2}$, or $\overline{RAS_3}$ will go active LOW in response to an active low input at $\overline{RAST}$. During refresh ($\overline{RFSH}$ = low), all $\overline{RAS}$ outputs go low in response to $\overline{RAST}$ = low.
39, 40, 1, 2	$\overline{RAS_0}$, $\overline{RAS_1}$, $\overline{RAS_2}$, $\overline{RAS_3}$,	O	Row address strobe outputs ($\overline{RAST}$). Each provides a row address strobe outputs for one of the four banks of memory. Each will go active low only when selected by $RSEL_0$ and $RSEL_1$ and only when $\overline{RAST}$ goes active low. All $\overline{RAS_{0-3}}$ outputs go active low in response to $\overline{RAST}$ when $\overline{RFSH}$ goes low.
7	$\overline{CAST}$	I	The column address strobe. An active low input at $\overline{CAST}$ will result in an active LOW output at $\overline{CASO}$, unless a refresh cycle is in progress ($\overline{RFSH}$ = low).
6	$\overline{CASO}$	O	The column address strobe output. The active low $\overline{CASO}$ output strobes the column address into the dynamic RAM, $\overline{CASO}$ is inhibited during refresh ($\overline{RFSH}$ = low).

6.5 Approved sources of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/	Replacement military specification part number
5962-87574O1QX	34335	AM2964B/BQA	
5962-87574O1UX	34335	AM2964B/BUA	

1/ Caution. Do not use this number for item acquisition. Items acquired to the similar vendor type only may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34335	Advanced Micro Devices, Inc. 901 Thompson Place Sunnyvale, CA 94088