This Preliminary data sheet provides detailed functional capabilities for product currently in prototype production. These specifications are being provided to allow for electrical design, layout and operation.

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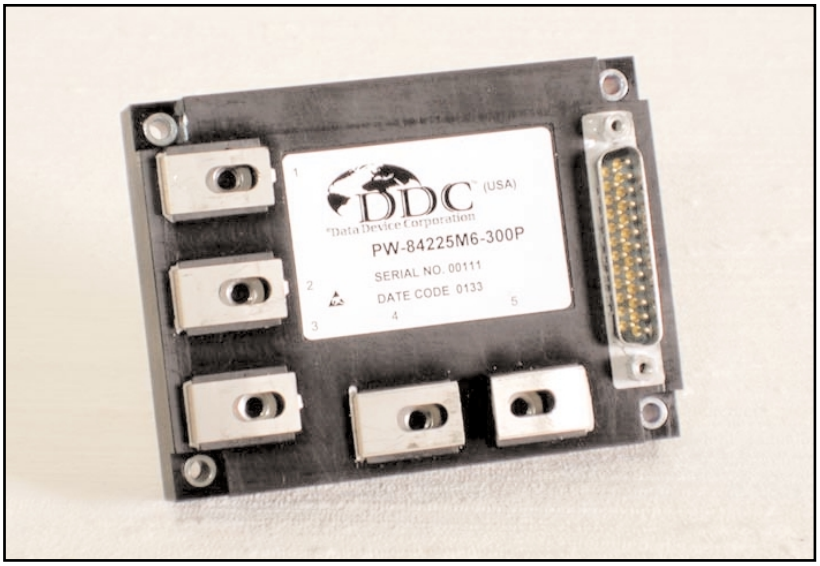
PW-8X225M6
225A, 600V MAGNUM MOTOR DRIVE



DESCRIPTION

The PW-83225M6, PW-84225M6 and PW-85225M6 are half-bridge drive modules containing isolated switch drivers, an upper and lower solid-state switch, and an isolated power supply. In addition, the PW-84225M6 contains isolated current sensing feedback circuitry and the PW-85225M6 contains a regenerative clamp protection circuit.

The three modules can be used in any combination to create drives for brush, brushless DC, or AC induction motors. The current sense output signal and logic inputs are compatible with DSP/ microprocessors and/or FPGA/ASIC circuits used to control the motor drives. These modular drives are capable of operating from either a ±135Vdc or 270Vdc power source that is electrically isolated from the logic input signals. The modules are fault tolerant from output shorts, loss of any or all power supplies, and power supply sequencing.

APPLICATIONS

The high reliability and flexibility of these drives make them suitable for Military and Aerospace applications. Among the many applications are: actuator systems for primary and secondary flight controls on aircraft, fan and compressor motor drives for environment conditioning, pump motors for fuel and hydraulic fluid, antenna and radar positioning, and thrust vector position control of missiles, drones, and RPV's.

FEATURES

- 600 Vdc Drive for 270 Vdc Motors
- 215 Amps @85°C
- Operates with Brushless, Brush, and Induction Motors
- Input to Output Ground Isolation with Floating Output Stage
- Short Circuit Protection
- Trapezoidal or Sinusoidal Compatible
- DSP/Microprocessor Compatible
- PW-83225M6 - Half-Bridge Drive
- PW-84225M6 - Half-Bridge Drive with Current Sense
- PW-85225M6 - Half-Bridge Drive with Regenerative Clamp

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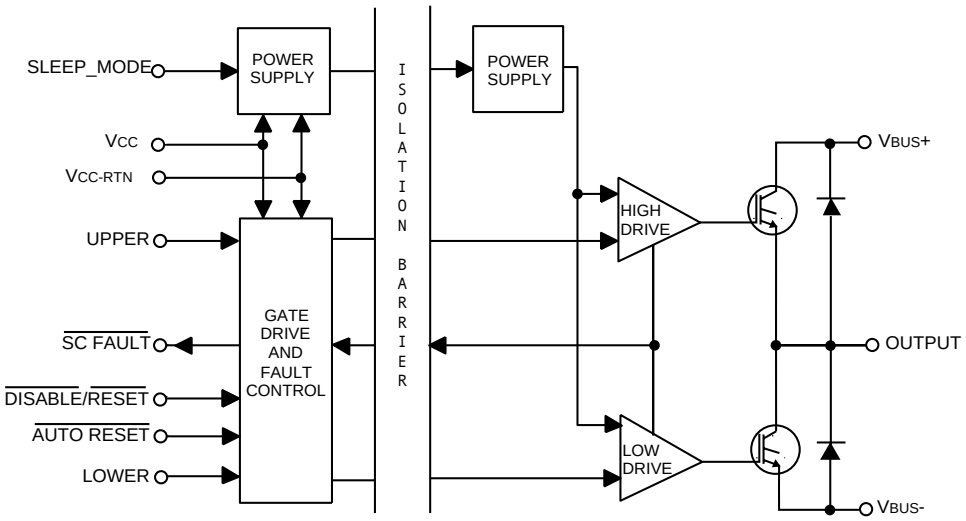


FIGURE 1A. PW-83225M6

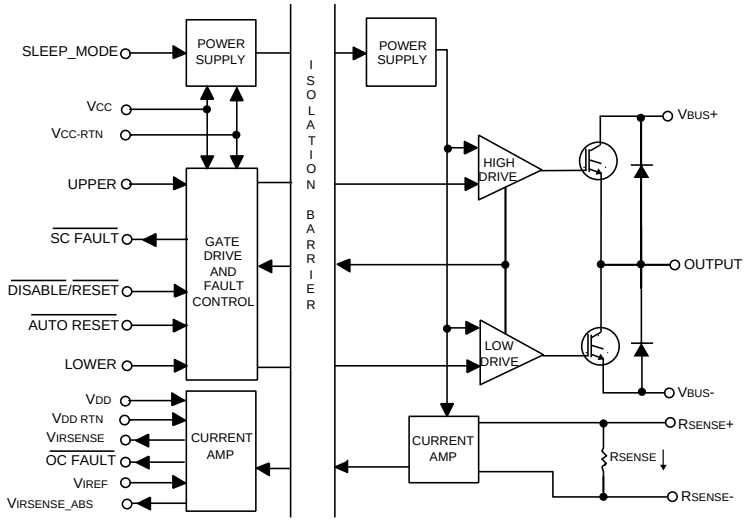


FIGURE 1B. PW-84225M6

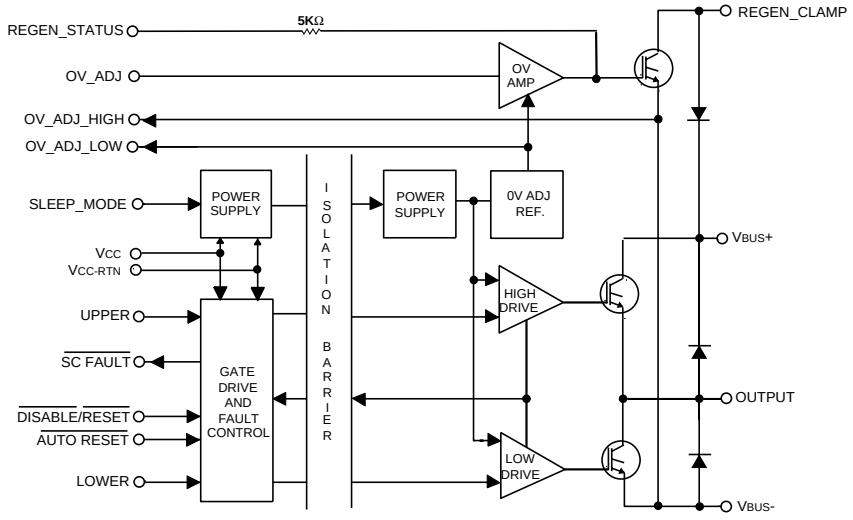


FIGURE 1C. PW-85225M6

TABLE 1. PW-8X225M6 ABSOLUTE MAXIMUM RATINGS TC = 25°C			
PARAMETER	**SYMBOL**	**VALUE**	**UNITS**
Drive Supply Voltage	V_{BUS}+ to V_{BUS}-	600	Vdc
Logic Power-In Supply Voltage	V_{CC}	5.5	Vdc
Input Logic Voltage	UPPER, LOWER, $\overline{\text{DISABLE}}$/$\overline{\text{RESET}}$, SLEEP_MODE, $\overline{\text{AUTO RESET}}$	5.5	Vdc
Reference Input Voltage	V_{IREF}	V_{DD} + 0.5 Vdc	Vdc
Continuous Output Current	I_O	225	A
Peak Output Current (<10mS)	I_{PEAK}	400	A
Storage Temperature Range	TCS	-65 to +125	°C
Intermittent Case Operating Temperature	TCI	-55 to +125	°C
Continuous Case Operating Temperature	TC	-55 to +100	°C
Junction Temperature, Power Devices	Tj	+150	°C
Junction Temperature, Other Components	Tj	+125	°C
Isolation Voltage (Note 2)	V_{ISO}	2500	Vdc

Note 1: In all tables TC refers to the temperature of the Magnum heat sink surface.
Note 2: From V_{CC-RTN} to V_{BUS}+, V_{BUS}-, OUTPUT, REGEN_CLAMP, R_{SENSE}+, R_{SENSE}-.

TABLE 2. PW-8X225M6 SPECIFICATIONS V_{CC} = V_{DD} = 5V UNLESS OTHERWISE NOTED, TC = -55°C TO 100°C FOR MIN. AND MAX VALUES, TC = 25°C FOR TYP VALUES (SEE NOTE 1).						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
OUTPUT STAGE						
Drive Supply Voltage (motor) Output Switch Transistors (each)	V_{BUS}+ to V_{BUS}-	Unipolar/Bipolar		270	600	Vdc
Output Current Continuous Drive (DC)	I_O	TC = 25°C, non switching DC			215	A
	I_O	TC = 85°C, non switching DC			150	A
Output Current Commutating Drive	I_O	TC = +25 to +85°C, 3 phase drive, 50% duty cycle, 20 KHz switching			215	A
Turn-on energy per pulse	E_{ON}	V_{CE} = 270V, I = 50A Tj = +125°C		1.8		mJ
Turn-off energy per pulse	E_{OFF}	V_{CE} = 270V, I = 50A Tj = +125°C		14.4		mJ
Peak Current	I_{PEAK}	TC = +25°C, ≤ 15 ms			360	A
Short Circuit Trip Current (Note 2)	I_{SC}	<5 µs	600	900	1200	A
Output Voltage Drop (IGBT)	$V_{CE(SAT)}$	I_O = 145A		2.2	2.6	Vdc
FLYBACK VOLTAGE						
Forward Voltage	V_F	I_O = 145A		1.45	1.65	Vdc
Reverse Recovery Time @ T j = +125° C	trr	I_O = 145A		180		ns
Reverse recovery Peak Current	Irr	di/dt = 480A/µs, IF = 150 A (90°C)		60	80	A
Reverse Leakage Current @ T j = +25° C	Ir	V_{BUS} = 480Vdc			1100	µA
Reverse Leakage Current @T j = +125° C	Ir	V_{BUS} = 480Vdc			6.0	mA
OUTPUT SWITCHING CHARACTERISTICS (SEE FIGURE 5)						
Turn-on Propagation Delay	td (on)	Vbus = 350Vdc, Resistive load	390		1000	ns
Turn-off Propagation Delay	td (off)	Vbus = 350Vdc, Resistive load	740		1200	ns
Disable Propagation Delay	tsd			100		µs
Turn-on Rise Time	tr		50		200	ns
Turn-off Fall Time	tf		100		200	ns
Sleep_Mode Delay	tsleep		0.7		1.5	ms
Output Switching Frequency	fPWM		0	25		KHz

Note 1: In all tables TC refers to the temperature of the Magnum heat sink surface.
Note 2: V_{BUS}+ to V_{BUS}- must be ≥10V (during short circuit) for short circuit protection to operate.

TABLE 2. PW-8X225M6 SPECIFICATIONS (CONT.)
V_{CC} = V_{DD} = 5V UNLESS OTHERWISE NOTED,
T_C = -55°C TO 100°C FOR MIN. AND MAX VALUES, T_C = 25°C FOR TYP VALUES (SEE NOTE 1).

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
CONTROL INPUTS						
AUTO RESET						
High Level Input Voltage	V_{IH}	V_{CC} = 4.5V	1.55	2.5	3.15	Vdc
Low Level Input Voltage	V_{IL}	V_{CC} = 4.5V	0.9	1.6	2.45	Vdc
Hysteresis Voltage	V_{HYST}		0.4	0.9	2.1	Vdc
High Level Input Current	I_{IH}	Vin = V_{CC}		0	1.5	µA
Low Level Input Current	I_{IL}	Vin = 0V		1.5		mA
UPPER, LOWER						
High Level Input Current	I_{IH}	Vin = V_{CC}		20	21	µA
Low Level Input Current	I_{IL}	Vin = 0V	0	0.1	100	nA
DISABLE/RESET						
High Level Input Current	I_{IH}	Vin = V_{CC}			1.5	µA
Low Level Input Current	I_{IL}	Vin = 0V		3		µA
SLEEP_MODE						
High Level Input Voltage	V_{IH}	V_{CC} = 4.5V	2.4			Vdc
Low Level Input Voltage	V_{IL}	V_{CC} = 4.5V			0.8	Vdc
High Level Input Current	I_{IH}	Vin = V_{CC}		0.1		µA
Low Level Input Current	I_{IL}	Vin = 0V		23		µA
UPPER-LOWER DEADTIME	tDEAD		0.6	1		µs
AUTO RESET Delay to output off	tdoff.auto			202		ms
AUTO RESET Delay to output enabled	tdon.auto			3		ms
RESET pulsewidth to clear SC FAULT	tpw.reset		300			ns
Cycle time between AUTO RESET retries	tcycle.auto	AUTO RESET tied to SC FAULT	40	100		ms
CONTROL OUTPUTS						
SC FAULT						
High Level Output Current	I_{SCFLTH}	Vo = V_{CC}	-80			µA
Low Level Output Current	I_{SCFLTL}	Vo = 0.4V		5	6	mA
THERMAL						
Maximum Thermal Resistance - IGBT	θjc	Each UPPER or LOWER		0.13	0.2	°C/W
Maximum Thermal Resistance - Diode	θjc			0.36	0.75	°C/W
Junction Temperature Range	Tj		-55		150	°C
Case Operating Temperature	Tc		-55		100	°C
Case Storage Temperature	Tcs		-65		125	°C
MECHANICAL						
Mounting Torque						
Hold down			10		12	in-lbs
Power Terminals			34		42	in-lbs
D-Connector Screws			5		65	in-lbs
Weight				17 (482)		oz (gm)

Note 1: In all tables T_C refers to the temperature of the Magnum heat sink surface.
Note 2: V_{BUS+} to V_{BUS-} must be ≥10V (during short circuit) for short circuit protection to operate.

TABLE 3. PW-83225M6 SPECIFICATIONS
V_{CC} = V_{DD} = 5V UNLESS OTHERWISE NOTED,
T_C = -55°C TO 100°C FOR MIN. AND MAX VALUES, T_C = 25°C FOR TYP VALUES (SEE NOTE 1).

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
POWER AND LOGIC SUPPLY						
Voltage	V_{CC}, V_{DD}		4.5	5	5.5	Vdc
Logic Supply Current (see Note 2)	I_{CC}	SLEEP_MODE			50	mA
	I_{CC}	fpwm = 25KHz		260	350	mA

Note 1: In all tables T_C refers to the temperature of the Magnum heat sink surface.
Note 2: During initial power-on @ Vcc~3.5VDC, a transient current pulse up to 100 mA above Icc may be observed.

TABLE 4. PW-84225M6 SPECIFICATIONS, V_{CC} = V_{DD} = 5V UNLESS OTHERWISE NOTED, T_C = -55°C TO 100°C FOR MIN. AND MAX VALUES, T_C = 25°C FOR TYP VALUES (SEE NOTE 1).						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
POWER AND LOGIC SUPPLY						
Voltage	V_{CC}, V_{DD}		4.5	5	5.5	Vdc
Logic Supply Current (see Note 2)	I_{CC}	SLEEP_MODE	15	25	50	mA
	I_{CC}	fpwm = 25Khz	150	260	350	mA
Current Amplifier Supply Current	I_{DD}			10	20	mA
CURRENT AMPLIFIER						
$V_{IRSENSE}$ Gain %	G_{VOUT}%	0A = V_{IREF}/2		0.185		%V_{IREF}/A
$V_{IRSENSE}$ Gain	G_{VOUT}	V_{IREF} = 5.0V		9.27		mV/A
$V_{IRSENSE}$ Gain ERROR	E_{VOUT}	0A = V_{IREF}/2	-7		7	%
$V_{IRSENSE}$ Offset %	V_{OS}%V_{IREF}	0A = V_{IREF}/2	-0.64		0.64	%V_{IREF}
$V_{IRSENSE}$ Offset	V_{OS}	V_{IREF} = 5.0V	-32		32	mV
$V_{IRSENSE}$ Offset % Drift	TC_{VOS}%	0A = V_{IREF}/2	-18		22	ppm of V_{IREF}/°C
$V_{IRSENSE}$ Offset Drift	TC_{VOS}	V_{IREF} = 5.0V	-90		130	µV/°C
$V_{IRSENSE\_ABS}$ Gain %	G_{VOUT}%	0A = 0V		0.372		%V_{IREF}/A
$V_{IRSENSE\_ABS}$ Gain	G_{VABS}	0A = 0V		18.6		mV/A
$V_{IRSENSE\_ABS}$ Gain ERROR	E_{VABS}		-9		9	%
$V_{IRSENSE\_ABS}$ Offset %	V_{OSABS} % V_{IREF}		-2.66		2.66	%V_{IREF}
$V_{IRSENSE\_ABS}$ Offset	V_{OSABS}	V_{IREF} = 5.0V	-133		133	mV
$V_{IRSENSE\_ABS}$ Offset % DRIFT	TC_{VOSABS}%		-18		22	ppm of V_{IREF}/°C
$V_{IRSENSE\_ABS}$ Offset DRIFT	TC_{VOSABS}	V_{IREF} = 5.0V	-90		110	µV/°C
Delay Time	tdelay	50A to 215A step		9	20	µs
Bandwidth	f_{BW}	-3 db	20	30		kHz
Linear Range	Irange			±215		A
OC FAULT Trip Level	I_{OC}	V_{IREF} = 5.0V	±246.2	±274	±299.7	A
Trip Delay Time	t_{IOC}	50A to 215A step, V_{IREF} = 5.0V		3	6	µs
Reference Voltage Current Input	I_{VIREF}			0.26	1	mA
Reference Voltage Input	V_{IREF}		4		V_{DD}	Vdc
$\overline{\text{OC FAULT}}$ (-55° TO 100°C)						
High Level Output Current	I_{OCFLTH}	V_O = V_{DD}		0.2	15	µA
Low Level Output Current	I_{OCFLTL}	V_O = 0.8V max			4	mA

Note 1: In all tables T_C refers to the temperature of the Magnum heat sink surface.
Note 2: During initial power-on @ Vcc~3.5VDC, a transient current pulse up to 100 mA above Icc may be observed.

TABLE 5. PW-85225M6 SPECIFICATIONS, V_{CC} = V_{DD} = 5V UNLESS OTHERWISE NOTED, T_C = -55°C TO 100°C FOR MIN. AND MAX VALUES, T_C = 25°C FOR TYP VALUES (SEE NOTE 1).						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
POWER AND LOGIC SUPPLY						
Voltage	V_{CC}		4.5	5	5.5	Vdc
Current (see Note 2)	I_{CC}	SLEEP_MODE		25	50	mA
	I_{CC}	fpwm = 25Khz		260	350	mA
OVERVOLTAGE TRANSISTOR (REGEN_CLAMP)						
Continuous Current Drive	Io	T_C = +25°C			75	A
	Io	T_C = +85°C			50	A
Peak Current	I_{PEAK}	T_C = +85°C, 15 ms			100	A
Output Voltage Drop (IGBT)	$V_{CE(SAT)}$	50A		2.5	3	Vdc
Reverse Leakage @ T J = +25°C	Ir	480 Vdc			200	µA
Reverse Leakage @ T J = +125°C	Ir	480 Vdc			1.0	mA
OVERVOLTAGE FLYBACK DIODE						
Reverse Leakage @ Tc = +25°C	Ir	480 Vdc			750	µA
Reverse Leakage @ Tc = +125°C	Ir	480 Vdc			20	mA
OVERVOLTAGE TRIP	V_{TRIP}	without external adjustment	358	400	440	Vdc
Trip Level Hysteresis	V_{HYST}		35	40	45	Vdc
REGEN STATUS (REF. TO VBUS-)						
High Level Output Voltage	V_{OH}status	No Load	11.4	12	12.6	Vdc
Low Level Output Voltage	V_{OL}status	No Load		0.2	0.4	Vdc
Output resistance	Rstatus		4.5	4.75	5	KΩ
Vtrip rise to status ON Delay	tdon.status			36		µs
Vtrip fall status OFF Delay	tdoff.status			48		µs
THERMAL						
Maximum Thermal Resistance				0.5	0.75	°C/W

Note 1: In all tables T_C refers to the temperature of the Magnum heat sink surface.
Note 2: During initial power-on @ Vcc~3.5VDC, a transient current pulse up to 100 mA above Icc may be observed.

INTRODUCTION

The PW-8X225M6 Magnum family is a series of universal modular half-bridge motor drives intended for use with brush, brushless, DC and AC induction motors in aerospace applications.

The PW-8X225M6 contains an isolation barrier between the power and control stages, that attenuates ground noise generated from the high speed, high power switching. All signals from the control to the power sections are isolated from power and ground of the other section. This eliminates false triggering of the input signals and the need for creative grounding schemes. The isolation barrier also allows the user to operate the output stage from either unipolar or bipolar power supplies without level shifting the input signals. A built in power supply located in the control stage provides power to all electronics in the power stage. This eliminates the need for refresh cycles or external power supplies for the gate drive circuitry and allows switching duty cycles from 0 - 100%. (Reference FIGURES 1A, 1B, and 1C)

The output power transistors on all modules are protected from a short circuit applied to the output pin. When a short circuit condition is detected, the output transistors are shut down and a flag $\overline{\text{SC FAULT}}$ is made active [logic low (L)] indicating a short has occurred. The PW-84225M6 contains additional current sensing circuitry that can monitor either motor current or DC bus current. The output voltage of the current sensing circuit can be used as a feedback signal in a servo drive to create a torque loop. (Reference FIGURE 1B)

All output power transistors can be protected from regenerative bus overvoltage when utilizing dynamic braking with the addition of one PW-85225M6 module. This module contains an overvoltage switch that is enabled when an overvoltage condition is detected. This switch is normally wired to an external (user supplied, application specific) load dump resistor to provide a load across the high voltage bus when overvoltage is detected. During an overvoltage condition, the status flag REGEN_STATUS is active (logic high (H)) indicating an overvoltage condition is occurring. (Reference FIGURE 1C)

MODULE AND I/O OPERATION

UPPER, LOWER (INPUTS)

UPPER and LOWER are active high CMOS Schmitt-trigger inputs that control the gate drives of the output transistors. (TTL compatibility requires external 10KΩ pull-up resistors) Each input is electrically isolated from the output. A dead band, as shown in FIGURE 2, between UPPER and LOWER inputs is necessary to prevent output cross conduction.

SC FAULT (OUTPUT)

$\overline{\text{SC FAULT}}$ is an active low open collector output signal that indicates when the output of the module has experienced a short circuit condition. $\overline{\text{SC FAULT}}$ will remain active until $\overline{\text{DISABLE/RESET}}$ is made active (L). The signal is inactive at a logic high (H) during normal operation.

See SHORT CIRCUIT PROTECTION for more detail.

DISABLE/RESET (INPUT)

$\overline{\text{DISABLE/RESET}}$ is an active low CMOS Schmitt-trigger input. When $\overline{\text{DISABLE/RESET}}$ is held active it does two things:

1.) Resets the $\overline{\text{SC FAULT}}$ (if it was active), and

2.) Disables the output (makes the output high impedance)

If this line is used solely to clear $\overline{\text{SC FAULT}}$ then it only needs to be pulsed active. The width of the active pulse must be at least the width of the trip reset pulse (100ns) to ensure that $\overline{\text{SC FAULT}}$ is cleared properly. When this line is inactive, the OUTPUT is allowed to respond to the other control lines of the module (UPPER, LOWER, SLEEP_MODE).

Note: TTL compatibility requires an external pull-up resistor.

AUTO RESET (INPUT)

$\overline{\text{AUTO RESET}}$ is an active low (L) input. When $\overline{\text{AUTO RESET}}$ is tied to $\overline{\text{SC FAULT}}$ the protection circuit will reset automatically after the short circuit fault has occurred. This automatic reset enables the output to respond to the input commands.

See SHORT CIRCUIT PROTECTION for more detail.

SHORT CIRCUIT PROTECTION

The PW-8X225M6 modules have provisions for complete short circuit protection from either a hard or soft short to the V_{BUS}+ or V_{BUS}- lines.

Each output transistor on all PW-8X225M6 modules is protected from a hard (direct, low impedance) short to the V_{BUS}+ or V_{BUS}-

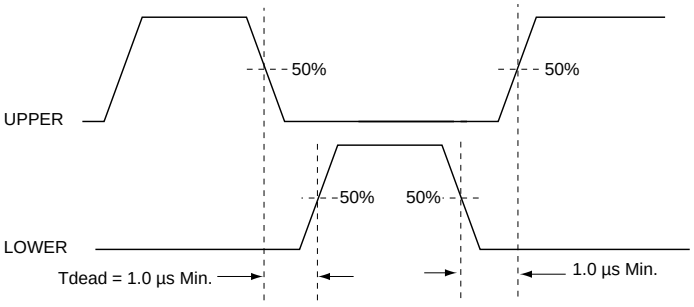


FIGURE 2. PW-8X225M6 DEAD BAND REQUIREMENT

lines by circuitry that detects the de-saturation voltage for that transistor during a short condition. Once a hard short circuit condition is detected, the active output transistors are shut down and SC FAULT output is set active [logic low (L)]. The SC FAULT signal can be used by a controller as a signal to initiate a fault routine to reset or shut down the system. The DISABLE/RESET input can be used to shut down the gate drivers if a short persists. If the AUTO RESET is tied to SC FAULT, the circuit will automatically reset when a fault occurs. This inactivates SC FAULT and reactivates the output transistor within 40 to 100ms. If the short is still present, the circuit will repeat the shut down and automatically reset until the short is clear.

Protecting against a soft short requires the addition of PW-84225M6 modules for current sensing and external circuitry. When a soft short occurs, the external circuit can set DISABLE/RESET low (L) to shut down the gate drivers.

SLEEP_MODE (INPUT)

SLEEP_MODE is an active high input that turns the internal power supply off. A logic low (L) enables the power supply and allows the motor drive to operate normally.

A logic high (H) on the SLEEP_MODE input disables the internal power supply, disabling the motor drive output. No damage will occur to the motor drive during turn on or turn off of the power supply. Additionally, no special power up sequence is required.

The UPPER and LOWER logic gate driver inputs should not be active while transitioning in and out of sleep mode. If the UPPER and LOWER logic inputs must be active while entering sleep mode then DISABLE/RESET must be held active while coming out of sleep mode.

Note: SLEEP_MODE has an internal pull-up resistor. If the input is not connected, it will default to logic high, turning the power supply and the motor drive off.

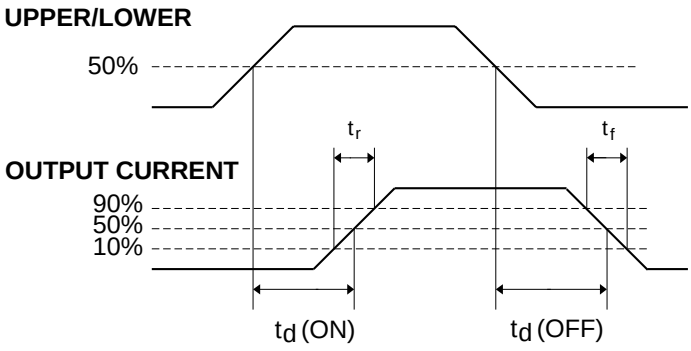


FIGURE 3. PW-8X225M6 INPUT/OUTPUT TIMING RELATIONSHIP

VCC, VCC-RTN (INPUTS)

The VCC and VCC-RTN are power connections that supply input power to the internal power supply, the gate drive and fault control circuits.

VBUS+, VBUS- (INPUTS)

VBUS+ and VBUS- are the high voltage power connections to the output stage. The high voltage can be either unipolar (+V and ground) or bipolar (+/- V). Care must be taken to ensure that the transient bus voltage VBUS at the module terminals never exceeds the absolute maximum supply ratings during switching excursions. External capacitor filtering will be required (See DDC applications note AN/H-7).

OUTPUT (OUTPUT)

Output is the power switch output that is connected to one input of the motor and applies VBUS+, VBUS-, or high impedance to the motor based on the state of the control inputs. FIGURE 3 illustrates the timing relationship between the output and the UPPER/LOWER inputs. The output is capable of sourcing or sinking up to 215 Amps, and can withstand a short circuit to VBUS+ or VBUS- without any damage by automatically turning itself off (Zstate).

VDD, VDD- RTN (APPLIES TO THE PW-84225M6 ONLY)

VDD and VDD-RTN supplies input power to the current amplifier.

VIRSENSE (OUTPUT) (APPLIES TO PW-84225M6 ONLY)

VIRSENSE is an output that provides a voltage proportional to the current passing through RSENSE. The voltage is scaled by a reference voltage VREF and is equal to VREF/2 to represent zero current. A voltage greater than VIREF/2 indicates a positive current flow (positive voltage from RSENSE + to RSENSE -) through RSENSE. See FIGURE 1B.

This VIRSENSE voltage is scaled by the input voltage at VIREF, where

VIRSENSE = (VIREF/2) + (VIREF/540) * (IRSENSE)

Note: IRSENSE is current through RSENSE = 108mΩ. Zero amps in RSENSE is indicated when VIRSENSE = VIREF/2. A voltage greater (less) than VIREF/2 indicates a positive (negative) current flow through RSENSE with a value defined by the VIRSENSE equation. VIRSENSE is electrically isolated from the output stage. A Positive (negative) current flow from RSENSE + to RSENSE - produces a positive (negative) voltage measurement (See FIGURE 1B). When the power supply is shut down (SLEEP_MODE input high), the voltage at VIRSENSE will indicate 0V.

VIREF (INPUT) (APPLIES TO PW-84225M6 ONLY)

A precision voltage reference from an external source is connected to the VIREF pin to set the output voltage scale for VIRSENSE and VIRSENSE_ABS. Note: The accuracy of the VIRSENSE and VIRSENSE_ABS outputs are subject to the accuracy and tem-

perature coefficient of VIREF. These must be taken into account in calculating the overall accuracy of VIRSENSE.

RSENSE+, RSENSE- (INPUTS) (APPLIES TO PW-84225M6 ONLY)

The RSENSE+ and RSENSE- pins are connected to an internal shunt resistor and monitoring circuitry. These pins can be connected anywhere within the isolation restrictions on the pins (600V to power pins, 2500V to logic pins). These pins are typically connected in series with the output, VBUS+ or VBUS-, to measure motor drive current.

VIRSENSE_ABS (OUTPUT) (APPLIES TO PW-84225M6 ONLY)

VIRSENSE_ABS output voltage is the absolute value of the VIRSENSE voltage signal. VIRSENSE_ABS is zero volts when there is no current flowing through the RSENSE resistor. It will increase towards the value of VIREF as the current in RSENSE approaches either -274 or +274 amps (measurement limits of VIRSENSE). VIRSENSE_ABS is an open source output and is "wire-OR-able". When two or more VIRSENSE_ABS outputs are "wire-OR-ed", the highest voltage will appear on the common signal. A typical use for combining these outputs is for determining when an overload condition has occurred. The VIRSENSE_ABS voltage is scaled by the input voltage VIRSENSE where:

$$V_{IRSENSE\_ABS} = 2 \times [V_{IRSENSE} - V_{IREF}/2]$$

OC FAULT (OUTPUT) (APPLIES TO PW-84225M6 ONLY)

$\overline{\text{OC FAULT}}$ is an active low open drain output that goes active when the current flowing through RSENSE has exceeded the $\overline{\text{OC FAULT}}$ trip level. This signal is not latched like $\overline{\text{SC FAULT}}$, and goes inactive as soon as the over current condition stops.

REGEN_STATUS (OUTPUT) (APPLIES TO PW-85225M6 ONLY)

The REGEN_STATUS pin is referenced to VBUS-. It indicates the state of the regen clamp switch (H = on, L = off). An external opto-isolator input can be connected between REGEN_STATUS and VBUS- to translate this status to logic circuits if desired. The REGEN_STATUS output is connected to the 0V amp through a 5K resistor. When the regen clamp switch is active (inactive), the 0V amp sources +15V (0V) through the 5K resistor. (see FIGURE 1C)

REGEN_CLAMP (OUTPUT) (APPLIES TO PW-85225M6 ONLY) (REF. R20 ON FIGURES 13 AND 14)

An external load dump resistor is connected between REGEN_CLAMP and VBUS+. When VBUS+ reaches the overvoltage trip level set by the OV_ADJ, the internal clamp circuit will apply the load dump resistor from VBUS+ to the VBUS-, thereby dissipating the regenerative energy in the external resistor.

TABLE 6. PW-8X225 TRUTH TABLE

UPPER	LOWER	TEST A*	TEST B*	TEST C*	$\overline{\text{AUTO RESET}}$	$\overline{\text{DISABLE/RESET}}$	SLEEP_MODE	$\overline{\text{SC FAULT}}$	OUTPUT
1	0	1	0	0	1	1	0	1	VBUS+
0	1	1	0	0	1	1	0	1	VBUS-
1	0	0	1	0	1	1	0	1	VBUS+
0	1	0	1	0	1	1	0	1	VBUS-
1	0	0	0	1	1	1	0	1	VBUS+
0	1	0	0	1	1	1	0	1	VBUS-
1	0	1	1	1	1	1	0	1	VBUS+
0	1	1	1	1	1	1	0	1	VBUS-
0	0	1	1	1	1	1	0	0	Z
1	0	1	1	1	1	1	0	0	Z
0	1	1	1	1	1	1	0	0	Z
X	X	0	0	0	X	1	0	X	Z
X	X	X	X	X	X	0	0	X	Z
X	X	X	X	X	X	X	1	1	Z

X = Indicates this input is irrelevant
Z = High Impedance state (off)
Z (VBUSx) = SC FAULT will not inhibit a gate drive that did not generate the fault. The opposite gate drive may still activate the output (VBUSx state). Only the gate drive (upper or lower) that faulted is inhibited and the output stays high impedance (Zstate) when faulted driver is commanded active.

* Optional feature of PW-8X225M6-600 only.

OV_ADJ (INPUT) (APPLIES TO PW-85225M6 ONLY)

The PW-85225M6 is internally set for a trip voltage of 400V.

The trip point can be adjusted to a higher or lower voltage by connecting an external overvoltage adjust resistor R_{OV_ADJ} (Ref. R21 on FIGURES 13 and 14).

To set the OV trip point to a voltage above 400 volts connect R_{OV_ADJ} between the OV_ADJ and OV_ADJ_HIGH pins. To set the OV trip point to a voltage above 400 volts connect R_{OV_ADJ} between the OV_ADJ and OV_ADJ_LOW pins. The value of R_{OV_ADJ} for voltages above (below) 400 volts should be selected based upon FIGURES 4 and 5.

TEST A, TEST B, TEST C (PW-8X225M6-600 ONLY)

These logic inputs are used to test individual pairs (UPPER and LOWER) of output transistors within the module per TABLE 6. The intent is to provide the user with the capability to detect an open transistor within the parallel combination of output devices.

Note: When Test A, Test B, Test C are exercised individually, the device is not capable of delivering the rated current.

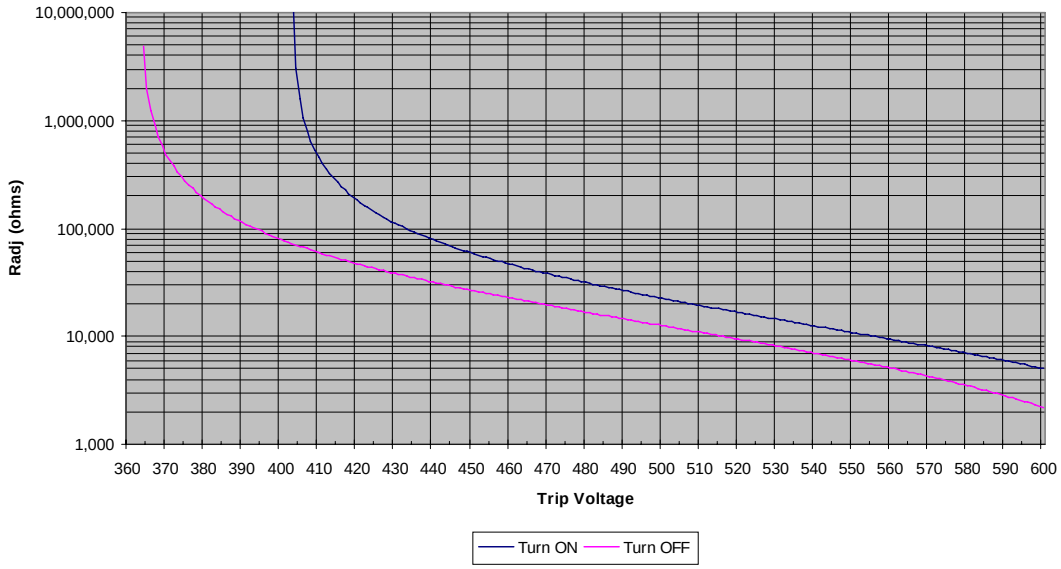


FIGURE 4. PW-8X225M6 OVERVOLTAGE TRIP VOLTAGE VS. RESISTANCE OF EXTERNAL RESISTOR CONNECTED BETWEEN OV_ADJ AND OV_ADJ_HIGH

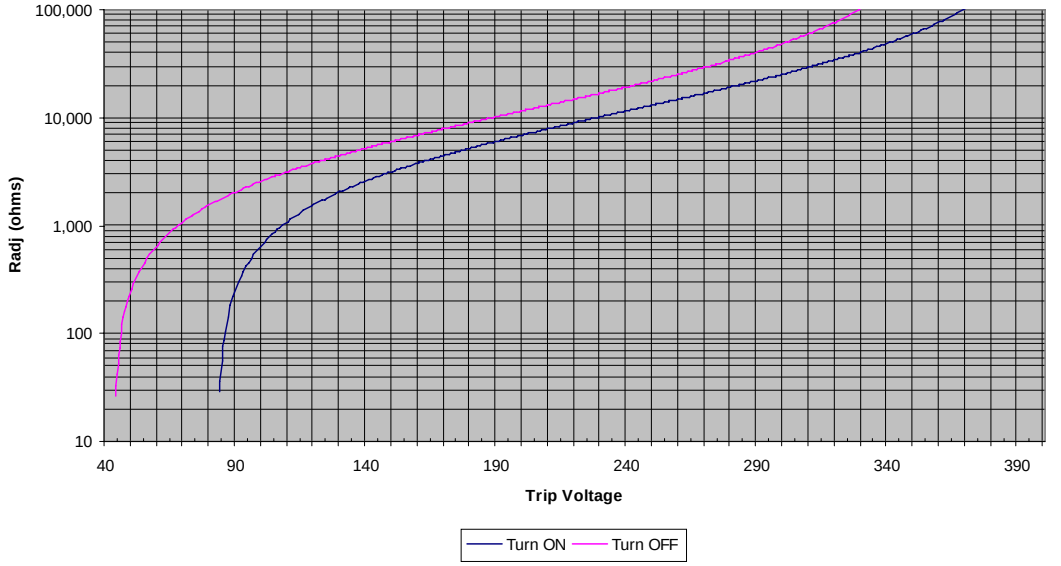


FIGURE 5. PW-8X225M6 TYPICAL OVERVOLTAGE TRIP VOLTAGE VS. RESISTANCE (IN OHMS) OF EXTERNAL RESISTOR ROV_ADJ CONNECTED BETWEEN OV_ADJ AND OV_ADJ_LOW

POWER DISSIPATION (SEE FIGURES 6 AND 7)

There are three major contributors to power dissipation in the motor driver: conduction losses, switching losses, and flyback diode losses. Consider the following operating conditions:

TCASE = 85 °C

VBUS = +270V

I_O = 40A

ton = 50µs ; T = 100µs (period)

$V_{CE(SAT)}$ = 2.2V (see TABLE 2 and FIGURES 6 and 7)

t_r = 200ns) t_f = 200ns

f_{PWM} = 10kHz (switching frequency)

V_F is the diode forward voltage, (TABLE 2), I_O = 50A, T_C = +25°C

V_F(avg) = 1.35V

$T_{J\ MAX}$ = 150 °C (TABLE 2, T_J) Θ_{JC} = 0.55°C/W (TABLE 2)

1. Conduction Losses (P_C)

$P_C = I_O \times V_{CE(SAT)} \times (ton / T)$
$P_C = 40A \times 2.2V \times (50µs / 100µs)$
$P_C = 44W$

2. Switching Losses ($P_{S\text{-}TOTAL}$)

$P_{S\text{-}TOTAL} = (P_{S\text{-}ON} + P_{S\text{-}OFF}) \times fpwm$
$P_{S\text{-}ON} = (E_{ON} \times (VBUS / 270) \times (I_O/50A))$
$P_{S\text{-}ON} = (4.0 \times (270 / 270) \times (40 / 50))$
$P_{S\text{-}ON} = 3.2$ mJ
$P_{S\text{-}OFF} = (E_{OFF} \times (V_{BUS}/270) \times (I_O/50))$
$P_{S\text{-}OFF} = (2.4$ mJ $\times (270/270) \times (40/50))$
$P_{S\text{-}OFF} = 1.92$ mJ
$P_{S\text{-}TOTAL} = 10000 \times (.0032 + .00192)$
$P_{S\text{-}TOTAL} = 51.2W$

3. Flyback diode Losses (Pdf)

$Pdf = I_O \times V_F(avg) \times (1- (ton / T))$
$Pdf = 40A \times 1.35V \times [1 - (50µs / 100µs)]$
$Pdf = 33.8W$

4. Transistor Power Dissipation (P_T)

$P_T = P_C + P_S = 95.2W$

5. Maximum Module Power Dissipation (P_{MAX})

To calculate the maximum power dissipation of the output transistor / diode pair as a function of the case temperature, use the following equation:

$P_{MAX} = ((T_{JMAX} - T_{CASE}) / \Theta_{JC})$
$118W = ((150\ °C - 85\ °C) / 0.55°C/W)$

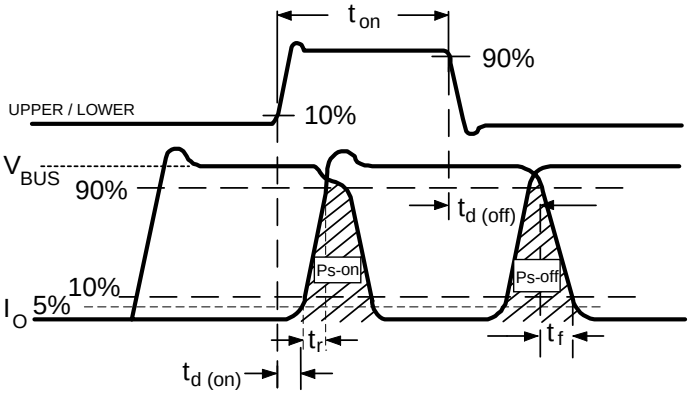


FIGURE 6. OUTPUT CHARACTERISTICS

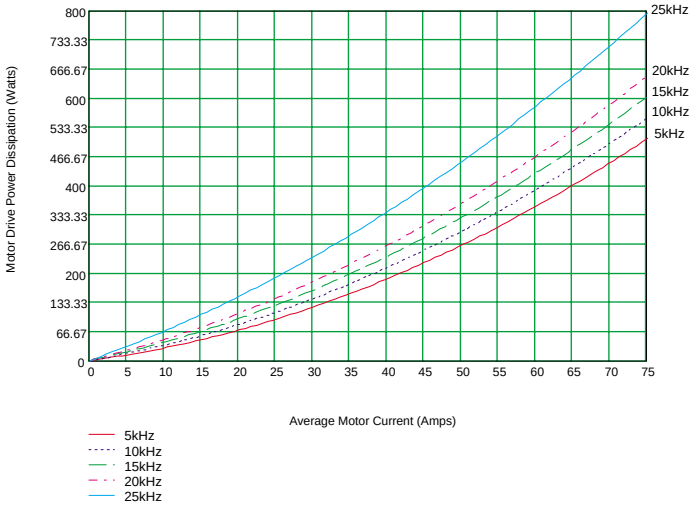


FIGURE 7. PW-8X2255 AVERAGE MOTOR CURRENT VS. MOTOR DRIVE POWER DISSIPATION

APPLICATIONS

The PW-8X225 3-module set can be easily used in a variety of applications, including motor position, velocity or torque control (see FIGURE 10). Examples of these applications are described below.

POSITION OR VELOCITY CONTROL USING DSP

FIGURE 13 shows an example of position and/or velocity control hook-up with inner torque loop using the Digital Signal Processor (DSP) for motor control. Using software, the DSP can be implemented with one of several motor control algorithms such as FOC (Field Oriented Control) with SVM (Space Vector modulation).

TORQUE HOOK-UP USING UC-2625 MOTOR CONTROLLER

FIGURE 14 shows an example of torque control loop with regenerative clamp protection using UC-2625, two PW-84225M6, and one PW-85225M6. Two PW-84225M6 (½ bridge with current sense) sense the current in motor phase B and C. VIRSENSE_ABS pins on each of the PW-84225M6 can be tied together to generate a single composite analog output which is compared to the torque commanded input to produce an error signal. UC2625 uses this error signal to regulate the output current (or torque) by controlling the duty cycle of the output transistors.

For the case when a resolver is available instead of Hall-effect devices, the circuit shown in FIGURE 15 converts the resolver (sin and cos) signals to Hall signals which can be used to commutate the output transistors.

HALL SIGNAL COMMUTATION

The hall signals HAB, HBC, HCA are logic signals from the motor Hall-effect sensors. The UC-2625 uses a phasing convention referred to as 120 degree spacing; that is, the output of HAB is in phase with motor back EMF voltage VAB, the output of HBC is in phase with motor back EMF voltage VBC, and the output of HCA is in phase with motor back EMF voltage VCA. Logic "1" (or HIGH) is defined by an input greater than 2.4Vdc or an open circuit to the controller; Logic "0"(or LOW) is defined as any Hall voltage input less than 0.8Vdc.

The UC-2625 will operate with Hall phasing of 60° or 120° electrical spacing. If 60° commutation is used, then the output of HCA must be inverted as shown in FIGURES 11 and 12. In FIGURE 11 the Hall sensor outputs are shown with the corresponding back EMF voltage they are in phase with.

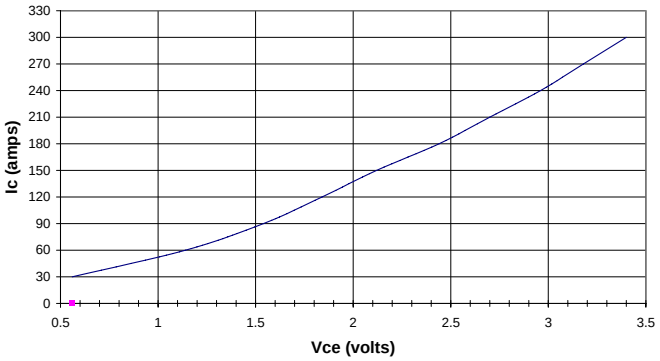


FIGURE 8. - SATURATION VOLTAGE CHARACTERISTICS

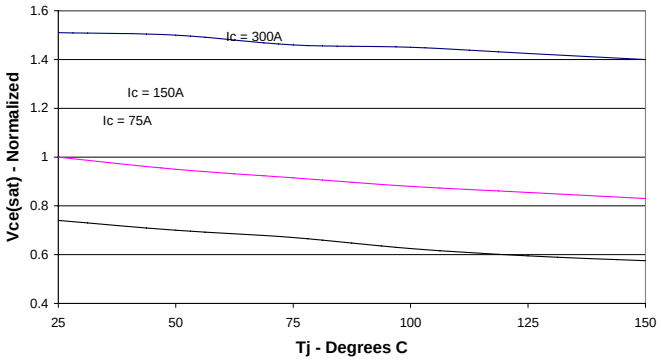


FIGURE 9. - TEMPERATURE DEPENDENCE OF VCE(SAT)

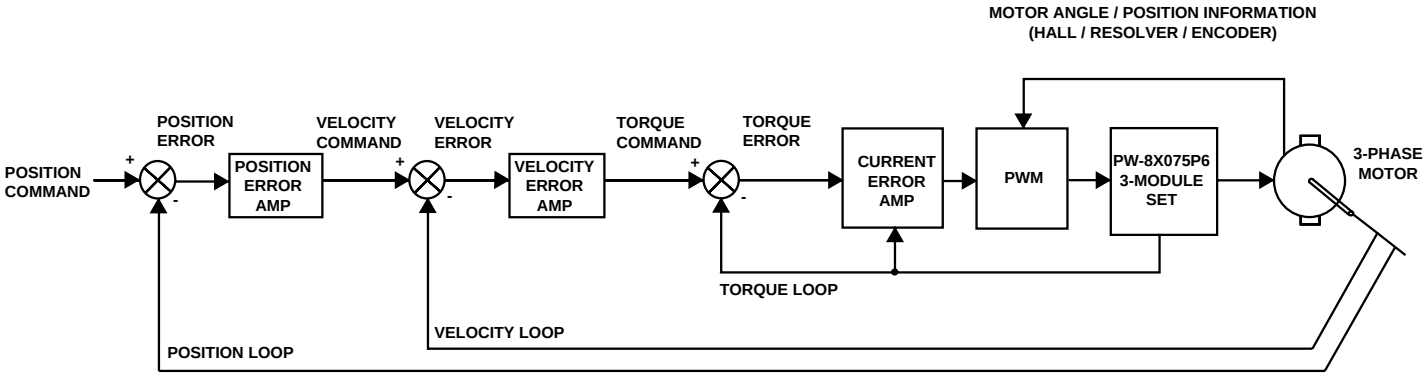


FIGURE 10. TYPICAL POSITION, VELOCITY AND TORQUE CONTROL LOOP

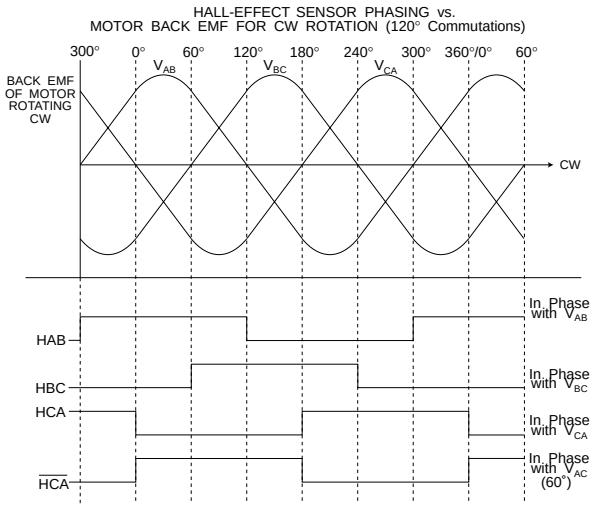


FIGURE 11. HALL PHASING

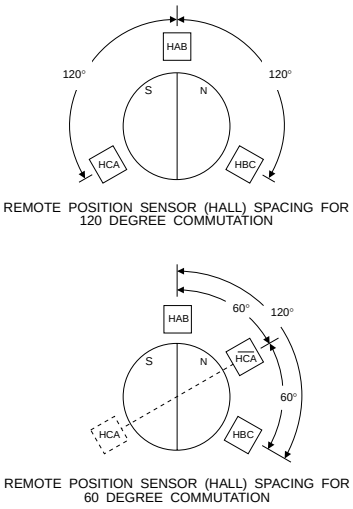
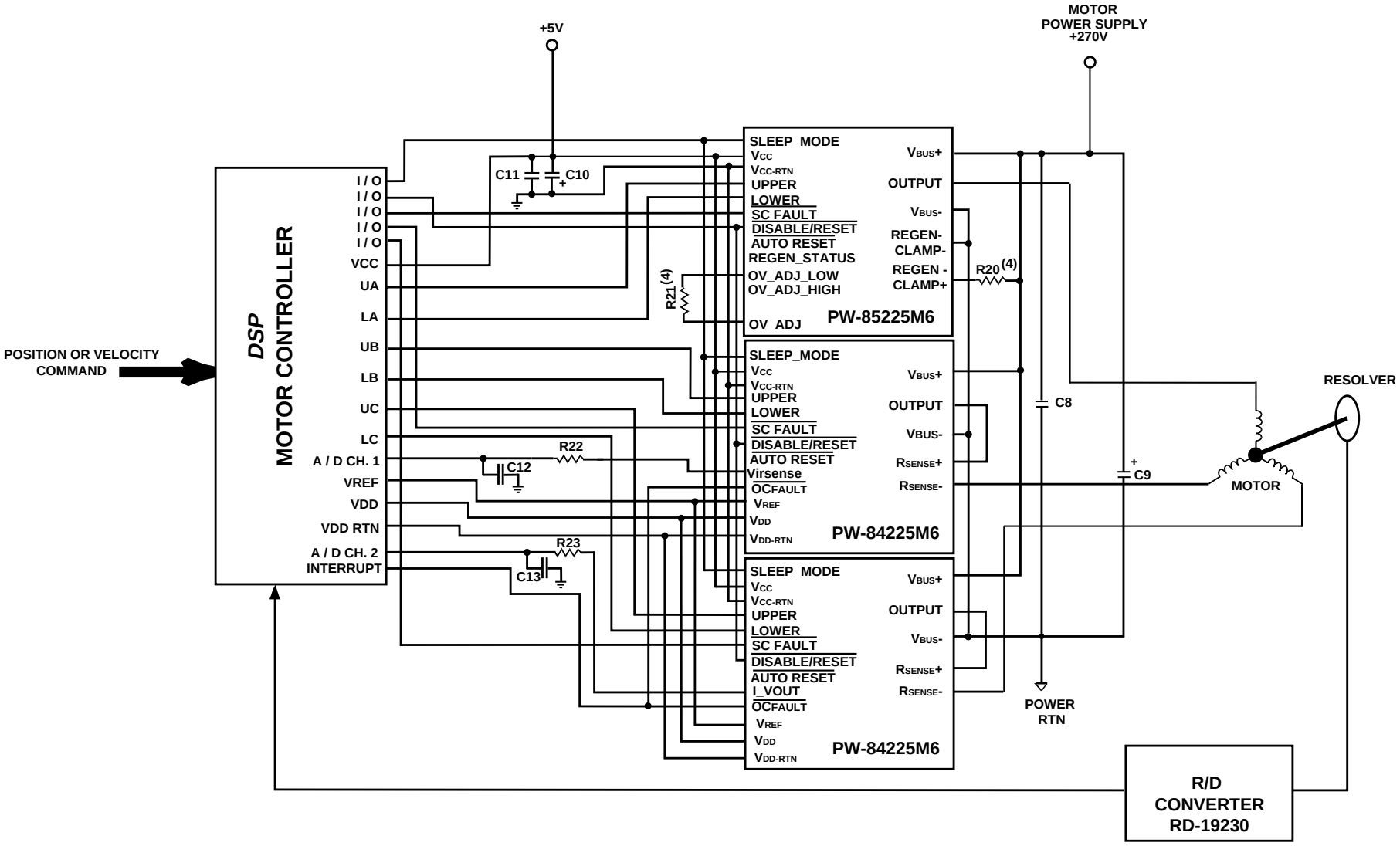
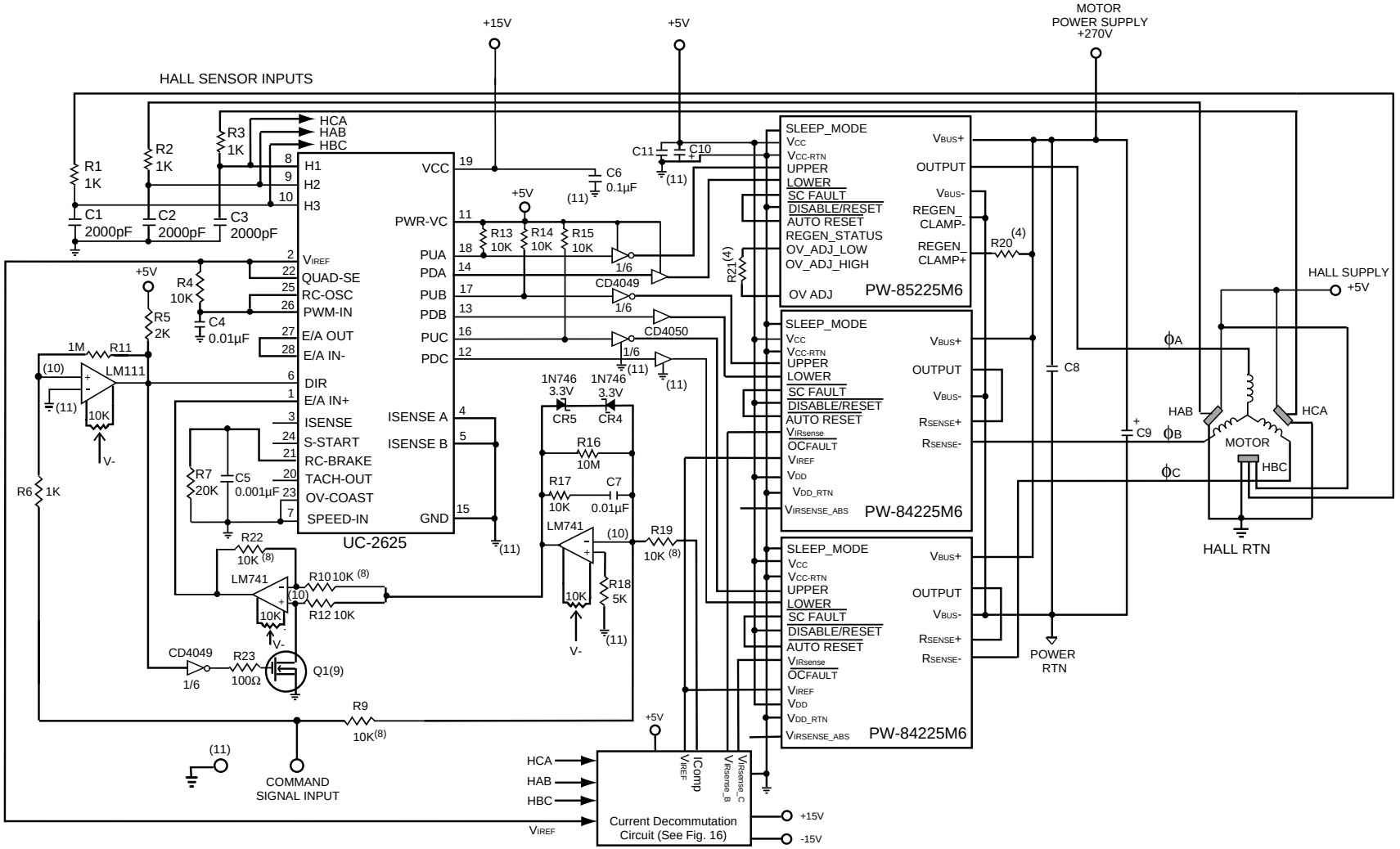


FIGURE 12. HALL SENSOR SPACING



NOTES:
1. C8 is a ceramic capacitor and should be selected per DDC Application Note AN/ H- 7, MAGNUM Motor Drive Power Supply Capacitor Selection.
2. C9 is an electrolytic capacitor and should be selected per DDC Application Note AN/ H- 7, MAGNUM Motor Drive Power Supply Capacitor Selection.
3. C10 is 22 µF, 15 V electrolytic capacitor. C11 is 0.1 µF, 50 V ceramic capacitor.
4. Resistance and power of R20 (Load dump resistor), and R21 (OV Adjust resistor) is application specific. (See OV_ADJ and REGEN_CLAMP descriptions for details)

FIGURE 13. PW- 8X225M6 POSITION OR VELOCITY HOOK- UP USING DSP MOTOR CONTROLLER



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2. C9 is an electrolytic capacitor and should be selected per DDC Application Note AN/ H- 7, MAGNUM Motor Drive Power Supply Capacitor Selection.
3. C10 is 22 µF, 15 V electrolytic capacitor. C11 is 0.1 µF, 50 V ceramic capacitor.
4. Resistance and power of R20 and R21 is application specific.
5. All resistors have a tolerance of ±10%, unless otherwise specified.
6. The CD4050 converts the +15V logic output of the UC- 2625 to +5V logic signals.
7. The CD4049 (or equivalent) inverts the upper signal from the UC- 2625.
8. 1% or better, depending on required accuracy.
9. Q 1 can be either IRML2402 or IRMU014 or IRLD014.
10. These high impedance inputs and summing junctions of the operational amplifiers are highly sensitive to noise.
11. These grounds should be closely tied together to reduce ground noise effect.
12. Connect Hall sensor inputs to motor shaft position sensors that are 120 electrical degrees apart. Motors with 60 electrical degree position sensor coding can be used if one or two of the position sensor signals are inverted.

FIGURE 14. PW- 8X225M6 TORQUE HOOK- UP USING UC- 2625 MOTOR CONTROLLER

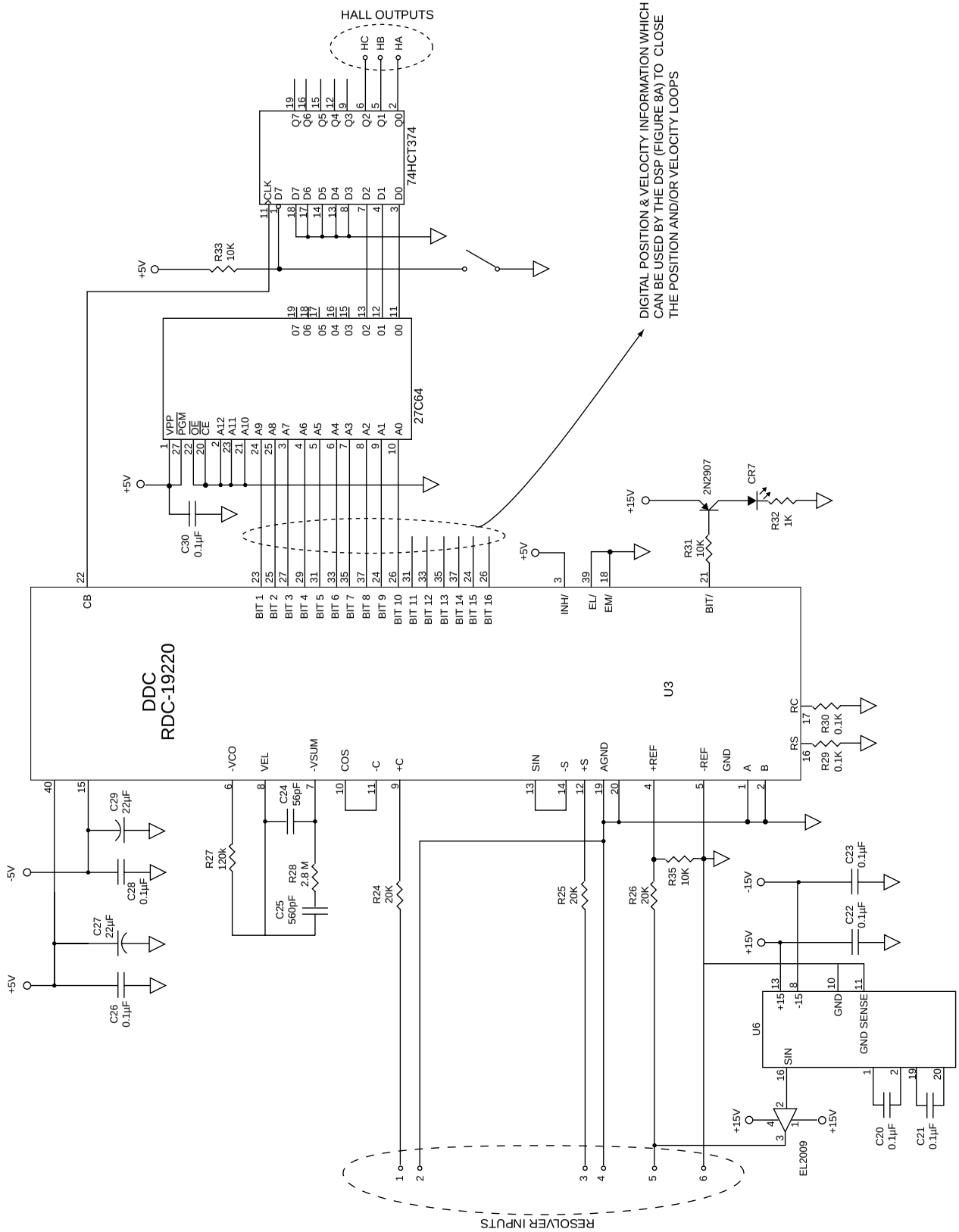

FIGURE 15. RESOLVER TO HALL SIGNAL CONVERSION CIRCUIT

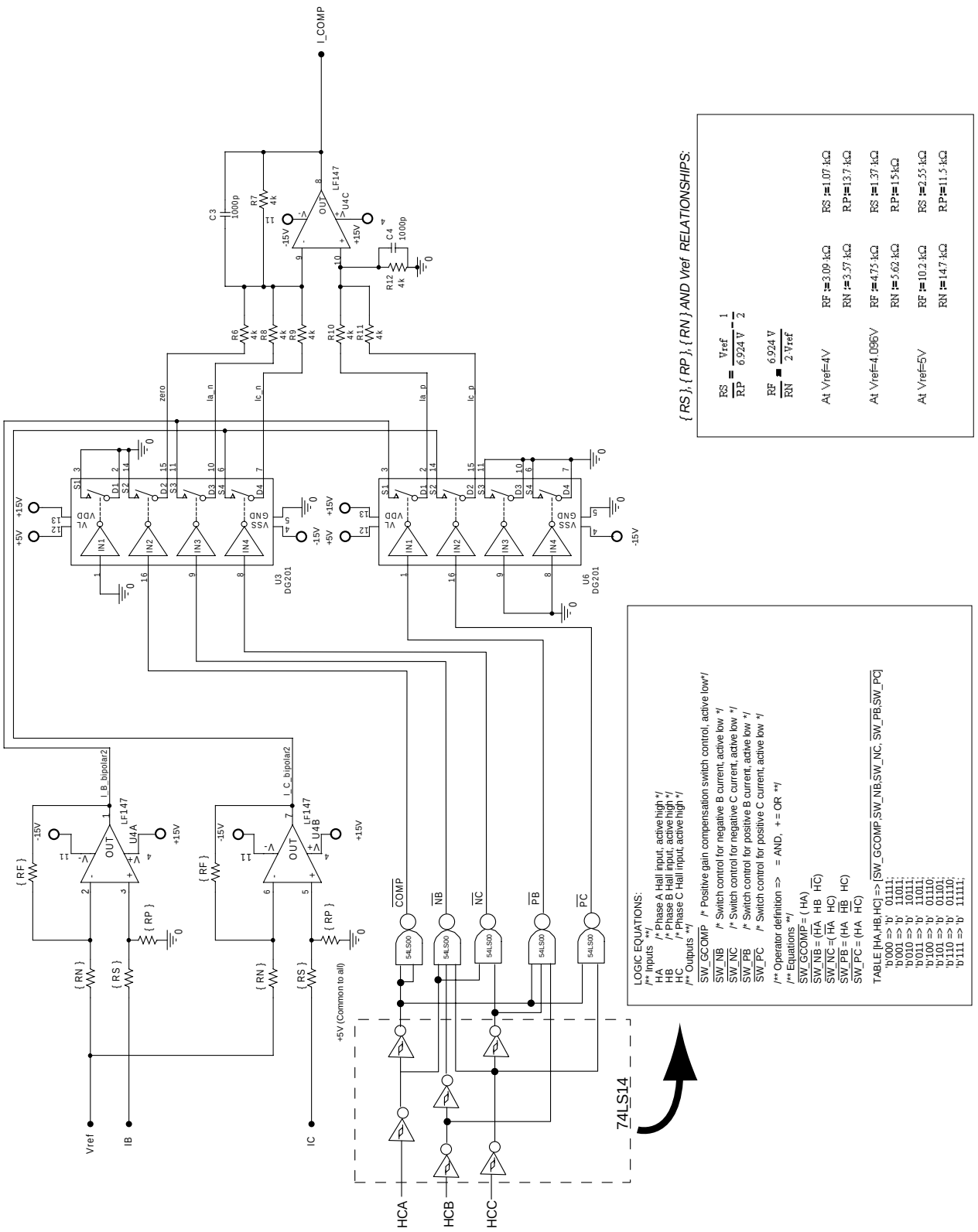

FIGURE 16. PW-8X225M6 CURRENT DECOMMUTATION CIRCUIT

TABLE 7. PIN ASSIGNMENTS			
PIN #	**PW-83225M6**	**PW-84225M6**	**PW-85225M6**
	CONTROL PINS		
1	SLEEP_MODE	SLEEP_MODE	SLEEP_MODE
2	TEST B *	TEST B *	TEST B *
3	TEST A *	TEST A *	TEST A *
4	VCC	VCC	VCC
5	VCC-RTN	VCC-RTN	VCC-RTN
6	N/C	N/C	N/C
7	$\overline{\text{SC FAULT}}$	$\overline{\text{SC FAULT}}$	$\overline{\text{SC FAULT}}$
8	N/C	N/C	N/C
9	N/C	N/C	REGEN_STATUS
10	N/C	N/C	0V_ADJ_HIGH
11	N/C	N/C	0V_ADJ
12	N/C	N/C	0V_ADJ_LOW
13	N/C	VIREF	N/C
14	TEST C *	TEST C *	TEST C *
15	$\overline{\text{AUTO RESET}}$	$\overline{\text{AUTO RESET}}$	$\overline{\text{AUTO RESET}}$
16	VCC	VCC	VCC
17	VCC-RTN	VCC-RTN	VCC-RTN
18	$\overline{\text{DISABLE/RESET}}$	$\overline{\text{DISABLE/RESET}}$	$\overline{\text{DISABLE/RESET}}$
19	LOWER	LOWER	LOWER
20	UPPER	UPPER	UPPER
21	N/C	VCC-RTN	N/C
22	N/C	VDD	N/C
23	N/C	VIRSENSE	N/C
24	N/C	VIRSENSE_ABS	N/C
25	N/C	$\overline{\text{OC FAULT}}$	N/C
	POWER PINS		
1	VBUS+	VBUS+	VBUS+
2	OUTPUT	OUTPUT	OUTPUT
3	VBUS-	VBUS-	VBUS-
4	N/A	RSENSE+	N/A
5	N/A	RSENSE-	REGEN_CLAMP

* Optional feature of PW-8X255M6-600 only

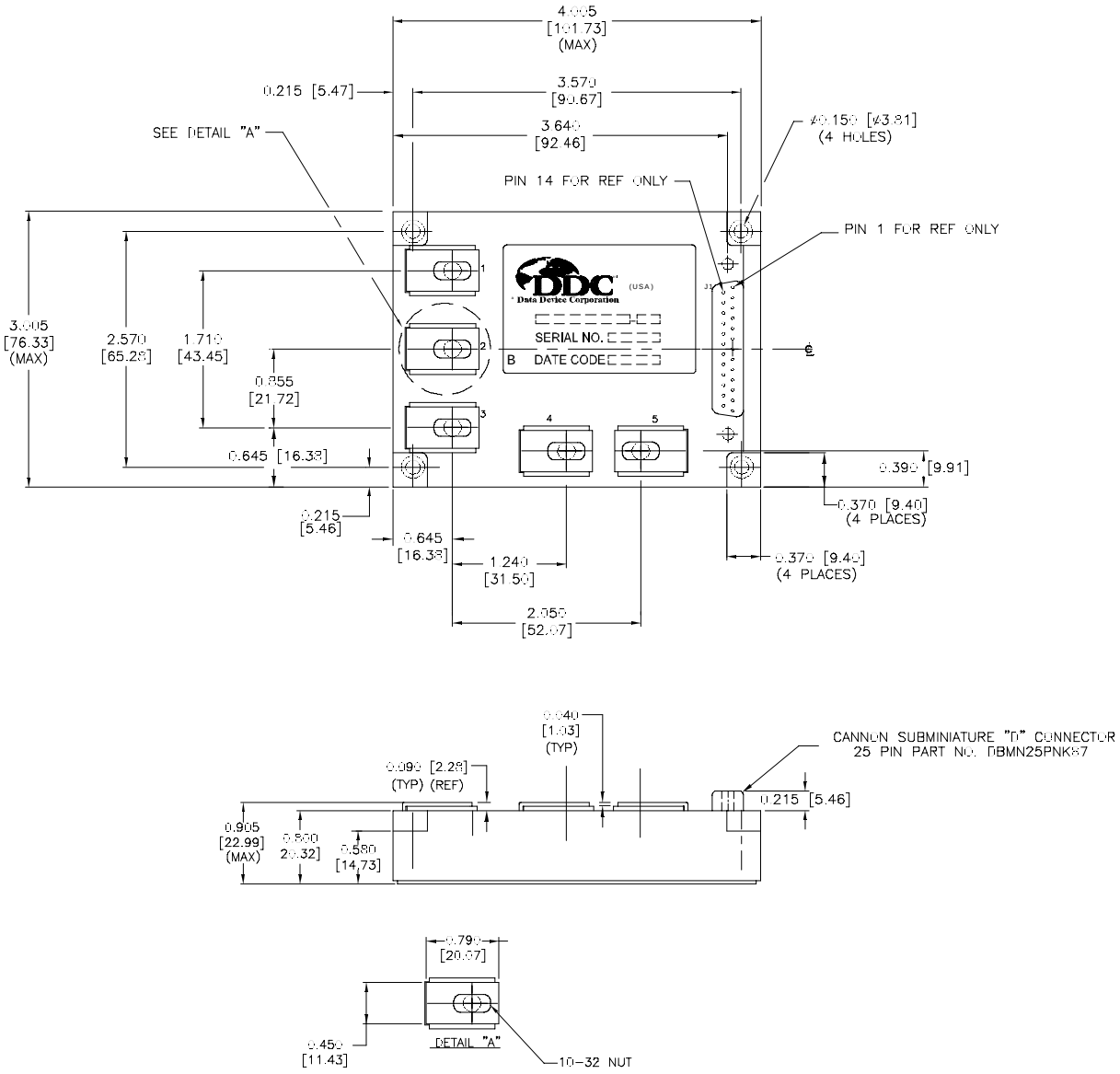

FIGURE 17. PW-8X225M6 MECHANICAL OUTLINE

ORDERING INFORMATION

PW - 8X225M6 - X X 0

Process Requirements
- 0 = Standard DDC Procedures no Burn-In
- 2 = High Reliability Processing with Burn-In

Temperature Grade/Data Requirements
- 1 = -55°C to +125°C
- 3 = -0°C to +70°C
- 4 = -55°C to +125°C with Variables Test Data
- 8 = 0°C to +70°C with Variables Test Data
- 9 = -55°C to 85°C

Voltage Rating
- 6 = 600V

Current Rating
- 225 = 225A

Features
- 3 = Standard ½ Bridge
- 4 = Standard ½ Bridge w/ current sense
- 5 = Standard ½ Bridge w/ regenerative voltage clamp

PW-8X225M6-600 High Reliability version (-55 to +125 degrees C) with individual transistor testability.

The information in this preliminary data sheet is believed to be accurate; however, no responsibility is assumed by Data Device Corporation for its use, and no license or rights are granted by implication or otherwise in connection therewith.
Specifications are subject to change without notice.

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