

NTMFS4108N

Power MOSFET

30 V, 35 A, Single N-Channel, SO-8 Flat Lead Package

Features

- Thermally and Electrically Enhanced Packaging Compatible with Standard SO-8 Package Footprint
- New Package Provides Capability of Inspection and Probe After Board Mounting
- Ultra Low $R_{DS(on)}$ (at 4.5 V_{GS}), Low Gate Resistance and Low Q_G
- Optimized for Low Side Synchronous Applications
- High Speed Switching Capability

Applications

- Notebook Computer Vcore Applications
- Network Applications
- DC-DC Converters

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating		Symbol	Value	Unit	
Drain-to-Source Voltage		V _{DSS}	30	V	
Gate-to-Source Voltage		V _{GS}	±20	V	
Continuous Drain Current (Note 1)	Steady State	T _A = 25°C	I _D	22	A
		T _A = 85°C		16	
	t ≤ 10 s	T _A = 25°C		35	
Power Dissipation (Note 1)	Steady State	T _A = 25°C	P _D	2.4	W
		t ≤ 10 s		6.25	
Continuous Drain Current (Note 2)	Steady State	T _A = 25°C	I _D	13.5	A
		T _A = 85°C		10	
Power Dissipation (Note 2)	Steady State	T _A = 25°C	P _D	0.91	W
Power Dissipation R _{θJC} (Note 1)		T _C = 25°C	P _D	100	
Pulsed Drain Current	t _p = 10 μs	I _{DM}	203	A	
Operating Junction and Storage Temperature		T _J , T _{stg}	-55 to 150	°C	
Continuous Source Current (Body Diode)		I _S	6.0	A	
Single Pulse Drain-to-Source Avalanche Energy (V _{DD} = 30 V, V _{GS} = 10 V, I _{PK} = 30 A, L = 1 mH, R _G = 25 Ω)		E _{AS}	450	mJ	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		T _L	260	°C	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

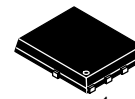
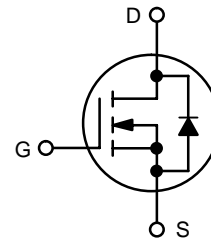
1. Surface-mounted on FR4 board using 1" sq. pad size (Cu area = 1.127" sq. [1 oz] including traces).
2. Surface-mounted on FR4 board using the minimum recommended pad size (Cu area = 0.412" sq.).



ON Semiconductor®

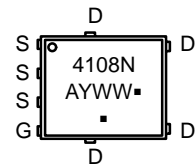
<http://onsemi.com>

V _{(BR)DSS}	R _{DS(on)} TYP	I _D MAX
30 V	1.8 mΩ @ 10 V	35 A
	2.7 mΩ @ 4.5 V	



SO-8 FLAT LEAD
CASE 488AA
STYLE 1

MARKING DIAGRAM



4108N = Specific Device Code
 A = Assembly Location
 Y = Year
 WW = Work Week
 ■ = Pb-Free Package
 (Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NTMFS4108NT1G	SO-8 FL (Pb-Free)	1500 Tape / Reel
NTMFS4108NT3G	SO-8 FL (Pb-Free)	5000 Tape / Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NTMFS4108N

THERMAL RESISTANCE RATINGS

Rating	Symbol	Max	Unit
Junction-to-Case (Drain)	$R_{\theta JC}$	1.25	°C/W
Junction-to-Ambient – Steady State (Note 3)	$R_{\theta JA}$	53	
Junction-to-Ambient – $t \leq 10$ s (Note 3)	$R_{\theta JA}$	20	
Junction-to-Ambient – Steady State (Note 4)	$R_{\theta JA}$	138	

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
----------------	--------	----------------	-----	-----	-----	------

OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0$ V, $I_D = 250$ μ A	30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			21		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0$ V, $V_{DS} = 24$ V	$T_J = 25^\circ\text{C}$		1.0	μ A
			$T_J = 125^\circ\text{C}$		25	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0$ V, $V_{GS} = 20$ V			100	nA

ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 250$ μ A	1.0		2.5	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			7.5		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 4.5$ V, $I_D = 19$ A		2.7	3.4	m Ω
		$V_{GS} = 10$ V, $I_D = 21$ A		1.8	2.2	
Forward Transconductance	g_{FS}	$V_{DS} = 15$ V, $I_D = 10$ A		25		S

CHARGES, CAPACITANCES AND GATE RESISTANCE

Input Capacitance	C_{ISS}	$V_{GS} = 0$ V, $f = 1.0$ MHz, $V_{DS} = 15$ V		6000		pF
Output Capacitance	C_{OSS}			1200		
Reverse Transfer Capacitance	C_{RSS}			700		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5$ V, $V_{DS} = 24$ V, $I_D = 21$ A		54		nC
Threshold Gate Charge	$Q_{G(TH)}$			11		
Gate-to-Source Charge	Q_{GS}			16		
Gate-to-Drain Charge	Q_{GD}			23		
Gate Resistance	R_G			0.7		

SWITCHING CHARACTERISTICS, $V_{GS} = 10$ V (Note 6)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 4.5$ V, $V_{DS} = 15$ V, $I_D = 1.0$ A, $R_G = 6.0$ Ω		45		ns
Rise Time	t_r			60		
Turn-Off Delay Time	$t_{d(OFF)}$			70		
Fall Time	t_f			140		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0$ V, $I_S = 6.0$ A	$T_J = 25^\circ\text{C}$		0.72	1.1	V
			$T_J = 125^\circ\text{C}$		0.65		
Reverse Recovery Time	t_{RR}	$V_{GS} = 0$ V, $dI_S/dt = 100$ A/ μ s, $I_S = 6.0$ A			41		ns
Charge Time	t_a				20		
Discharge Time	t_b				21		
Reverse Recovery Charge	Q_{RR}				45		

- Surface-mounted on FR4 board using 1" sq. pad size (Cu area = 1.127" sq. [1 oz] including traces).
- Surface-mounted on FR4 board using the minimum recommended pad size (Cu area = 0.412" sq.).
- Pulse Test: Pulse Width ≤ 300 μ s, Duty Cycle $\leq 2\%$.
- Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES

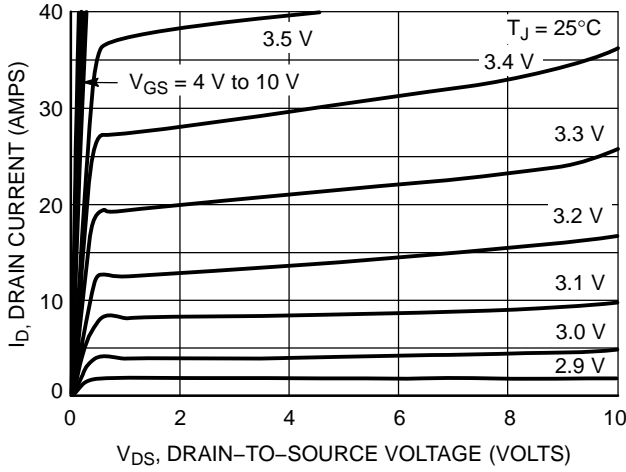


Figure 1. On-Region Characteristics

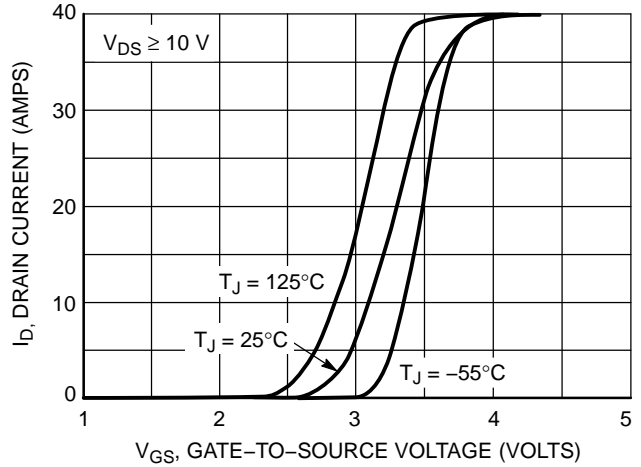


Figure 2. Transfer Characteristics

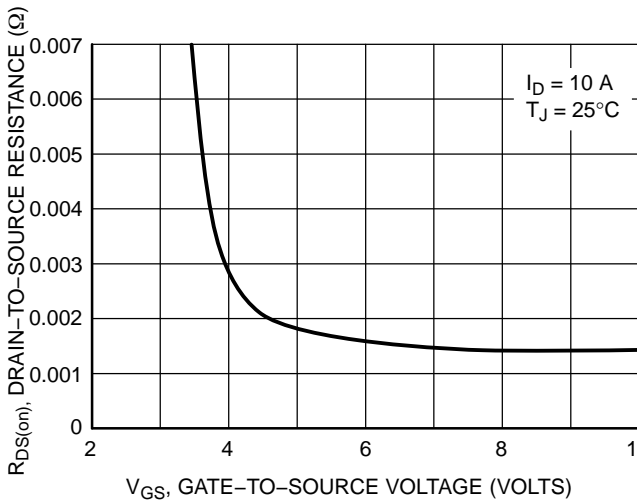


Figure 3. On-Resistance vs. Gate-to-Source Voltage

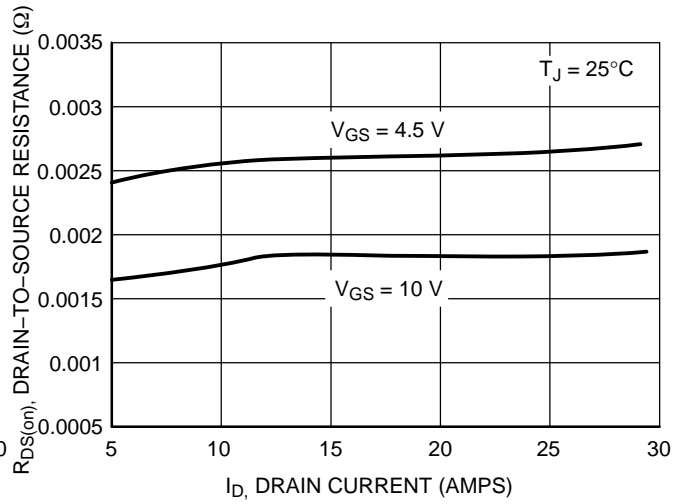


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

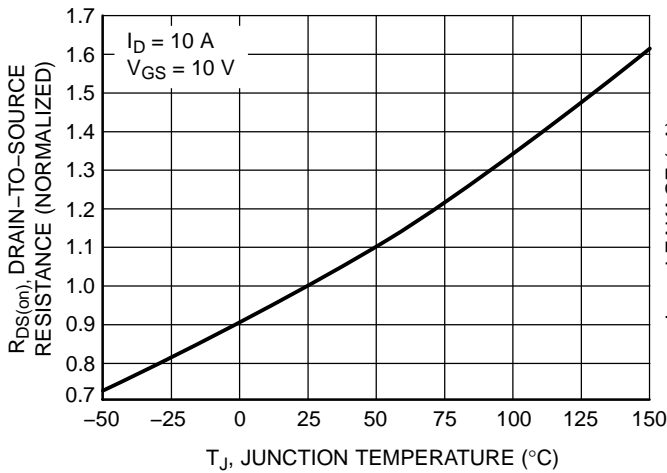


Figure 5. On-Resistance Variation with Temperature

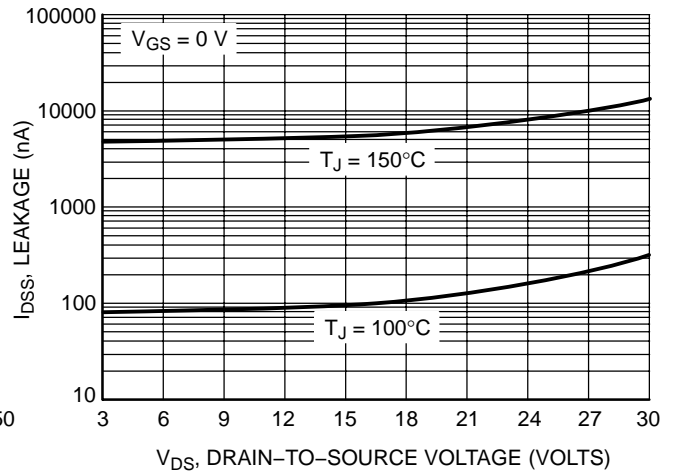


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL PERFORMANCE CURVES

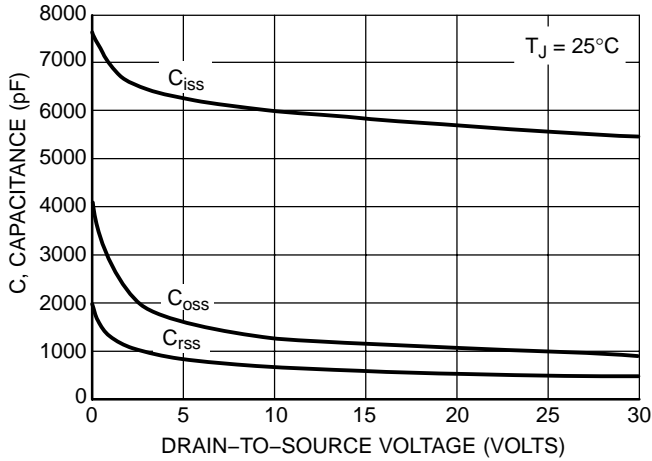


Figure 7. Capacitance Variation

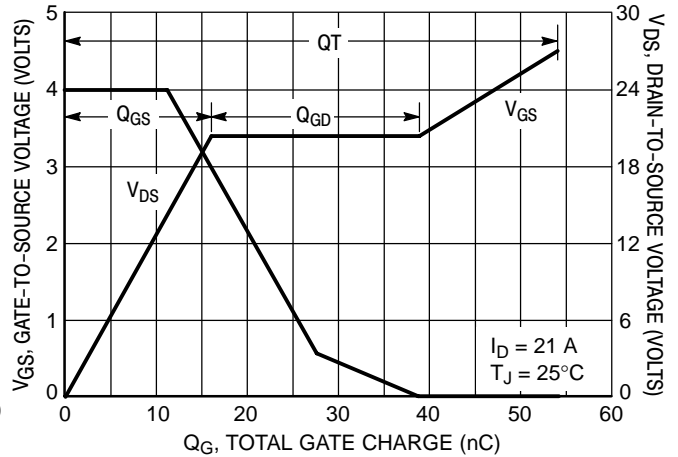


Figure 8. Gate-To-Source and Drain-To-Source Voltage vs. Total Charge

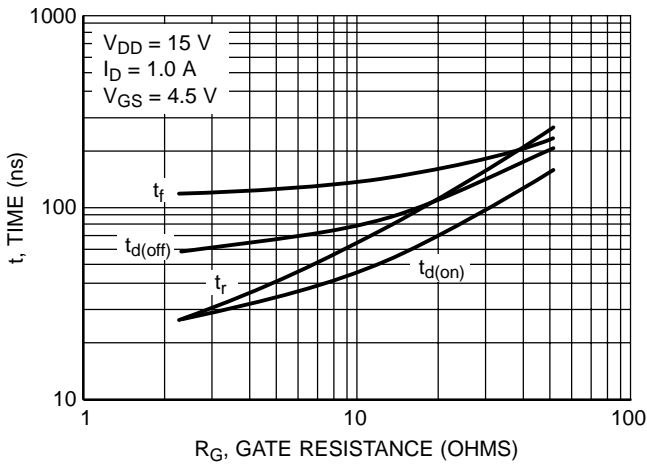


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

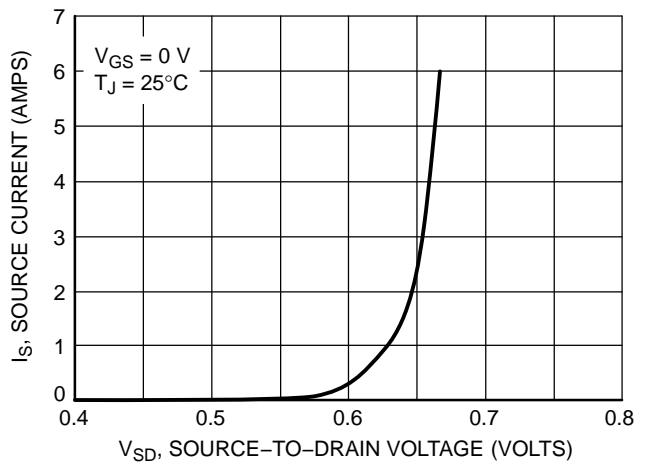


Figure 10. Diode Forward Voltage vs. Current

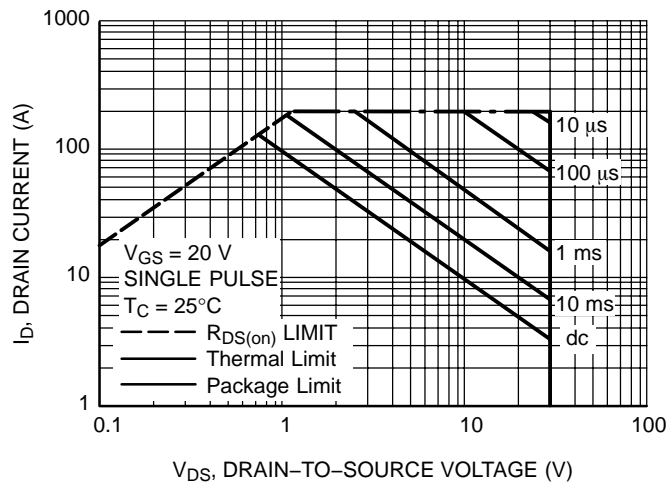
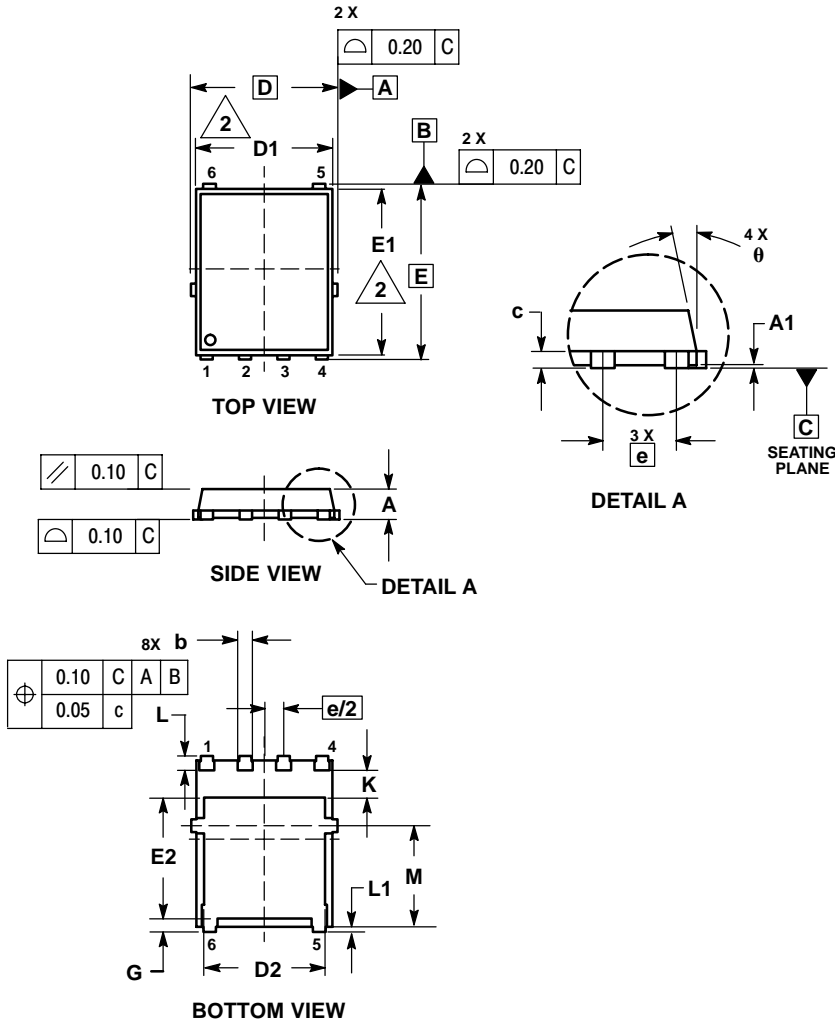


Figure 11. Maximum Rated Forward Biased Safe Operating Area

NTMFS4108N

PACKAGE DIMENSIONS

SO-8 FLAT LEAD (DFN6)
CASE 488AA-01
ISSUE B



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	0.99	1.20
A1	0.00	----	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.15 BSC		
D1	4.50	4.90	5.10
D2	3.50	----	4.22
E	6.15 BSC		
E1	5.50	5.80	6.10
E2	3.45	----	4.30
e	1.27 BSC		
G	0.51	0.61	0.71
K	0.51	----	----
L	0.51	0.61	0.71
L1	0.05	0.17	0.20
M	3.00	3.40	3.80
θ	0°	----	12°

STYLE 1:

1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN

NTMFS4108N

ON Semiconductor and **ON** are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
P.O. Box 61312, Phoenix, Arizona 85082-1312 USA
Phone: 480-829-7710 or 800-344-3860 Toll Free USA/Canada
Fax: 480-829-7709 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada

Japan: ON Semiconductor, Japan Customer Focus Center
2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051
Phone: 81-3-5773-3850

ON Semiconductor Website: <http://onsemi.com>

Order Literature: <http://www.onsemi.com/litorder>

For additional information, please contact your
local Sales Representative.

NTMFS4108N/D