Integrated Device Technology, Inc.

3.3V CMOS STATIC RAM 1 MEG (128K x 8-BIT) REVOLUTIONARY PINOUT

PRELIMINARY
IDT71V124

FEATURES:

- 128K x 8 advanced high-speed CMOS static RAM
- JEDEC revolutionary pinout (center power/GND) for reduced noise.
- Equal access and cycle times
  — Commercial: 12/15/20ns
- One Chip Select plus one Output Enable pin
- Bidirectional inputs and outputs directly TTL-compatible
- Low power consumption via chip deselect
- Available in Plastic32-pin 400 mil SOJ and 32-pin 400 mil TSOP Type II

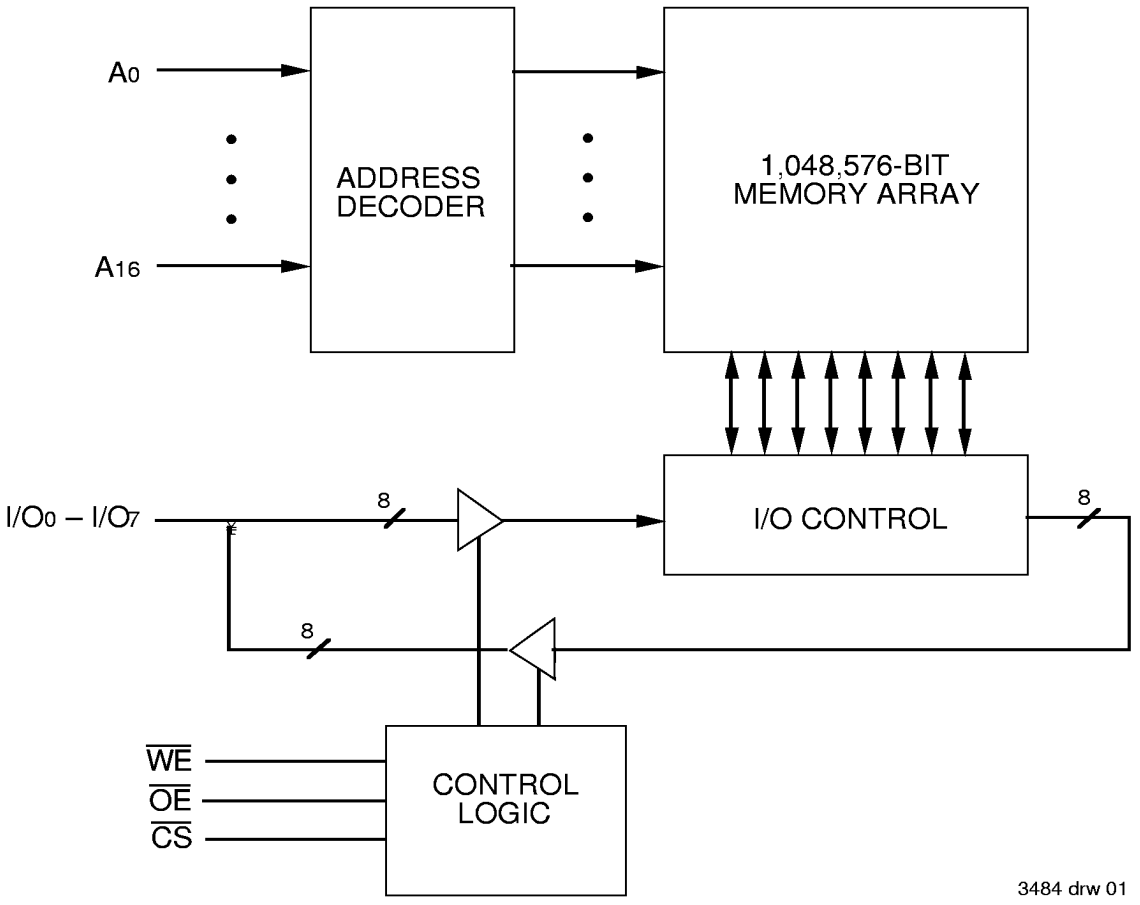
DESCRIPTION:

The IDT71V124 is a 1,048,576-bit high-speed static RAM organized as 128K x 8. It is fabricated using IDT's high-performance, high-reliability CMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective solution for high-speed memory needs. The JEDEC centerpower/GND pinout reduces noise generation and improves system performance.

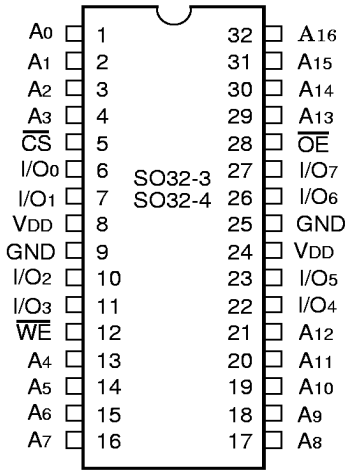
The IDT71V124 has an output enable pin which operates as fast as 6ns, with address access times as fast as 12ns available. All bidirectional inputs and outputs of the IDT71V124 are TTL-compatible and operation is from a single 3.3V supply. Fully static asynchronous circuitry is used; no clocks or refreshes are required for operation.

The IDT71V124 is packaged in Plastic 32-pin 400 mil SOJ and 32-pin 400 mil TSOP Type II.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



3484 drw 02

SOJ/TSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +4.1(2)	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–55 to +125	°C
P_T	Power Dissipation	1.25	W
I_{OUT}	DC Output Current	50	mA

NOTES: 3484 tbl 02
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliabilty.
2. V_{TERM} must not exceed VDD + 0.5V.

TRUTH TABLE(1,2)

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O	Function
L	L	H	$DATA_{OUT}$	Read Data
L	X	L	$DATA_{IN}$	Write Data
L	H	H	High-Z	Output Disabled
H	X	X	High-Z	Deselected - Standby (I_{SB})
V_{HC}(3)	X	X	High-Z	Deselected - Standby (I_{SB1})

NOTES: 3484 tbl 01
1. H = V_{IH}, L = V_{IL}, x = Don't care.
2. V_{LC} = 0.2V, V_{HC} = V_{DD} -0.2V.
3. Other inputs ≥V_{HC} or ≤V_{LC}.

CAPACITANCE

(T_A = +25°C, f = 1.0MHz, SOJ package)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	8	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 3dV	8	pF

NOTE: 3484 tbl 03
1. This parameter is guaranteed by device characterization, but is not production tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	3.0	3.3	3.6	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.0	—	VDD+0.3	V
V_{IL}	Input Low Voltage	–0.3(1)	—	0.8	V

NOTE: 3484 tbl 04
1. V_{IL} (min.) = –1V for pulse width less than 5ns, once per cycle.

DC ELECTRICAL CHARACTERISTICS

V_{DD} = 3.3V ± 10%

Symbol	Parameter	Test Condition	IDT71V124 Min.	IDT71V124 Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{DD} = Max., V_{IN} = GND to V_{DD}	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	V_{DD} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{DD}	—	5	µA
V_{OL}	Output LOW Voltage	I_{OL} = 8mA, V_{DD} = Min.	—	0.4	V
V_{OH}	Output HIGH Voltage	I_{OH} = –8mA, V_{DD} = Min.	2.4	—	V

3484 tbl 05

DC ELECTRICAL CHARACTERISTICS(1)

(V_{DD} = 3.3V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{DD} – 0.2V)

Symbol	Parameter	71V124S12(3)		71V124S15		71V124S20		Unit
		Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I_{CC}	Dynamic Operating Current and $\overline{CS} \le V_{IL}$, Outputs Open, V_{DD} = Max., f = f_{MAX}(2)	105	—	100	—	95	—	mA
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS} \ge V_{IH}$, Outputs Open, V_{DD} = Max., f = f_{MAX}(2)	20	—	20	—	20	—	mA
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS} \ge V_{HC}$, Outputs Open, V_{DD} = Max., f = 0(2), $V_{IN} \le V_{LC}$ or $V_{IN} \ge V_{HC}$	5	—	5	—	5	—	mA

NOTES:
3484 tbl 06

1. All values are maximum guaranteed values.
2. f_{MAX} = 1/t_{RC} (all address inputs are cycling at f_{MAX}); f = 0 means no address input lines are changing.
3. 12ns specification is preliminary.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

3484 tbl 07

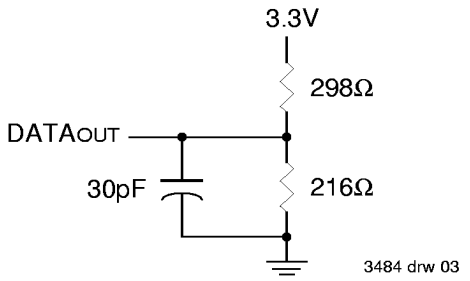
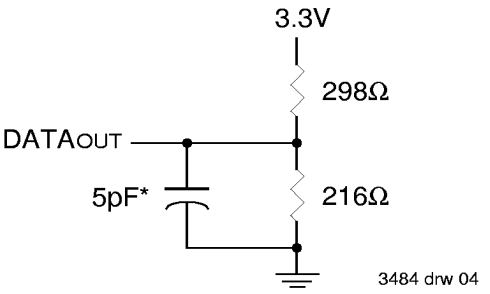


Figure 1. AC Test Load



*Including jig and scope capacitance.

Figure 2. AC Test Load
(for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{OW}, and t_{WHZ})

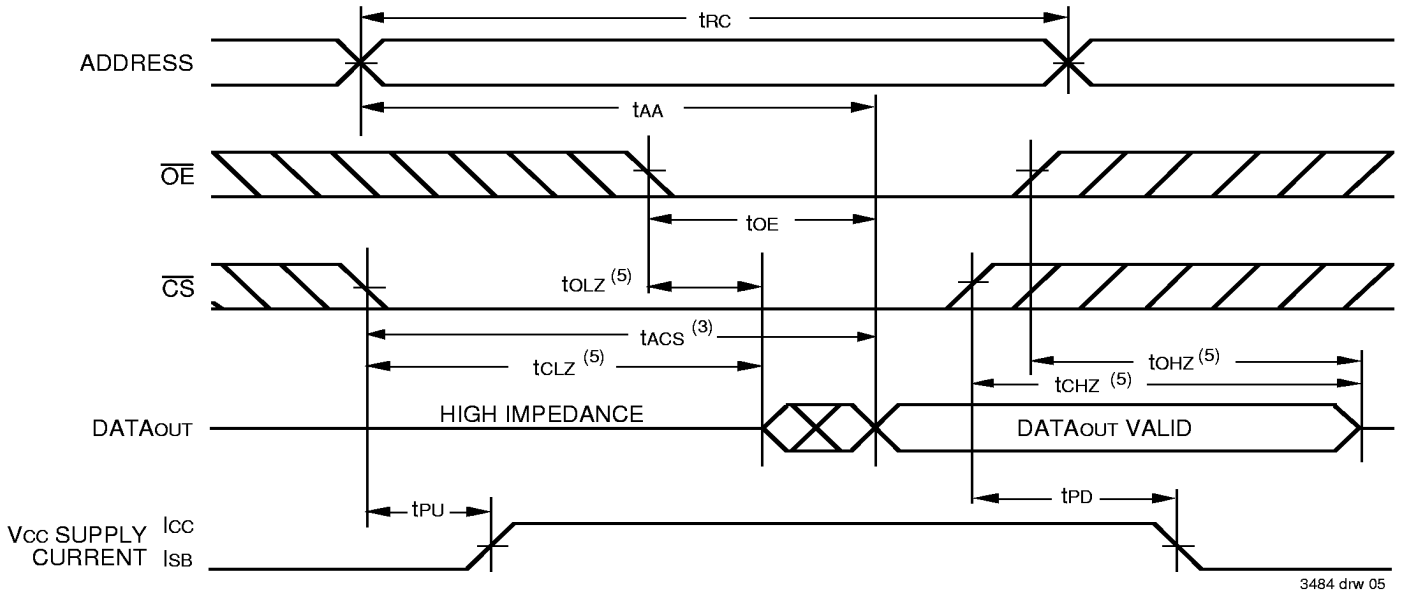
AC ELECTRICAL CHARACTERISTICS (V_{DD} = 3.3V ± 10%, Commercial Range)

Symbol	Parameter	71V124S12[3] Min.	71V124S12[3] Max.	71V124S15 Min.	71V124S15 Max.	71V124S20 Min.	71V124S20 Max.	Unit
Read Cycle								
t_{RC}	Read Cycle Time	12	—	15	—	20	—	ns
t_{AA}	Address Access Time	—	12	—	15	—	20	ns
t_{ACS}	Chip Select Access Time	—	12	—	15	—	20	ns
t_{CLZ}[2]	Chip Select to Output in Low-Z	3	—	3	—	3	—	ns
t_{CHZ}[2]	Chip Deselect to Output in High-Z	0	6	0	7	0	8	ns
t_{OE}	Output Enable to Output Valid	—	6	—	7	—	8	ns
t_{OLZ}[2]	Output Enable to Output in Low-Z	0	—	0	—	0	—	ns
t_{OHZ}[2]	Output Disable to Output in High-Z	0	5	0	5	0	7	ns
t_{OH}	Output Hold from Address Change	4	—	4	—	4	—	ns
t_{PU}[2]	Chip Select to Power-Up Time	0	—	0	—	0	—	ns
t_{PD}[2]	Chip Deselect to Power-Down Time	—	12	—	15	—	20	ns
Write Cycle								
t_{WC}	Write Cycle Time	12	—	15	—	20	—	ns
t_{AW}	Address Valid to End-of-Write	10	—	12	—	15	—	ns
t_{CW}	Chip Select to End-of-Write	10	—	12	—	15	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	10	—	12	—	15	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End-of-Write	7	—	8	—	9	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	ns
t_{OW}[2]	Output Active from End-of-Write	3	—	3	—	4	—	ns
t_{WHZ}[2]	Write Enable to Output in High-Z	0	5	0	5	0	8	ns

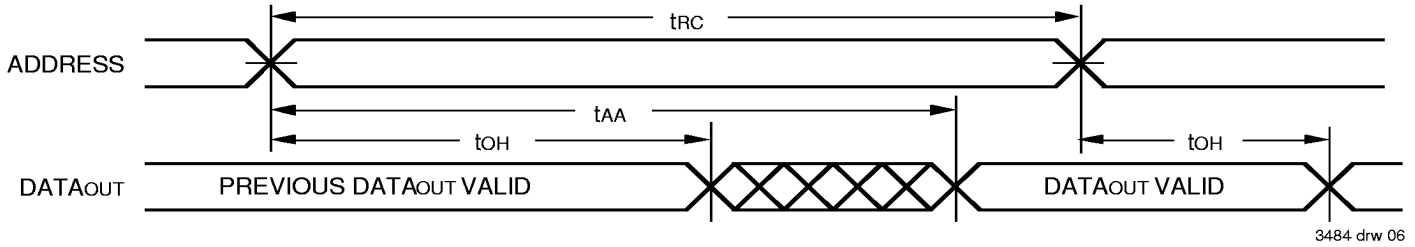
NOTES:
3484 tbl 08

1. 0°C to +70°C temperature range only.
2. This parameter guaranteed with the AC load (Figure 2) by device characterization, but is not production tested.
3. 12ns specification is preliminary.

TIMING WAVEFORM OF READ CYCLE NO. 1(1)

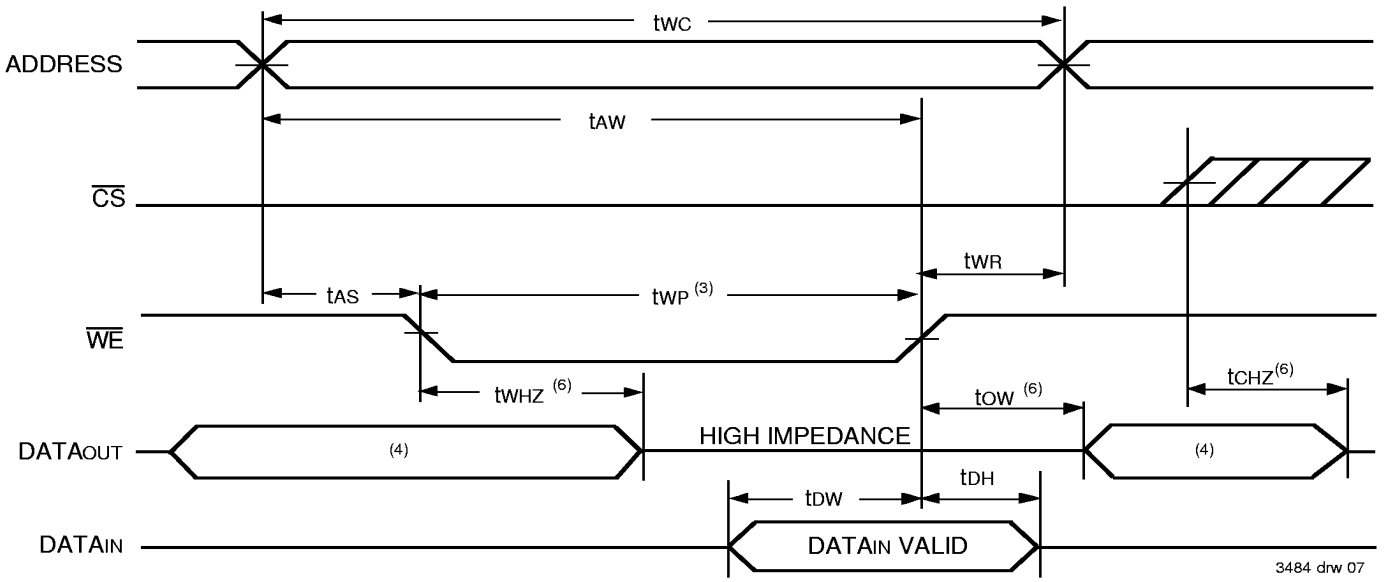


TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)

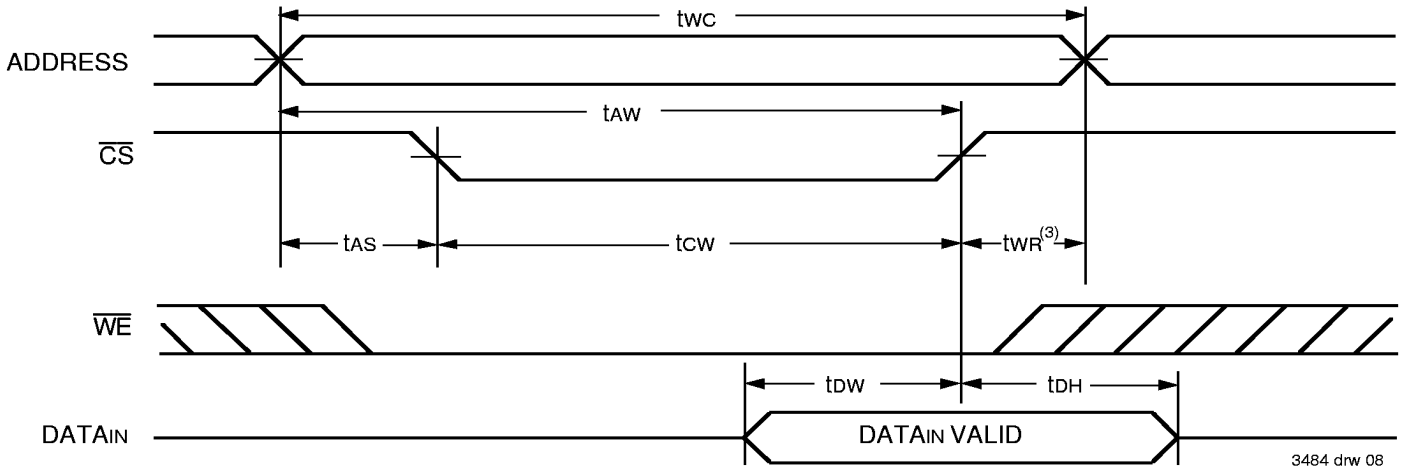


NOTES:
1. $\overline{WE}$ is HIGH for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ is LOW.
3. Address must be valid prior to or coincident with the later of $\overline{CS}$ transition LOW; otherwise t_{AA} is the limiting parameter.
4. $\overline{OE}$ is LOW.
5. Transition is measured ±200mV from steady state.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 5, 7)



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 5)



NOTES:
1. $\overline{WE}$ must be HIGH, $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. $\overline{OE}$ is continuously HIGH. During a $\overline{WE}$ controlled write cycle with $\overline{OE}$ LOW, t_{WP} must be greater than or equal to $t_{WHZ} + t_{DW}$ to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the minimum write pulse is the specified t_{WP}.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high impedance state. $\overline{CS}$ must be active during the t_{CW} write period.
6. Transition is measured ±200mV from steady state.

ORDERING INFORMATION