ADC-817A, ADC-827A Fast 12-Bit A/D Converters

FEATURES

- **12-Bit resolution**
- **2 Microseconds or 3 microseconds conversion times**
- **Unipolar and bipolar operation**
- **6 Programmable input ranges**
- **Parallel data output**

GENERAL DESCRIPTION

The ADC-817A and ADC-827A are high-speed two-pass A/D converters in miniature hybrid from using thick-and thin-film hybrid technology. Both models have identical specifications except for conversion times. The ADC-827 has a maximum conversion time of 3.0 microseconds, while the ADC-817A accomplishes a 12-bit conversion in only 2.0 microseconds, maximum.

These converters feature six analog input voltage ranges: 0 to -5V dc, 0 to -10V dc, 0 to -20V dc, ±2.5V dc, ±5V dc, and ±10V dc. Selection of input range is accomplished by simple external pin connection. Both devices provide a user-selectable, fast settling precision input buffer with input impedance of 100MΩ, allowing them to be driven directly from a high impedance source. The input buffer may be bypassed.

Output data is coded as straight binary for unipolar operation and as either offset binary or two's complement for bipolar operation.

Specifications shared by both models include maximum nonlinearity of ±1 LSB maximum and a gain tempco of 25 ppm/ °C maximum.

These converters are functionally complete units requiring a minimum of passive external components for operation. Each unit is composed of a fast settling precision input buffer, an ultrafast settling D/A converter, a precision voltage reference, clock generator and control logic circuits. The combination of unique design and the latest hybrid fabrication technology allows this level of performance to be achieved in a minature, hermetically sealed 32-pin ceramic DIP package.

Both models require ±15V dc and +5V supplies, and are available in versions for the 0 to 70 °C or -55 to +125 °C operating temperature ranges.

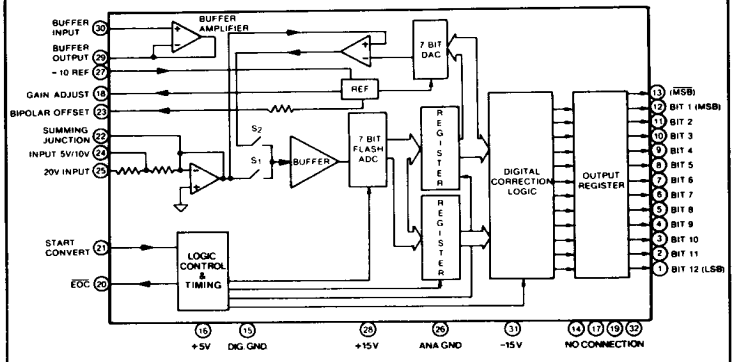
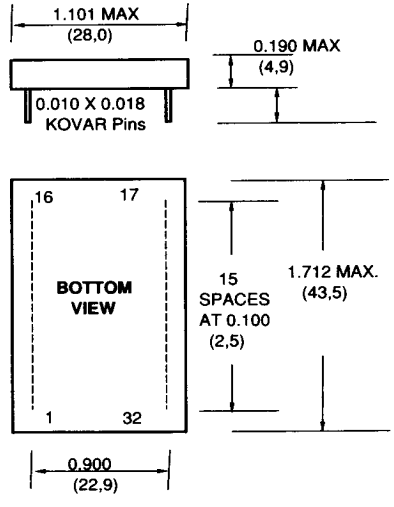


Figure 1. ADC-817A,-827A Simplified Block Diagram

MECHANICAL DIMENSIONS INCHES (mm)



NOTE: Pins have a 0.025 inch, ±0.01 stand-off from case.

I/O CONNECTIONS

PIN	FUNCTION
1	BIT 12 OUT (LBS)
2	BIT 11 OUT
3	BIT 10 OUT
4	BIT 9 OUT
5	BIT 8 OUT
6	BIT 7 OUT
7	BIT 6 OUT
8	BIT 5 OUT
9	BIT 4 OUT
10	BIT 3 OUT
11	BIT 2 OUT
12	BIT 1 OUT (MSB)
13	BIT 1 OUT (MSB)
14	NO CONNECTION
15	DIGITAL GROUND
16	+5V POWER
17	NO CONNECTION
18	REFERENCE OUTPUT
19	NO CONNECTION
20	EOC OUTPUT
21	START CONVERSION
22	SUMMING JUNCTION
23	BIPOLAR OFFSET
24	5/10V INPUT RANGE
25	20V INPUT RANGE
26	ANALOG GROUND
27	REFERENCE INPUT
28	+15V POWER
29	BUFFER OUTPUT
30	BUFFER INPUT
31	-15V POWER
32	NO CONNECTION

ABSOLUTE MAXIMUM RATINGS

Positive Supply	+18V
Negative Supply	-18V
Logic Supply	+7V
Digital Inputs	+5.5V
Analog Inputs	±20V
Buffer Amplifier Input	±15V

FUNCTIONAL SPECIFICATIONS

Typical at 25 °C, ±15V supplies, unless otherwise noted.

INPUTS

Analog Input Ranges Unipolar	0 to -5V, 0 to -10V, 0 to -20V
Bipolar	±2.5Vm ±5V, ±10V
Input Impedance	
5V/10V Ranges	1.05 KΩ
20V Range	4Ω
Start Conversion	2V min. to 5.5V max. positive pulse with duration of 50 nsec. min. Rise and fall times <30 nsec. Logic "1" to "0" transition initiates next conversion.
Logic Levels:	
Logic "1"	2.4V min.
Logic "0"	0.4V max.
Logic Loading:	
Logic"1"	-160 µA max.
Logic "0"	6.4 mA max.
Buffer Amplifier Gain	±1
Buffer Amplifier Input Voltage	±10.0V
Buffer Amplifier Input Impedance	100 MΩ
Buffer Amplifier Settling Time[1]	500 nsec. max.

OUTPUTS

Parallel Output Data	13 parallel lines (12 binary bits plus MSB) valid from negative going edge of EOC pulse to positive going edge of START CONVERSION pulse. Vout "0" ≤ +0.4V Vout "1" ≥ +2.4V Loading: 4 TTL loads
Coding:	
Unipolar[2]	Straight Binary
Bipolar[3]	Offset Binary, Two's Complement[3]
End of Conversion (EOC)	Conversion Status Signal: 4 TTL Loads Vout "0" ≤ +0.4V for conversion complete Vout "1" ≤ +2.4V for conversion in progress

PERFORMANCE

Resolution	12 binary bits[4]
Nonlinearity, max	±1 LSB
Differential Nonlinearity, max	±1LSB
Temp. Coeff. of Gain, max[4]	±25 ppm/ °C of FSR
Temp. Coeff. of Zero, unipolar max.	±150 µV/ °C of FSR
Temp. Coeff. of bipolar, zero error, max.[4]	±15 ppm of FSR/ °C[6]
Diff. Nonlinearity Tempco, max	±5 ppm/ °C of FSR
Power Supply Rejection	±0.01%/% Supply max.
Conversion Time Over Full Temp	2.0 µsec. max., ADC-817A 3.0 µsec. max., ADC-827A

POWER REQUIREMENTS

Supply Voltage	+15V dc ±0.5V at +70 mA max. -15V dc ±0.5V at -50 mA max. +5V dc ±0.25V at +65 mA max.
Power Dissipation	2.2 W max.

PHYSICAL/ENVIRONMENTAL

Operating Temp. Range,	
MC	0 °C to +70 °C
MM	-55 °C to +125 °C
Storage Temp. Range	-65 °C to +150 °C
Package Type	32 pin hermetically sealed ceramic DIP
Pins	0.010 x 0.018 inch Kovar
Weight	0.5 ounce (14 grams)

FOOTNOTES

1. 10V step to 0.01%, 5V and 20V steps settle to 0.01% in 150 nanoseconds and 800 nanoseconds, respectively.
2. These converters operate with inverted analog, that is F.S. +1 LSB is encoded as 1111 1111 1111 and +FS is encoded as 0000 0000 0000 (examples given are for offset binary coding).
3. Parallel output data only is available in offset binary (uses MSB out) or two's complement coding (uses MSB out).
4. For 0°C to +70°C operation, these values double outside of this temperature range.
5. FSR is Full Scale Range.

TECHNICAL NOTES

1. The high operating speed of these converters requires that good high frequency board layout techniques be used. Capacitance from long leads on the data outputs can prevent the internal DAC from turning on in time, creating linearity errors. Leads from data outputs should be kept as short as possible, output leads longer than 1 inch (2.5 cm) require the use of an output register. Ground loop problems are avoided by connecting all grounds on the board to the ground plane. Analog and digital grounds are connected internally.

2. Analog input leads should be as short and direct as possible. The use of shielded cable as an analog input lead will ensure isolation of analog signals from environmental interference.

3. The ADC-817A/827A provides an internal buffer amplifier. Use of this buffer provides an input impedance greater than 100 MΩ, allowing the A/D to be driven from a high impedance source or directly from an analog multiplexer. When using the input buffer, a delay equal to its setting time must be allowed between input level change and the negative going edge of the start conversion pulse. If the buffer is not required, its input should be connected to analog ground to avoid introducing noise in to the converter.

4. Both analog and digital supplies should be bypassed to ground with 1 µF electrolytic capacitors in parallel with 0.1 µF ceramic capacitors as shown in the connections diagrams. Bypass capacitors should be located directly

adjacent to, or on, each supply pin. The -10V reference output (pin 18) should be bypassed to ground with a 2.2 µF electrolytic capacitor mounted as previously indicated.

5. In the bipolar mode, two's complement output coding is available by using the MSB output (pin 13); offset binary coding is obtained by using the MSB output (pin 12). Unipolar operation requires use of the MSB output (pin 12) to achieve straight binary output coding.

6. Applications of these converters that require the use of a sample-hold may be satisfied by DATEL's model SHM-45 or SHM-4860 featuring 200 nanosecond acquisition time and 0.01% accuracy. The SHM-45 offers gains of -1 or -2.

7. These converters have a maximum power dissipation of 2.2W. The case-to-ambient thermal resistance for this package is approximately 28°C per watt. For operation in ambient temperatures exceeding +70°C, care must be taken to ensure free air circulation in the vicinity of the converter.

NOTE

In any application using the ADC-817A or the ADC-827A, signal integrity and noise isolation are a function of grounding. The suggested ground plane shown should be used whenever possible.

1

GROUND PLANE LAYOUT

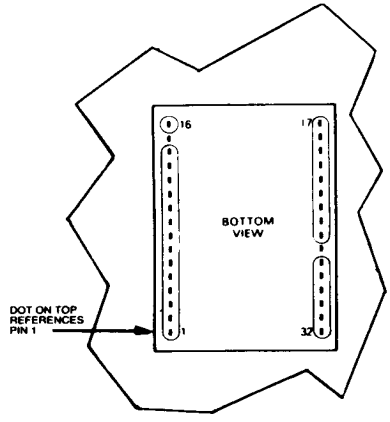


Figure 3. Ground Plane Layout

TIMING DIAGRAM
OPERATING PERIODS

ADC-817A	ADC-827A
T1 2.0 µSEC.	3.0 µSEC.

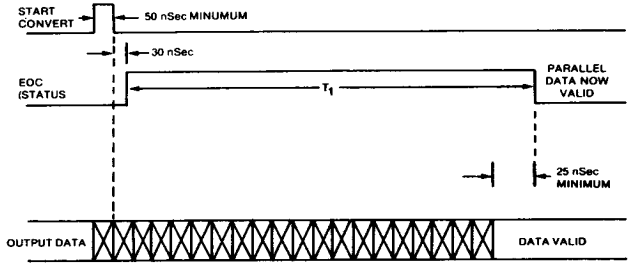


Figure 2. Timing Diagram for ADC-817A, ADC-827A

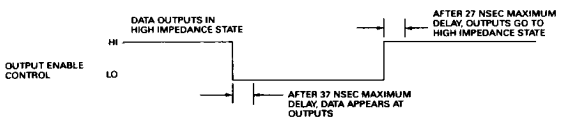
OUTPUT CODING

UNIPOLAR SCALE	UNIPOLAR ANALOG INPUT -20V RANGE	-10V RANGE	-5V RANGE	STRAIGHT BINARY OUTPUT CODE
-FS + 1 LSB	-19.9952V	-9.9976V	-4.9988V	1111 1111 1111
-7/8 FS	-17.5000V	-8.7500V	-4.3750V	1110 0000 0000
-3/4 FS	-15.0000V	-7.5000V	-3.7500V	1100 0000 0000
-1/2 FS	-10.0000V	-5.0000V	-2.5000V	1000 0000 0000
-1/4 FS	-5.0000V	-2.5000V	-1.2500V	0100 0000 0000
-1 LSB	-0.0049V	-0.0024V	-0.0012V	0000 0000 0001
0	-0.0000V	-0.0000V	-0.0000V	0000 0000 0000

BIPOLAR SCALE	ANALOG INPUT ±10V RANGE	±5V RANGE	±2.5V RANGE	DATA OUTPUT CODING OFFSET BINARY	TWO's COMPLEMENT
-FS + 1 LSB	-9.9951V	-4.9976V	-2.4988V	1111 1111 1111	0111 1111 1111
-1/2 FS	-5.0000V	-2.5000V	-1.2500V	1100 0000 0000	0100 0000 0000
-1 LSB	-0.0049V	-0.0024V	-0.0012V	1000 0000 0001	0000 0000 0001
0	0.0000V	0.0000V	0.0000V	1000 0000 0000	0000 0000 0000
+1 LSB	+0.0049V	+0.0024V	+0.0012V	0111 1111 1111	1111 1111 1111
+1/2 FS	+5.0000V	+2.5000V	+1.2500V	0100 0000 0000	1100 0000 0000
+FS -1 LSB	+9.9951V	+4.9976V	+2.4988V	0000 0000 0001	1000 0000 0001
+FS	+10.0000V	+5.0000V	+2.5000V	0000 0000 0000	1000 0000 0000

Providing Three-State Outputs

For applications where the converted input must interface to tri-state TTL or CMOS logic, the ADC-817A OR ADC-827A outputs are easily converted using buffers such as the DM8095's shown in the diagram. Signal length must be less than one inch between devices to ensure signal integrity. Also note that two's complement outputs are available from the ADC-817A and ADC-827A by using pin 13 instead of pin 12 as the MSB output. The timing diagram shows the delays incurred as the signal passes through the buffers.



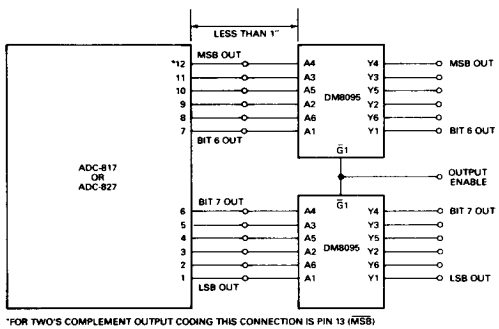
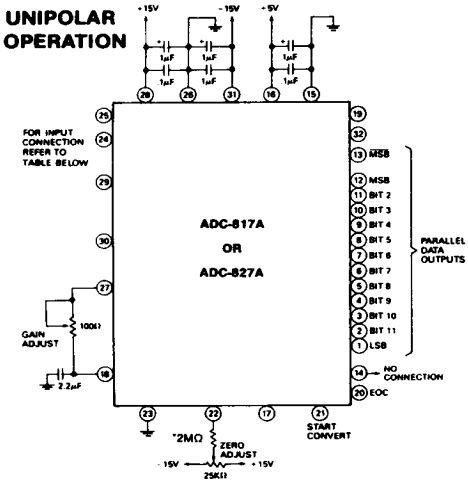


Figure 4. High Speed Three-State Output Buffer

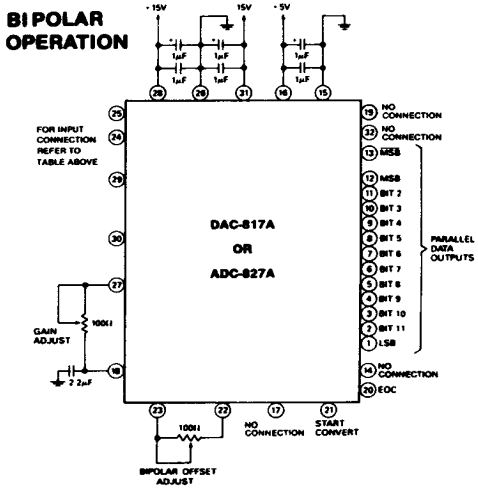
TYPICAL CONNECTIONS

UNIPOLAR OPERATION



*FOR GREATER UNIPOLAR ZERO GAIN ADJUSTMENT THE 2 MEG OHM RESISTOR MAY BE REDUCED TO A VALUE OF 500 KΩ

BIPOLAR OPERATION



CALIBRATION PROCEDURE

1. Connect the converter as shown in the applicable connections diagram. A trigger pulse of 50 nanoseconds minimum is applied to the start conversion input (pin 21) at a rate of 200 kHz.

2. **Zero and Offset Adjustments**

   Apply a precision voltage reference source between the appropriate input for the selected full scale range and ground. Adjust the output of the reference source to the value shown in the Calibration Table for the unipolar zero adjustment (0 -1/2 LSB) or the bipolar offset adjustment (+FS -1/2 LSB). Adjust the appropriate trimming potentiometer so that the output code flickers equally between X000 0000 0000 and X000 0000 0001. The MSB, indicated by X, will be 0 for straight binary and offset binary output coding, or 1 for two's complement output coding.

3. **Full Scale Adjustment**

   Set the output of the voltage reference source used in step 2 to the value shown in the Calibration Table for the unipolar or bipolar gain adjustment (-FS +1 1/2 LSB). Adjust the gain trimming potentiometer so that the output code flickers equally between X1111 1111 1111 and X111 1111 1110. The MSB, indicated by X, will be 1 for straight binary and offset binary output coding, or 0 for two's complement output coding.

CALIBRATION TABLE

UNIPOLAR RANGE	ADJUST	INPUT VOLTAGE
0 TO -5V	ZERO GAIN	-0.6 mV -4.9982V
0 TO -10V	ZERO GAIN	-1.2mV -9.9963V
0 TO -20V	ZERO GAIN	-2.44mV -19.9925V
BIPOLAR RANGE		
±2.5V	OFFSET GAIN	+2.4994V -2.4982V
±5V	OFFSET GAIN	+4.9988V -4.9963V
±10V	OFFSET GAIN	+9.9976V -9.9927V

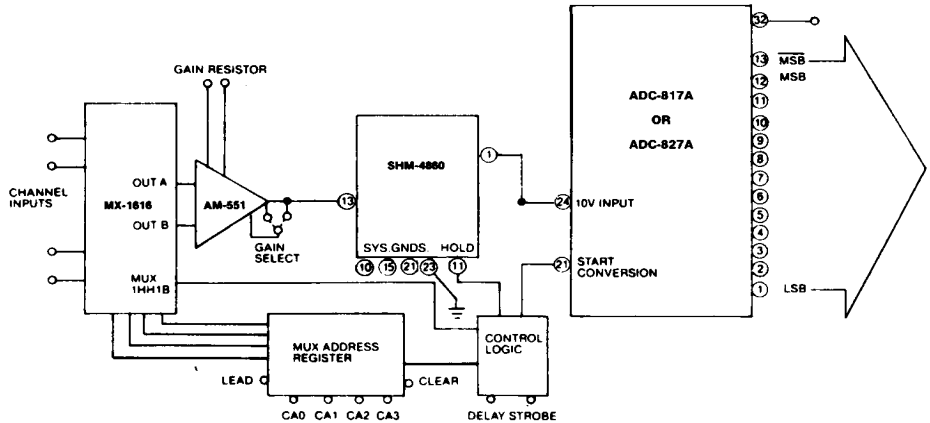


Figure 5. High Speed Data Acquisition System

The ADC-817A/827A configured as shown with DATEL's MX-1616, a high speed CMOS multiplexer, AM-551, a hybrid precision programmable gain instrumentation amplifier, and SHM-4860, a 200 nanosecond, 0.01% hybrid sample hold forms an 8-channel (differential), 12-bit, hight speed data acquisition system capable of throughput rates of 200 kHz.

INPUT CONNECTIONS

INPUT VOLTAGE RANGE	*WITH INPUT BUFFER			WITHOUT INPUT BUFFER		
	INPUT PIN	CONNECT THESE PINS TOGETHER		INPUT PIN	CONNECT THESE PINS TOGETHER	
0 to -5V	30	29 to 24	22 to 25	24	22 to 25	30 to 26
0 to -10V	30	29 to 24	–	24	–	30 to 26
±2.5V	30	29 to 24	22 to 25	24	22 to 25	30 to 26
±5V	30	29 to 24	–	24	–	30 to 26
±10V	30	29 to 25	–	25	–	30 to 26

ORDERING INFORMATION

MODEL	TEMP. RANGE
ADC-817A MC	0 °C to +70 °C
ADC-817A MM	-55 °C to +125 °C
ADC-827A MC	0 °C to +70 °C
ADC-827A MM	-55 °C to +125 °C

ACCESSORIES

Part Number	Description
TP25K or TP100K	Trimming Potentiometers

For military devices compliant to MIL-STD-883, consult the factory.