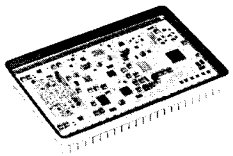
ADC-00113

12 BIT 10 MHz T/H + A/D HYBRID HIGH SPEED, SMALL SIZE, MIL-SPEC



DESCRIPTION

The ADC-00113 is a 12 bit, 10 MHz track/hold and A/D converter hybrid packaged in a 46 pin plug-in. Pin-for-pin compatible with the ADC603.

Containing T/H, A/D converter, data registers, tri-state output buffers, and timing circuits, the ADC-00113 is the fastest and smallest digitizer of its kind. The ADC-00113 operates over a temperature range of -55°C to +125°C and military processing is available.

The ADC-00113 is implemented with a 2-step A/D conversion algorithm. A number of factors contributed to achieving the ADC-00113's technical breakthroughs in speed and size. Foremost among them are proprietary ICs for the DAC, the conversion logic, and the gain amp functions. In addition, judicious use of thin-film and thick-film hybrid technology resulted in minimum layout area.

With its high speed, small package and wide operating temperature range, the ADC-00113 is ideal for the most demanding military and industrial data conversion applications. Typical of these applications are radar and IR digitizing, vibration and FFT analysis, medical and nuclear instrumentation, and high-speed data acquisition and communications systems.

FEATURES

- ***Improved Pin-For-Pin ADC603***
- ***Includes***
  - ***Track/Hold***
  - ***A/D Converter***
  - ***Tri-State Output Registers***
  - ***Timing Circuits***
- ***10 MHz Word Rate***
- ***Small 46 Pin Plug-In Hermetic Hybrid***
- ***Input Voltage Options***
- ***-55°C TO +125°C Operating Temperature***

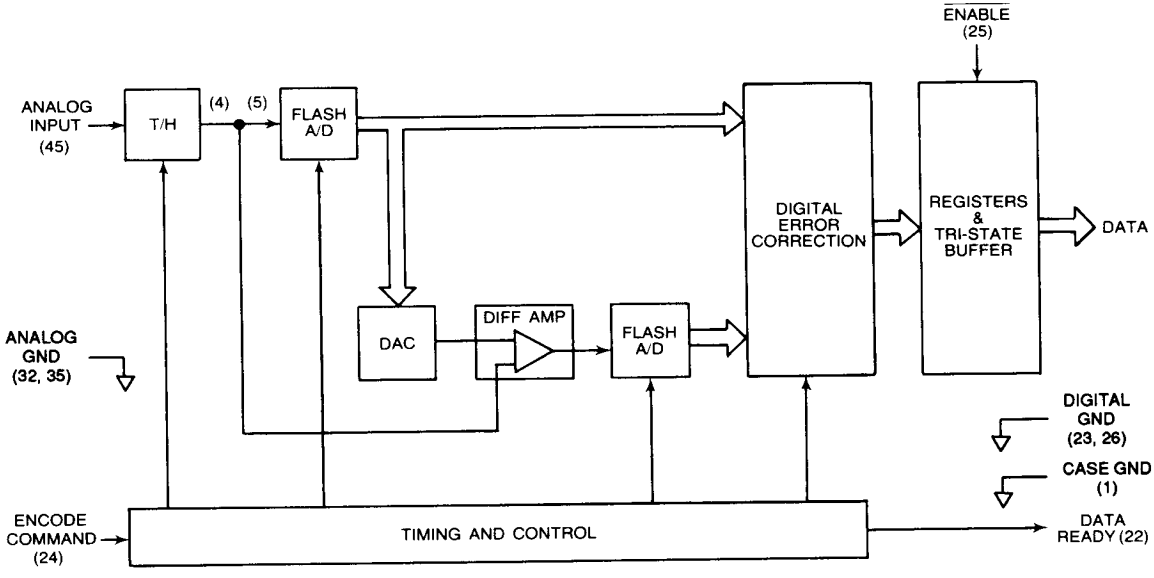


FIGURE 1. ADC-00113 BLOCK DIAGRAM

TABLE 1. ADC-00113 SPECIFICATIONS (T/H and A/D)

Typical values at listed temperature range, nominal power supply voltages, 10 MHz encode rate, and 15 minute warmup, unless otherwise noted.

PARAMETER	UNITS	VALUES FOR: ADC-00113-1XX at 25°C			ADC-00113-1XX at −55 to +125°C			ADC-00113-3XX at 25°C			ADC-00113-3XX at 0 to +70°C			CONDITIONS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TEMPERATURE RANGE	°C		25		−55		+125		25		0	25	+70	T_{case}
RESOLUTION	Bits		12			12			12			12		
ACCURACY														
Linearity Error	LSB		0.75			0.75			0.75			0.75		F = 200Hz
Diff Linearity Error														
■ 68.3% of all codes	LSB		0.3			0.4			0.3			0.4		F = 200Hz
■ 99.7% of all codes	LSB		0.4			0.5			0.4			0.5		F = 200Hz
■ 100% of all codes	LSB		0.5			0.75			0.5			0.75		F = 200Hz
Gain Error	%FSR(1)		±0.2	±2		±0.4	±2		±0.2	1.0		±0.4	1.5	F = 200Hz
Offset Error	%FSR		±0.2	±2		±0.4	±2		±0.2	0.75		±0.4	1.0	dc
No Missing Codes		Guaranteed												
DYNAMIC CHARACTERISTICS														
Conversion Rate	MHz	dc		10	dc		10	dc		10	dc		10	Fixed
Pipeline Delay(2)		3 Encode Commands												Fixed
Aperture Uncertainty (Jitter)	psec rms		9			10			9			10		
Aperture Time (Delay)	nsec		−5			−6			−5			−6		
Signal-to-Noise Ratio(3)	(SNR)													
■ 5MHz analog input	dB	64	67		64	67		64	67		64	67		F_S = 9.99MHz
■ 1MHz analog input	dB	65	67.5		65	67.5		65	67.5		65	67.5		F_S = 9.99MHz
■ 100kHz analog input	dB	66	68		66	68		66	68		66	68		F_S = 9.99MHz
Transient Response(4)	nsec		100			100			100			100		See note 4.
Overvoltage Recovery(5)	nsec		80			80			80			80		2x full-scale input
Input Bandwidth														
■ Small Signal, 3dB(6)	MHz		70			70			70			70		
■ Large Signal, 3dB(7)	MHz		40			40			40			40		
Total Harmonic Distortion														
■ 5MHz analog input	dB		−68	−64		−67	−60		−68	−64		−67	−64	F_S = 9.99MHz
■ 100kHz analog input	dB		−70	−66		−69	−64		−70	−66		−69	−66	F_S = 9.99MHz
Two-tone linearity														
■ 2.20MHz	dB		−75	−67		−72	−68		−75	−67		−72	−68	F_S = 8.006MHz
■ 2.50MHz	dB		−75	−67		−72	−68		−75	−67		−72	−68	F_S = 8.006MHz
ANALOG INPUT														
Voltage Range	V	−1.25		+1.25	−1.25		+1.25	−1.25		+1.25	−1.25		+1.25	Full scale
Impedance														
■ Resistance	MΩ		0.15			0.15			0.15			0.15		
■ Capacitance	pF		5			5			5			5		
ENCODE COMMAND INPUT(8)														
Logic Levels	V	TTL Compatible												t = Encode Command Period
Pulse Width	nsec	10		t-20	10		t-20	10		t-20	10		t-20	
DIGITAL OUTPUT														
Format	Bits	12 parallel; NRZ												
Logic Levels	V	TTL Compatible												
Time Skew	nsec	5	35		5	35		5	35		5	35		
Coding		Two's complement and inverted two's complement												
Drive	TTL Loads		3			3			3			3		

A

TABLE 1. ADC-00113 SPECIFICATIONS (T/H and A/D) (continued)

Typical values at listed temperature range, nominal power supply voltages, 10 MHz encode rate, and 15 minute warmup, unless otherwise noted.

PARAMETER	UNITS	VALUES FOR: ADC-00113-1XX at 25°C			ADC-00113-1XX at −55 to +125°C			ADC-00113-3XX at 25°C			ADC-00113-3XX at 0 to +70°C			CONDITIONS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLIES														
+15 Volt Supply	V	+14.25	+15	+15.75	+14.25	+15	+15.75	+14.25	+15	+15.75	+14.25	+15	+15.75	
■ Current Drain	mA		+ 40			+40			+40			+ 40		
−15 Volt Supply	V	−14.25	−15	−15.75	−14.25	−15	−15.75	−14.25	−15	−15.75	−14.25	−15	−15.75	
■ Current Drain	mA		−40			−40			−40			− 40		
+5 Volt Supply	V	+ 4.75	+5	+5.25	+4.75	+5	+5.25	+4.75	+5	+5.25	+ 4.75	+5	+5.25	
■ Current Drain	mA		+320			+320			+320			+320		
− 5.2 Volt Supply	V	− 4.95	− 5.2	− 5.46	− 4.95	− 5.2	− 5.46	− 4.95	− 5.2	− 5.46	− 4.95	− 5.2	− 5.46	
■ Current Drain	mA		−620			−620			−620			−620		
Power Dissipation	W		6.1			6.1			6.1			6.1		
PSRR:														
±15V Supplies	%FSR/%V_S		0.01			0.01			0.01			0.01		
+ 5V and -5.2V Supplies	%FSR/%V_S		0.03			0.03			0.03			0.03		

Notes:

(1) FSR: Full-Scale Range = 2.5V_{p-p}; F = input frequency; F_S = sampling Frequency.
(2) Measured from the rising edge of Encode Command to the falling edge of Data Ready; use rising edge to strobe output data into external circuits. See figure 2, timing diagram.
(3) Rms signal to rms noise ratio.
(4) For full-scale step input, 12-bit accuracy attained in specified time.
(5) Recovers to 12-bit accuracy in specified time after 2 x FS input overvoltage.
(6) With analog input 40 dB below FS.
(7) With F_S analog input (Large-signal bandwidth flat within 0.2dB,dc to 5MHz).
(8) Transition from digital 0 to digital 1 initiates encoding.

GENERAL DESCRIPTION

Figure 1 is a functional block diagram of the ADC-00113 sampling A/D converter. Its major elements are a track/hold amplifier, 6-bit and 8-bit flash A/D converters, a 6-bit D/A converter, and a differential amplifier. The remaining functions are timing and control circuits, digital buffers, and registers.

These components implement a straightforward 2-step A/D conversion algorithm. First, the conversion cycle is initiated with the receipt of an Encode Command. This causes the timing circuit to place the track/hold in the HOLD mode, storing the voltage at its analog input. The flash A/D then generates a coarse encode of the sampled voltage. Its 6-bit coarse encode output is stored temporarily in the MSB register. At the same time, the coarse 6-bit word is input to the DAC, which converts it to an analog voltage.

The differential amplifier subtracts the voltage representing the coarse encode from the sampled input, and scales it up to the correct full scale range.

Next, the 8-bit flash A/D converter generates a fine encode of the scaled difference voltage. The fine encode 8-bit word is stored in the LSB register. Finally, the contents of the 6-bit MSB and 8-bit LSB registers are combined in the digital error correction circuit to yield a 12-bit output word. This 12-bit word is stored in the output registers. The encoded digital output is available upon application of an Enable signal to the tri-state output buffer.

Since the ADC-00113 has output storage registers, its digital output is available to the user at all times, except for a short interval when it is being updated. A Data Ready output signal is provided to indicate when the digital output is valid.

Care must be taken when designing with the ADC-00113, to achieve its rated performance. This high-speed sampling A/D converter generates high-frequency power supply and ground currents. For this reason, it is recommended that decoupling capacitors be used on each power supply line. See the paragraph on Power Supply Decoupling for more detail. High-frequency layout considerations should be kept in mind when designing a printed circuit board for the ADC-00113. Conductor lengths should be kept to a minimum, and a large area ground plane should be used to keep ground impedances as low as possible.

TIMING DIAGRAM

A Typical ADC-00113 timing diagram is shown in figure 2. Note that the Encode Command repeats at 100 nsec intervals with a throughput (pipeline) delay of 280 nsec.

A conversion cycle is initiated by the application of a positive pulse (15 nsec min) to the Encode Command pin. The rising edge of the Encode Command starts the timing cycle. First the internal track/hold is placed in the HOLD mode. The output signal is then

delivered to the 6-bit flash A/D converter for a coarse conversion of the 6 MSBs The output of the 6-bit flash A/D is also delivered to the D/A whose output is applied to the differential amplifier. The output of the differential amplifier is then delivered to the 8-bit flash A/D converter. Once the 8-bit flash conversion is complete, the internal T/H is returned to the TRACK mode. The output of the 8-bit flash A/D converter along with the original coarse 6-bit word is input to the digital error correction circuit with output to the 12-bit register. The Encode Command input then updates the register to take data.

The idea behind pipelining is that a second Encode is started before the first Encode has completed conversion. Consequently, the input signal is encoded and output data is delivered at a 10MHz rate. The pipeline delay is two Encode periods plus 80 nsec, or 280 nsec, minimum. Since Data Ready stays low for 50 nsec, it is possible to use the Encode Command to enable and continuously take data at a 10M Hz rate, though output data lags analog input by two encode periods plus 80 nsec. Note that data is not valid during the first 5 nsec following the falling edge of Data Ready, but is otherwise valid. The timing diagram also indicates the tri-state propagation delays for both enabling and disabling the latch as 8 nsec typ, and 10 nsec max.

LAYOUT PRECAUTIONS

The ADC-00113 high-speed sampling A/D converter generates high-frequency power supply and ground currents, and is sensitive to coupled signals. High-frequency layout considerations must therefore be kept in mind when designing a printed circuit board for it. All conductor lengths must be kept to a minimum, and a large area ground plane must be used to keep ground impedances as low as possible. Analog inputs and digital outputs must be kept separated from each other to minimize crosstalk. Input and output circuits must be kept as close to the A/D converter package as possible. Likewise, the three analog ground pins must be connected to the digital ground pin as close as possible to the hybrid package, with connection to the case ground pin. While the case ground pin may be left floating it is recommended that the case be tied to system ground in order to minimize ground contributions to noise.

OUTPUT CODING

Output coding is illustrated in table 2. The ADC-00113 is TTL compatible and outputs two's complement data and inverted two's complement. Two's complement coding occurs when a LOW state TTL input is applied to pin 27, Output Logic Invert; application of a HIGH state TTL input results in inverted two's complement output data. Moreover, data is accessed through a tri-state latch. A LOW state input to pin 25, $\overline{\text{Enable}}$, enables output data; input HIGH disables as illustrated in the figure 2.

TABLE 2. OUTPUT CODING

INPUT VOLTAGE	BIPOLAR	
	TWO'S COMPLEMENT (pin 27 = low)	INVERTED TWO'S COMPLEMENT (pin 27 = high)
+FS (+1.25V)	0111 1111 1111	1000 0000 0000
+FS –1 LSB	0111 1111 1110	1000 0000 0001
3/4 FS	0001 1111 1111	1110 0000 0000
+1/2 FS	0011 1111 1111	1100 0000 0000
+1 LSB	0000 0000 0000	1111 1111 1111
0	1111 1111 1111	0000 0000 0000
–1 LSB	1111 1111 1110	0000 0000 0001
–1/2 FS	1011 1111 1111	0100 0000 0000
–3/4 FS	1001 1111 1111	0110 0000 0000
–FS + 1 LSB	1000 0000 0000	0111 1111 1111
	B1(MSB) thru B12(LSB)	B1(MSB) thru B12(LSB)

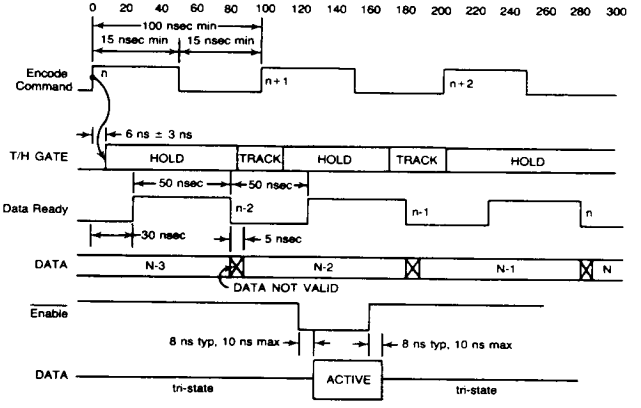


FIGURE 2. ADC-00113 TIMING DIAGRAM

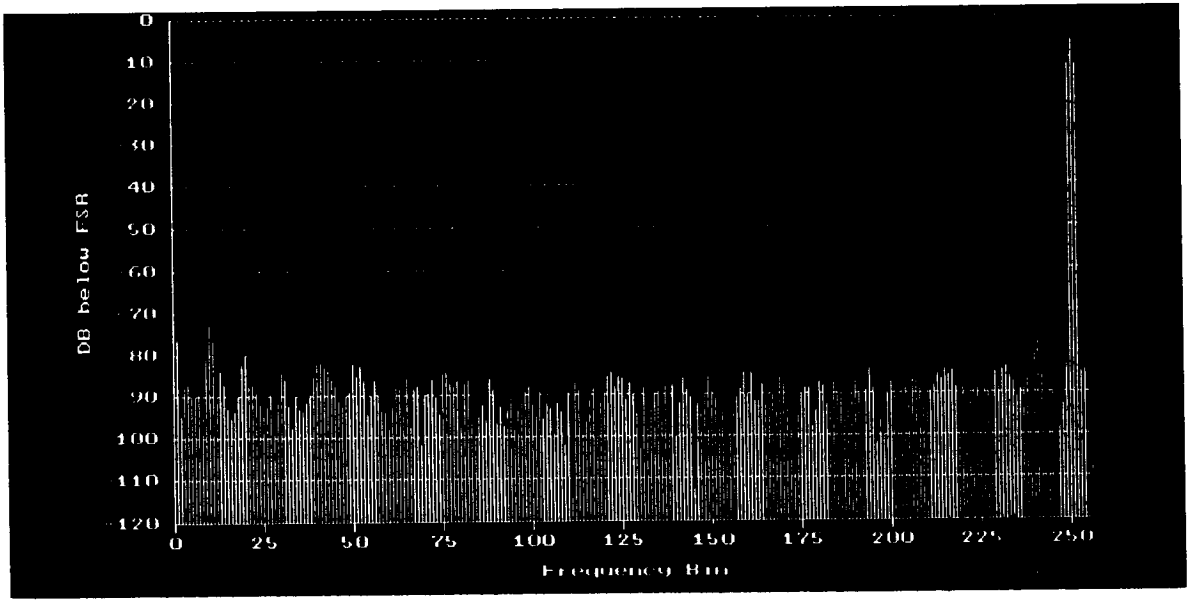
FFT TEST DESCRIPTION

In order to determine the harmonic distortion and signal to noise ratio of the ADC-00113, DDC uses some specialized hardware and an FFT analysis program. The details of the method are described below and illustrated in figure 3.

The FFT used is 512 points. The extra points that are taken can be used for either increasing the spectral resolution or for averaging a number of records to minimize the run-to run variation in readings. A single 512 point record typically gives run-to-run variations of as much as 1 dB in signal to noise ratio. An 8 record average can decrease this to about 0.2 dB. The 512 data samples are windowed using Hanning weighting. An FFT is then performed on the weighted bins. The frequency bins are then scanned for the bin with the largest amplitude. This is defined as the fundamental frequency. The amplitude of the fundamental is determined by computing the rms sum of the bin below the fundamental, the fundamental and the bin above the fundamental.

This 3-cell summation yields an amplitude accurate to less than 0.01 dB. The amplitude for each harmonic is calculated by summing the 3 bins around 2X the fundamental for the second harmonic, 3X the fundamental for the third and so on. This yields the harmonic distortion.

The signal to noise ratio is calculated by taking the rms sum of the frequency bins up to 255 (the Nyquist rate) with the exception of the dc term (bins 1, 2, and 3), the fundamental frequency (10 bins below the fundamental to 10 bins above the fundamental) and ±2 bins around each harmonic. The number of bins eliminated in each case is due to the leakage of the windowing function causing spillover into the area around the frequency terms. The summed frequency bins are then compared to the normalized fundamental for calculation of the broadband signal-to-noise ratio.



HARMONIC	BIN #	AMPLITUDE (dB)
1	251	- 1.04
2	10	-70.74
3	241	-80.69
4	20	-77.65
5	231	-80.07

SIGNAL-TO-NOISE RATIO = 65.10 dB
TOTAL HARMONIC DISTORTION = -68.17 dB
SIGNAL-TO-(NOISE + DISTORTION) = 63.68 dB
FFT size is 512 points.
Input Data Weighted by Hanning Window.

FIGURE 3. DYNAMIC TEST DATA

OFFSET AND GAIN ADJUSTMENT

The ADC-00113 is carefully laser-trimmed to its rated accuracy without external adjustments. The user may trim both input offset voltage error and gain error to zero by using external potentiometers (see Figure 4). The trim is typically 2%.

Note:

When large offset and gain changes are desired use other means, within the system, to achieve them; such as, using an input buffer amplifier.

For good high-speed analog practice, decoupling is recommended.

If offset and gain adjustment is not needed, pins 36 and 37 should be unconnected

TABLE 4. ADC-00113 PIN FUNCTIONS

PIN	FUNCTION	PIN	FUNCTION
1	Case Ground	46	Analog Ground
2	NC	45	T/H Analog Input
3	+5V Analog Supply	44	+15V Supply
4	T/H Analog Output	43	-15V Supply
5	A/D Analog Input	42	-5.2V Analog Supply
6	-5.2V Analog Supply	41	NC
7	NC	40	NC(Factory Test Point)
8	NC	39	NC
9	Bit 1 (MSB)	38	NC
10	Bit 2	37	Gain Adjust
11	Bit 3	36	Offset Adjust
12	Bit 4	35	Analog Ground
13	Bit 5	34	+15V Supply
14	Bit 6	33	-15V Supply
15	Bit 7	32	Analog Ground
16	Bit 8	31	-5.2V Digital Supply
17	Bit 9	30	+5V Analog supply
18	Bit 10	29	NC (Factory Test Point)
19	Bit 11	28	NC (Factory Test Point)
20	Bit 12 (LSB)	27	Output Logic Invert
21	+5V Digital Supply	26	Digital Ground
22	Data Ready	25	Output Enable
23	Digital Ground	24	Encode Command

Notes:
1. Pins 4 and 5 are to be externally connected.
2. NC means do not connect any signal to these pins as damage may occur to the hybrid.

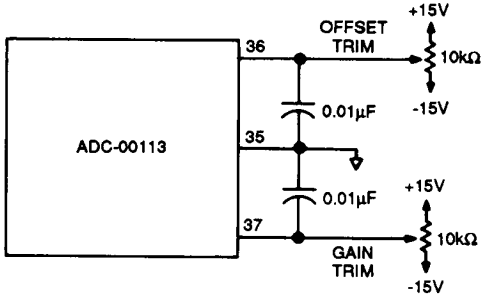


FIGURE 4. OFFSET AND GAIN ADJUSTMENT

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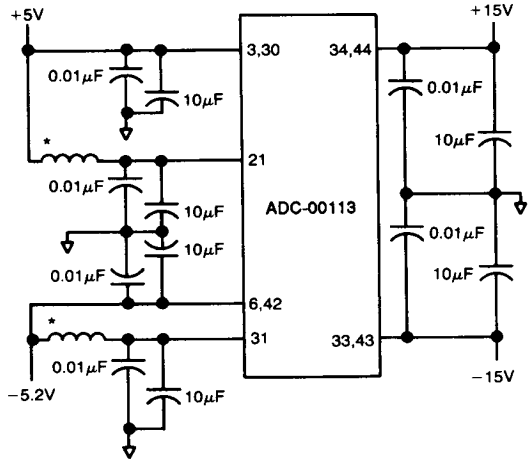
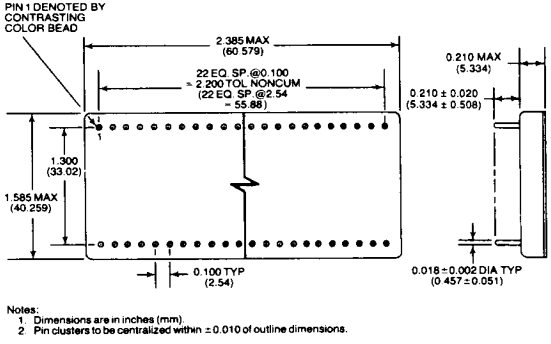
POWER SUPPLY DECOUPLING

Decoupling capacitors are required on each power supply to minimize noise. Figure 5 illustrates the recommended decoupling scheme. Each decoupled line must have a 10 µF or larger tantalum capacitor in parallel with a 0.01 µF ceramic capacitor. All capacitors must be mounted as close as possible to the hybrid package. While the user may use the same power supply for the 5.2V analog and digital supplies, it is recommended that the supply lines to the ADC-00113 be separated at the supply and treated as individual supplies at the board in order to minimize crosstalk. The same applies to the 5V analog and digital supplies. It is further recommended that an inductor, such as the Ferrox Cube Bead model #VK20020/4B be used in the digital supply line to prevent digital switching from being transposed on the analog supply. For instances where the user has a separate analog and digital supplies: the +5V current drain is approximately 20% digital; and the -5.2V current drain is approximately 50% digital.



*Ferrite bead. (See text on **POWER SUPPLY DECOUPLING**).

FIGURE 5. POWER SUPPLY DECOUPLING



Notes:
1. Dimensions are in inches (mm).
2. Pin clusters to be centralized within ±0.010 of outline dimensions.

FIGURE 6. ADC-00113 MECHANICAL OUTLINE

ORDERING INFORMATION

ADC-00113 – 1 0 2

Reliability:
- 0 = Standard DDC procedures
- 1 = Military processing available (Consult Factory)
- 2 = Military processing available but without QCI testing.(Consult Factory)

Operating Temperature Range:
- 1 = -55 to +125°C
- 3 = 0 to +70°C

B

Consult factory for ECL Logic Compatibility.