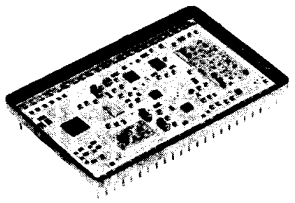
ADC-00110® AND ADC-00112®

12 BIT 10 MHz T/H + A/D HYBRID HIGH SPEED, SMALL SIZE, MIL-SPEC



NEW

PRELIMINARY

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DESCRIPTION

The ADC-00110 is a 12 bit, 10 MHz track/hold and A/D converter hybrid packaged in a 46 pin plug-in.

Containing T/H, A/D converter, data registers, tri-state output buffers, and timing circuits, the ADC-00110 is the fastest and smallest digitizer of its kind. The ADC-00110 operates over a temperature range of −55°C to +125°C and is available screened to MIL-STD-883.

The ADC-00110 is implemented with a 2-step A/D conversion algorithm. A number of factors contributed to achieving the ADC-00110's technical breakthroughs in speed and size. Foremost among them are proprietary ICs for the DAC, the conversion logic, and the gain amp functions. In addition, judicious use of thin film and thick film hybrid technology resulted in minimum layout area.

With its high speed, small package and wide operating temperature range, the ADC-00110 is ideal for the most demanding military and industrial data conversion applications. Typical of these applications are radar and sonar digitizing, vibration and FFT analysis, medical and nuclear instrumentation, and high speed data acquisition and communications systems.

FEATURES

- *INCLUDES:*
  - *TRACK/HOLD*
  - *A/D CONVERTER*
  - *TRI-STATE OUTPUT REGISTERS*
  - *TIMING CIRCUITS*
- *10 MHz WORD RATE*
- *SMALL 46 PIN PLUG-IN HERMETIC HYBRID*
- *TTL OR ECL OPTIONS*
- *−55°C TO +125°C OPERATING TEMPERATURE*
- *MIL-STD-883 SCREENING*

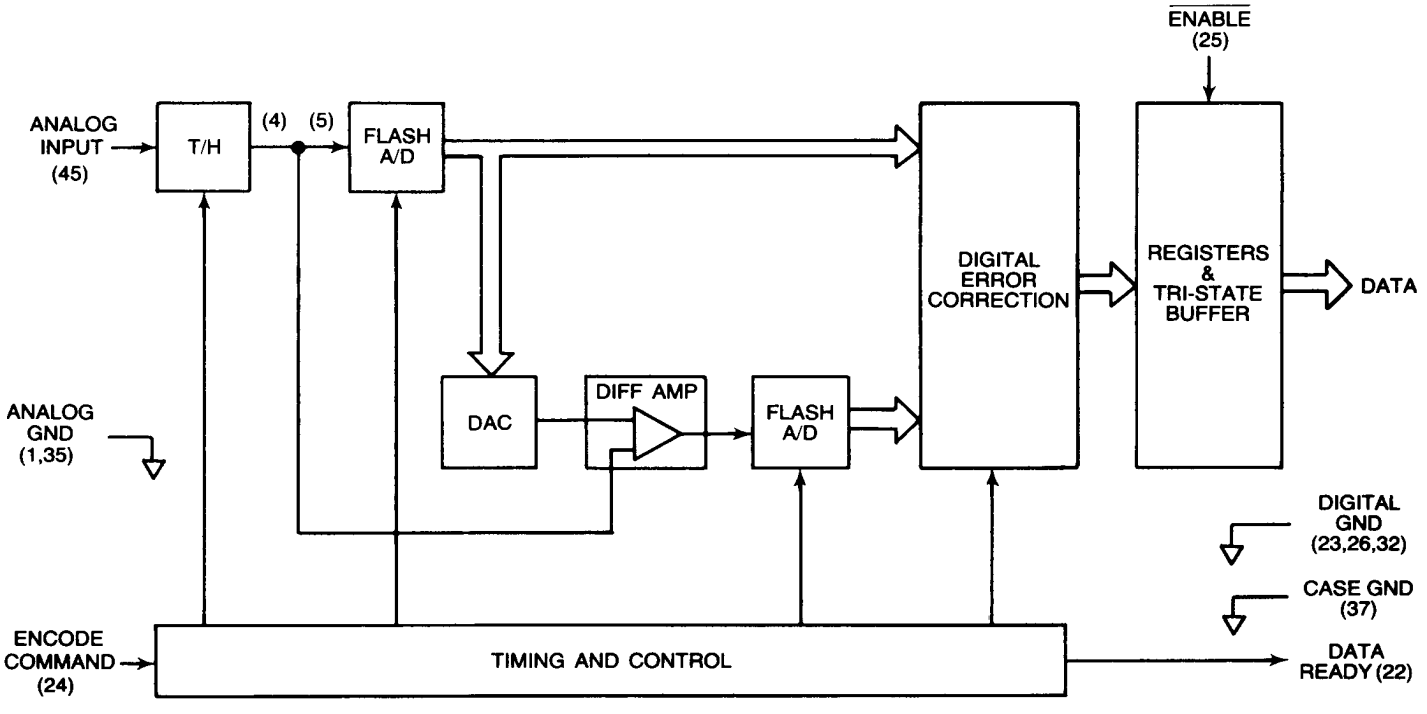


FIGURE 1. ADC-00110 BLOCK DIAGRAM

TABLE 1. ADC-00110 SPECIFICATIONS (T/H and A/D)		
Typical values at +25°C case temperature, nominal power supply voltages, and 10 MHz encode rate, unless otherwise noted.		
PARAMETER	**UNITS**	**VALUES**
Resolution	Bits	12
ACCURACY		
Linearity Error	%FSR	±0.025 typ, ±0.050 max
Linearity Error Tempco	ppm FSR/°C	2 max
Diff Linearity Error	LSB	±1 max
Gain Error	%FSR	±0.5 max
Gain Error Tempco	ppm FSR/°C	50
Offset Error	%FSR	±0.5 max
Offset Error Tempco	ppm FSR/°C	50 max
DYNAMIC CHARACTERISTICS		
Conversion Rate	MHz	DC to 10 min
Pipeline Delay[1]	nsec	2 Encode Commands +80 nsec
Aperture Uncertainty (Jitter)	psec	±20
Aperture Time (Delay)	nsec	6(±3)
Signal to Noise Ratio (SNR)[2]	db	66 typ, 62 min
Transient Response[3]	nsec	100 max
Overvoltage Recovery[4]	nsec	200 max
Input Bandwidth		
Small Signal, 3dB[5]	MHz	35
Large Signal, 3dB[6]	MHz	30
Two-tone linearity (at input frequencies)		
60 KHz; 62 KHz	db below FS	62 min
2.498 MHz; 2.500 MHz	db below FS	62 min
4.996 MHz; 4.998 MHz	db below FS	60 min
ANALOG INPUT		
Voltage Range		
(Normal Operation)	V	±2.5
(Absolute Max)	V	±5 max
Impedance		
Resistance	Ohms	1M min
Capacitance	pF	10
ENCODE COMMAND INPUT[7] (ADC-00110)		
Logic Levels, TTL Compatible	V	Logic 0 = 0.4 Logic 1 = 2.4
Minimum Pulse Width	nsec	10
Maximum Pulse Width	nsec	Encode Command Period −20 nsec
ENCODE COMMAND INPUT[7,8] (ADC-00112)		
Logic Levels, ECL Compatible	V	Logic 0 = −1.7 Logic 1 = −0.9
Minimum Pulse Width	nsec	10
Maximum Pulse Width	nsec	Encode Command Period −20 nsec
DIGITAL OUTPUT (ADC-00110)		
Format	Bits	12 parallel; NRZ
Logic Levels, TTL Compatible	V	Logic 0 = 0.4 Logic 1 = 2.4
Time Skew	nsec	5 max
Coding		Offset binary two's complement
DIGITAL OUTPUT (ADC-00112)		
Format	Bits	12 parallel; NRZ
Logic Levels, ECL Compatible	V	Logic 0 = −1.7 Logic 1 = −0.9
Time Skew	nsec	5 max
Coding		Offset binary two's complement

TABLE 1. ADC-00110 SPECIFICATIONS (T/H and A/D) (continued)		
PARAMETER	**UNITS**	**VALUES**
POWER SUPPLIES		
+15 Volt Supply	V	+15±5%
Current Drain	mA	80 typ, 120 max
−15 Volt Supply	V	−15±5%
Current Drain	mA	80 typ, 125 max
+5 Volt Supply	V	+5±5%
Current Drain	mA	300 typ, 400 max
−5.2 Volt Supply	V	−5.2±5%
Current Drain[9]	mA	600 typ, 700 max
Power Dissipation	W	7.0 typ, 9.25 max
TEMPERATURE RANGE		
Operating (Case)		
-1 Option	°C	−55 to +125
-3 Option	°C	0 to +70
Storage	°C	−55 to +165

Notes:
(1) Measured from the rising edge of Encode Command to the falling edge of Data Ready; use rising edge to strobe output data into external circuits. See figure 2, timing diagram.
(2) Rms signal to rms noise ratio with 996 KHz analog input.
(3) For full-scale step input, 12-bit accuracy attained in specified time.
(4) Recovers to 12-bit accuracy in specified time after 2 x FS input overvoltage.
(5) With analog input 40 dB below FS.
(6) With FS analog input. (Large-signal bandwidth flat within 0.2 dB, DC to 5M Hz.)
(7) Transition from digital 0 to digital 1 initiates encoding.
(8) Applies to ADC-00112 ECL compatible converter. Only logic input and output related specifications change. All other specifications are valid for both ADC-00110 and ADC-00112.
(9) ADC-00112 requires 650 typ, 750 max.

GENERAL DESCRIPTION

Figure 1 is a functional block diagram of the ADC-00110 sampling A/D converter. Its major elements are a track/hold amplifier, 6-bit and 8-bit flash A/D converters, a 6-bit D/A converter, and a differential amplifier. The remaining functions are timing and control circuits, digital buffers and registers.

These components implement a straightforward 2-step A/D conversion algorithm. First, the conversion cycle is initiated with the receipt of an Encode Command. This causes the timing circuit to place the track/hold in the HOLD mode, storing the voltage at its analog input. The flash A/D then generates a coarse encode of the sampled voltage. Its 6-bit coarse encode output is stored temporarily in the MSB register. At the same time, the coarse 6-bit word is input to the DAC, which converts it to an analog voltage.

The differential amplifier subtracts the voltage representing the coarse encode from the sampled input, and scales it up to the correct full scale range.

Next, the 8-bit flash A/D converter generates a fine encode of the scaled difference voltage. The fine encode 8-bit word is stored in the LSB register. Finally, the contents of the 6-bit MSB and 8-bit LSB registers are combined in the digital error correction circuit to yield a 12-bit output word. This 12-bit word is stored in the output registers. The encoded digital output is available upon application of an Enable signal to the tri-state output buffer.

Since the ADC-00110 has output storage registers, its digital output is available to the user at all times, except for a short interval when it is being updated. A Data Ready output signal is provided to indicate when the digital output is valid.

Care must be taken when designing with the ADC-00110, to achieve its rated performance. This high speed sampling A/D converter generates high frequency power supply and ground currents. For this reason, it is recommended that decoupling

capacitors be used on each power supply line. See the paragraph on Power Supply Decoupling for more detail. High frequency layout considerations should be kept in mind when designing a printed circuit board for the ADC-00110. Conductor lengths should be kept to a minimum, and a large area ground plane should be used to keep ground impedances as low as possible.

TIMING DIAGRAM

A typical ADC-00110 timing diagram is shown in figure 2. Note that the Encode Command repeats at 100 nsec intervals with a throughput (pipeline) delay of 280 nsec.

A conversion cycle is initiated by the application of a positive pulse (15 nsec min) to the Encode Command pin. The rising edge of the Encode Command starts the timing cycle. First, the internal track/hold is placed in the HOLD mode. The output signal is then delivered to the 6-bit flash A/D converter for a coarse conversion of these 6 MSBs. The output of the 6-bit flash A/D is also delivered to the D/A whose output is applied to the differential amplifier. The output of the differential amplifier is then delivered to the 8-bit flash A/D converter. Once the 8-bit flash conversion is complete, the internal T/H is returned to the TRACK mode. The output of the 8-bit flash A/D converter, along with the original coarse 6-bit word, is input to the digital error correction circuit with output to the 12-bit register. The Encode Command input then updates the register to take data.

The idea behind pipelining is that a second Encode is started before the first Encode has completed conversion. Consequently, the input signal is encoded and output data is delivered at a 10 MHz rate. The pipeline delay is two Encode periods plus 80 nsec, or 280 nsec, minimum. Since Data Ready stays low for 50 nsec, it is possible to use the Encode Command to enable and continuously take data at a 10 MHz rate, though output data lags analog input by two encode periods plus 80 nsec. Note that data is not valid during the first 5 nsec following the falling edge of Data Ready, but is otherwise valid. The timing diagram also indicates the tri-state propagation delays for both enabling and disabling the latch as 8 nsec typ, and 10 nsec max.

LAYOUT PRECAUTIONS

The ADC-00110 high speed sampling A/D converter generates high frequency power supply and ground currents, and is sensitive to coupled signals. High frequency layout considerations must therefore be kept in mind when designing a printed circuit board for it. All conductor lengths must be kept to a minimum, and a large area ground plane must be used to keep ground impedances as low as possible. Analog inputs and digital outputs must be kept separated from each other to minimize crosstalk. Input and output circuits must be kept as close to the A/D converter package as possible. Likewise, the three analog ground pins must be connected to the digital ground pin as close as possible to the hybrid package, with connection to the case ground pin. While the case ground pin may be left floating, it is recommended that the case be tied to the system ground in order to minimize ground contributions to noise.

POWER SUPPLY DECOUPLING

Decoupling capacitors are required on each power supply to minimize noise. Figure 3 illustrates the recommended decoupling scheme. Each decoupled line must have a 10 μF or larger tantalum capacitor in parallel with a 0.01 μF ceramic capacitor. All capacitors must be mounted as close as possible to the hybrid package. While the user may use the same power supply for the 5.2V analog and digital supplies, it is recommended that the supply lines to the ADC-00110 be separated at the supply and treated as individual supplies at the board in order to minimize crosstalk. The same applies to the 5V analog and digital supplies. It is further recommended that an inductor, such as the Ferrox Cube Bead model #UK20020/4B be used in the digital supply line to prevent digital switching from being transposed on the analog supply.

OUTPUT CODING

Output coding is illustrated in table 2. The ADC-00110 is TTL compatible and outputs offset binary and two's complement data. Moreover, data is accessed through a tri-state latch. A LOW state input to pin 25, $\overline{\text{Enable}}$, enables output data; input HIGH disables as illustrated in figure 2.

The ADC-00110 is ECL compatible and outputs offset binary and two's complement data. Pin 25 becomes $\overline{\text{Encode}}$ to enable differential input. External 100 Ohm pull-down resistors must be used. Other than logic format, the ADC-00110 and ADC-00112 are identical and exhibit the same electrical characteristics shown in table 1 unless otherwise noted.

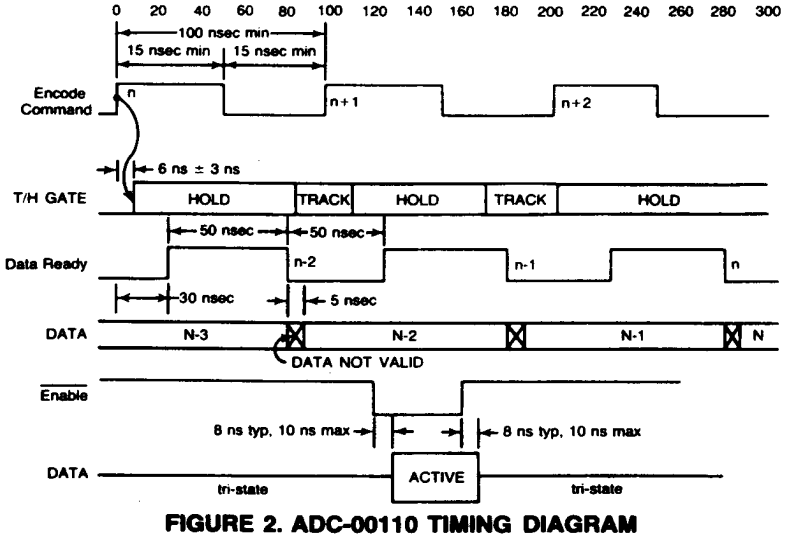
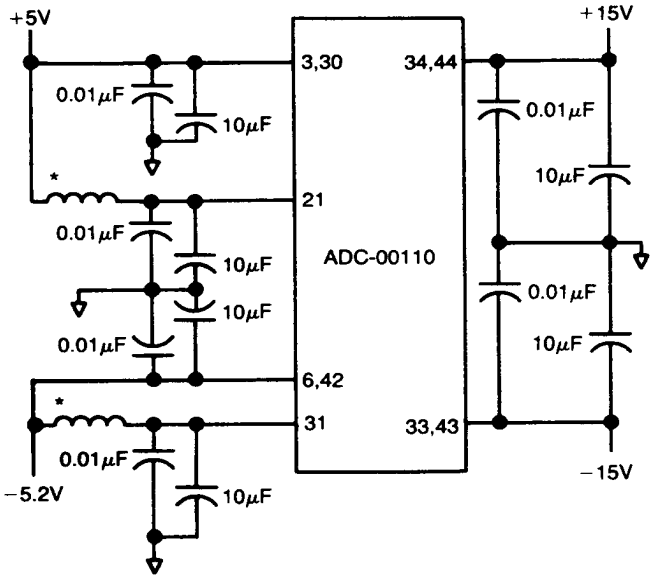


FIGURE 2. ADC-00110 TIMING DIAGRAM

TABLE 2. OUTPUT CODING

INPUT VOLTAGE	BIPOLAR	
	Offset Binary	Two's Complement
−FS	0000 0000 0000	1000 0000 0000
−¾FS	0001 1111 1111	1001 1111 1111
−½FS	0011 1111 1111	1011 1111 1111
−1 LSB	0111 1111 1110	1111 1111 1110
0	0111 1111 1111	1111 1111 1111
+1 LSB	1000 0000 0000	0000 0000 0000
+½FS	1011 1111 1111	0011 1111 1111
+¾FS	1101 1111 1111	0101 1111 1111
+FS−1LSB	1111 1111 1110	0111 1111 1110
+FS	1111 1111 1111	0111 1111 1111
	B1 thru B12	$\overline{\text{B1}}$, B2 thru B12



*Ferrite bead. (See text on **POWER SUPPLY DECOUPLING**).

FIGURE 3. POWER SUPPLY DECOUPLING

TABLE 3. ADC-00110 PIN FUNCTIONS

PIN	FUNCTION	PIN	FUNCTION
1	Analog Ground	46	Analog Return
2	NC	45	T/H Analog Input
3	+5V Analog Supply	44	+15V Supply
4	T/H Analog Output	43	−15V Supply
5	A/D Analog Input	42	−5.2V Analog Supply
6	−5.2V Analog Supply	41	NC
7	Overrange	40	NC (Factory Test Point)
8	$\overline{\text{MSB}}$	39	NC
9	Bit 1 (MSB)	38	NC
10	Bit 2	37	Case Ground
11	Bit 3	36	NC (Factory Test Point)
12	Bit 4	35	Analog Ground
13	Bit 5	34	+15V Supply
14	Bit 6	33	−15V Supply
15	Bit 7	32	Digital Ground
16	Bit 8	31	−5.2V Digital Supply
17	Bit 9	30	+5V Analog Supply
18	Bit 10	29	NC (Factory Test Point)
19	Bit 11	28	NC (Factory Test Point)
20	Bit 12 (LSB)	27	NC (Factory Test Point)
21	+5V Digital Supply	26	Digital Ground
22	Data Ready	25	$\overline{\text{Output Enable}}$
23	Digital Ground	24	Encode Command

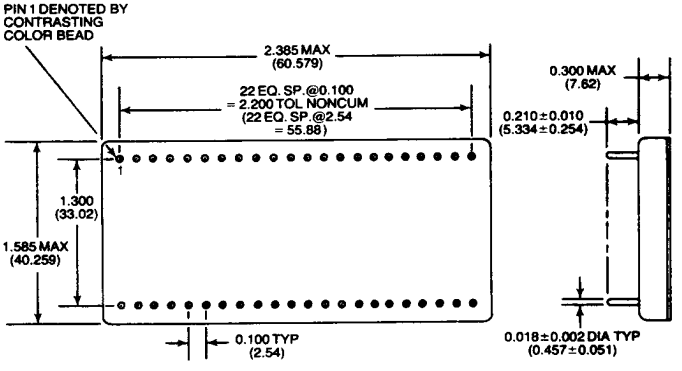
Notes:
1. Pins 4 and 5 are to be externally connected.
2. Pin 25 becomes Encode for ADC-00112, ECL.
3. The ADC-00112 output bits must have ECL terminations such as 100 Ohms to −2V or equivalent.
4. NC means do not connect any signal to these pins as damage may occur to the hybrid.

ORDERING INFORMATION

ADC-00110 - 1 0 2

- Reliability Grade:
  - 0 = Standard DDC procedures.
  - 1 = Fully compliant with MIL-STD-883
  - 2 = Screened to MIL-STD-883 but without QCI testing
- Operating Temperature Range (Case)
  - 1 = −55°C to +125°C
  - 3 = 0°C to +70°C
- Logic Compatibility:
  - 0 = TTL
  - 2 = ECL

ADC-00110-605 EVALUATION CARD



Notes:
1. Dimensions are in inches (mm).
2. Pin clusters to be centralized within ±0.010 of outline dimensions.

FIGURE 4. ADC-00110 AND ADC-00112 MECHANICAL OUTLINE

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