3 Electrical Characteristics

3.1 Absolute Maximum Ratings Over Operating Free-Air Temperature Range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) ..... 7 V
Input voltage range, V_I ..... −0.5 V to V_{DD} + 0.5 V
Analog output short-circuit duration to any power supply or common ..... unlimited
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Junction temperature, T_J ..... 175°C
Case temperature for 10 seconds, T_C ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

3.2 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Supply voltages, AV_{DD}, DV_{DD}	4.75	5	5.25	V
Reference voltage, V_{ref}	1.15	1.235	1.26	V
High-level input voltage, V_{IH}	2.4		V_{DD}+0.5	V
Low-level input voltage, V_{IL}			0.8	V
Output load resistance, R_L		37.5		Ω
FS ADJUST resistor, R_{SET}		523		Ω
XTAL1/XTAL2 crystal frequency		14.31818		MHz
Operating free-air temperature, T_A	0		70	°C

3.3 Electrical Characteristics

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = −800 µA	2.4			V
V_{OL}	Low-level output voltage	D(7–0), GI/O (4–0), VCLK, RCLK, SENSE, PCLKOUT, MCLK	I_{OL} = 3.2 mA			0.4	V
		HSYNCOUT, VSYNCOUT	I_{OL} = 15 mA			0.4	
		SCLK	I_{OL} = 18 mA			0.4	
I_{IH}	High-level input current	TTL inputs	V_I = 2.4 V			1	µA
		ECL inputs	V_I = 4 V			1	
I_{IL}	Low-level input current	TTL inputs	V_I = 0.8 V			−1	µA
		ECL inputs	V_I = 0.4 V			−1	
I_{DD}	Supply current	TVP3026-135A				500	mA
		TVP3026-175A				550	
		TVP3026-175B				350	mA
		TVP3026-220A				650	mA
		TVP3026-220B				450	mA
		TVP3026-250A				650	mA
		TVP3026-250B				530	mA
I_{DD}	Supply current reduction	TVP3026-135	DAC disabled		60		mA
		TVP3026-175			60		
		TVP3026-220			60		
		TVP3026-250			60		
		TVP3026-135A	DAC and DOT CLOCK disabled		300		mA
		TVP3026-175A			350		
		TVP3026-175B			200		mA
		TVP3026-220A			450		mA
		TVP3026-220B			300		mA
		TVP3026-250A			450		mA
		TVP3026-250B			380		mA
I_{OZ}	High-impedance-state output current					10	µA
C_i	Input capacitance	TTL inputs	f = 1 MHz, V_I = 2.4 V		4		pF
		ECL inputs	f = 1 MHz, V_I = 4 V		4		
V_{ID}	Differential input voltage	ECL inputs		0.6		6	V
V_{IC}	Common-mode input voltage	ECL inputs		2.85	3.15	V_{DD}−0.5	V

† All typical values are at V_{DD} = 5 V, T_A = 25°C.

3.4 Operating Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution (each DAC)		8/$\overline{6}$ high		8		bits
		8/$\overline{6}$ low		6		
E_L	End-point linearity error (each DAC)	8/$\overline{6}$ high			1	LSB
		8/$\overline{6}$ low			1/4	
E_D	Differential linearity error (each DAC)	8/$\overline{6}$ high			1	LSB
		8/$\overline{6}$ low			1/4	
Gray scale error					5%	
Output current (see Note 2)		White level relative to blank	17.69	19.05	20.4	mA
		White level relative to black (7.5 IRE only)	16.74	17.62	18.5	mA
		Black level relative to blank (7.5 IRE only)	0.95	1.44	1.9	mA
		Blank level on IOR, IOB	0	5	50	µA
		Blank level on IOG (with SYNC enabled)	6.29	7.6	8.96	mA
		Sync level on IOG (with SYNC enabled)	0	5	50	µA
		One LSB (8/$\overline{6}$ high)		69.1		µA
		One LSB (8/$\overline{6}$ low)		276.4		µA
DAC-to-DAC matching				2%	5%	
DAC-to-DAC crosstalk				–20		dB
Output compliance			–1		1.2	V
Voltage reference output voltage			1.15	1.235	1.26	V
Output impedance				50		kΩ
Output capacitance		f = 1 MHz, I_{OUT} = 0		13		pF
Sense voltage reference			300	350	400	mV
Clock and data feedthrough				–20		dB
Glitch area (see Note 3)				50		pV–s
Pipeline delay, VGA port				18		DOTCLK periods
Pipeline delay, pixel port (see Note 4)				18		DOTCLK periods
Pixel clock PLL, MCLK PLL	Lock time			5		ms
	Jitter			±200		ps

NOTES: 2. Test conditions for RS343-A video signals (unless otherwise specified), see Section 3.2, *Recommended Operating Conditions*, using external voltage reference V_{ref} = 1.235 V, R_{SET} = 523 Ω. When using the internal voltage reference, R_{SET} may need to be adjusted in order to meet these limits.

3. Glitch area does not include clock and data feedthrough. The – 3-dB test bandwidth is twice the clock rate.
4. Pipeline delay from pixel port depends on Latch Control Register setting. Value shown is for LCR = 0x06.

3.5 Timing Requirements (see Note 5 and Figures 3-1 and 3-2)

			TVP3026 -135		TVP3026 -175		TVP3026 -220		TVP3026 -250		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
	DOTCLK frequency			135		175		220		250	MHz
	Pixel clock PLL	Internal frequency		135		175		220		250	MHz
		PCLKOUT frequency		110		110		110		110	MHz
	MCLK PLL frequency			100		100		100		100	MHz
	VCO frequency, pixel clock PLL, MCLK PLL, and loop clock PLL		110	220	110	220	110	220	110	250	MHz
	CLK0 frequency for VGA mode 2			85		85		85		85	MHz
t_{cyc}	Clock cycle time	TTL	7.4		7.1		7.1		7.1		ns
		ECL	7.4		5.7		4.5		4		
t_{d4}	Delay time, RCLK to LCLK (see Note 6)			0.5		0.5		0.5	0.5		RCLK periods
t_{su1}	Setup time, RS(3–0) valid before $\overline{RD}$ or $\overline{WR}\downarrow$		10		10		10		10		ns
t_{h1}	Hold time, RS(3–0) valid after $\overline{RD}$ or $\overline{WR}\downarrow$		10		10		10		10		ns
t_{su2}	Setup time, D(7–0) valid before $\overline{WR}\uparrow$		35		35		35		35		ns
t_{h2}	Hold time, D(7–0) valid after $\overline{WR}\uparrow$		0		0		0		0		ns
t_{su3}	Setup time, VGA(7–0) and $\overline{VGAHS}$, $\overline{VGAVS}$, and $\overline{VGABL}$ valid before CLK0↑		2		2		2		2		ns
t_{h3}	Hold time, VGA(7–0) and $\overline{VGAHS}$, $\overline{VGAVS}$, and $\overline{VGABL}$ valid after CLK0↑		2		2		2		2		ns
t_{su4}	Setup time, P(63–0), and PSEL valid before LCLK↑		2		2		2		2		ns
t_{h4}	Hold time, P(63–0), and PSEL valid after LCLK↑		1		1		1		1		ns
t_{su5}	Setup time, $\overline{SYSHS}$, $\overline{SYSVS}$, and OVS valid before LCLK↑		2		2		2		2		ns
t_{h5}	Hold time, $\overline{SYSHS}$, $\overline{SYSVS}$, and OVS valid after LCLK↑		1		1		1		1		ns

NOTES: 5. TTL input signals are 0 to 3 V with less than 3 ns rise/fall time between the 10% and 90% levels unless otherwise specified. ECL input signals are $V_{DD}-1.8$ V to $V_{DD}-0.8$ V with less than 2 ns rise/fall time between the 20% and 80% levels. For input and output signals, timing reference points are at the 10% and 90% signal levels. Analog output loads are less than 10 pF. D7–D0 output loads are less than 50 pF. All other output loads are less than 50 pF unless otherwise specified.

6. This parameter only applies when SCLK is used as the VRAM shift clock. When SCLK is not used, the delay may be as much as is required by system logic (assuming the loop clock PLL compensates for the system delay).

3.5 Timing Requirements (see Note 5 and Figures 3-1 and 3-2) (continued)

			TVP3026 -135		TVP3026 -175		TVP3026 -220		TVP3026 -250		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{su6}	Setup time, $\overline{SYSBL}$ valid before LCLK↑		3		3		3		3		ns
t_{h6}	Hold time, $\overline{SYSBL}$ valid after LCLK↑		2		2		2		2		ns
t_{w1}	Pulse duration, $\overline{RD}$ or $\overline{WR}$ low		50		50		50		50		ns
t_{w2}	Pulse duration, $\overline{RD}$ or $\overline{WR}$ high		30		30		30		30		ns
t_{w3}	Pulse duration, clock high	TTL	3		3		2		2		ns
		ECL	3		2.5		2		2		
t_{w4}	Pulse duration, clock low	TTL	3		3		2		2		ns
		ECL	3		2.5		2		2		

NOTE 5. TTL input signals are 0 to 3 V with less than 3 ns rise/fall time between the 10% and 90% levels unless otherwise specified. ECL input signals are $V_{DD}-1.8$ V to $V_{DD}-0.8$ V with less than 2 ns rise/fall time between the 20% and 80% levels. For input and output signals, timing reference points are at the 10% and 90% signal levels. Analog output loads are less than 10 pF. D7–D0 output loads are less than 50 pF. All other output loads are less than 50 pF unless otherwise specified.

3.6 Switching Characteristics (See Figures 3-1 and 3-2)

PARAMETER		TVP3026-135			TVP3026-175			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
	SCLK/RCLK frequency (see Note 7)			85			85	MHz
	VCLK frequency (see Note 7)			85			85	MHz
t_{en1}	Enable time, $\overline{RD}$ low to D(7–0) valid			40			40	ns
t_{dis1}	Disable time, $\overline{RD}$ high to D(7–0) disabled			17			17	ns
t_{v1}	Valid time, D(7–0) valid after $\overline{RD}$ high	5			5			ns
t_{d1}	Delay time, $\overline{RD}$ low to D(7–0) starting to turn on	5			5			ns
t_{d2}	Delay time, selected input clock high/low to DOTCLK (internal signal) high/low		7			7		ns
t_{d3}	Delay time, SCLK high/low to RCLK high/low (see Notes 8, 9, and 10)	1	2	4	1	2	4	ns
t_{d6}	Analog output settling time (see Note 11)		6			5		ns
t_r	Analog output rise time (see Note 12)		2			2		ns
	Analog output skew	0		2	0		2	ns

NOTES: 7. SCLK can drive an output capacitive load up to 60 pF. The worst-case transition time between the 10% and 90% levels is less than 4 ns (typically 3 ns). RCLK and VCLK can drive output capacitive loads up to 15 pF, with worst-case transition times between 10% and 90% levels less than 4 ns (typically 3 ns).

8. The SCLK delay time to RCLK depends on the load that the signals drive. This parameter is measured with a VCLK = RCLK load of 15 pF and SCLK load of 60 pF.
9. In SCLK mode, RCLK is delayed from SCLK so that when RCLK is connected to LCLK, the timing is essentially the same as the TLC3407x family of parts.
10. This parameter applies when SCLK is used.
11. Measured within ± 1 LSB from 50% point of full-scale transition to output settling, (settling time does not include clock and data feedthrough).
12. Measured between 10% and 90% of full-scale transition.

3.6 Switching Characteristics (See Figures 3-1 and 3-2) (continued)

	PARAMETER	TVP3026-220			TVP3026-250			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
	SCLK/RCLK frequency (see Note 7)			85			85	MHz
	VCLK frequency (see Note 7)			85			85	MHz
t_{en1}	Enable time, $\overline{RD}$ low to D(7–0) valid			40			40	ns
t_{dis1}	Disable time, $\overline{RD}$ high to D(7–0) disabled			17			17	ns
t_{v1}	Valid time, D(7–0) valid after $\overline{RD}$ high	5			5			ns
t_{d1}	Delay time, $\overline{RD}$ low to D(7–0) starting to turn on	5			5			ns
t_{d2}	Delay time, selected input clock high/low to DOTCLK (internal signal) high/low		7			7		ns
t_{d3}	Delay time, SCLK high/low to RCLK high/low (see Notes 8, 9, and 10)	1	2	4	1	2	4	ns
t_{d6}	Analog output settling time (see Note 11)		5			5		ns
t_r	Analog output rise time (see Note 12)		2			2		ns
	Analog output skew	0		2	0		2	ns

NOTES: 7. SCLK can drive an output capacitive load up to 60 pF. The worst-case transition time between the 10% and 90% levels is less than 4 ns (typically 3 ns). RCLK and VCLK can drive output capacitive loads up to 15 pF, with worst-case transition times between 10% and 90% levels less than 4 ns (typically 3 ns).

8. The SCLK delay time to RCLK depends on the load that the signals drive. This parameter is measured with a VCLK = RCLK load of 15 pF and SCLK load of 60 pF.
9. In SCLK mode, RCLK is delayed from SCLK so that when RCLK is connected to LCLK, the timing is essentially the same as the TLC3407x family of parts.
10. This parameter applies when SCLK is used.
11. Measured within ± 1 LSB from 50% point of full-scale transition to output settling, (settling time does not include clock and data feedthrough).
12. Measured between 10% and 90% of full-scale transition.

3.7 Timing and Switching Diagrams

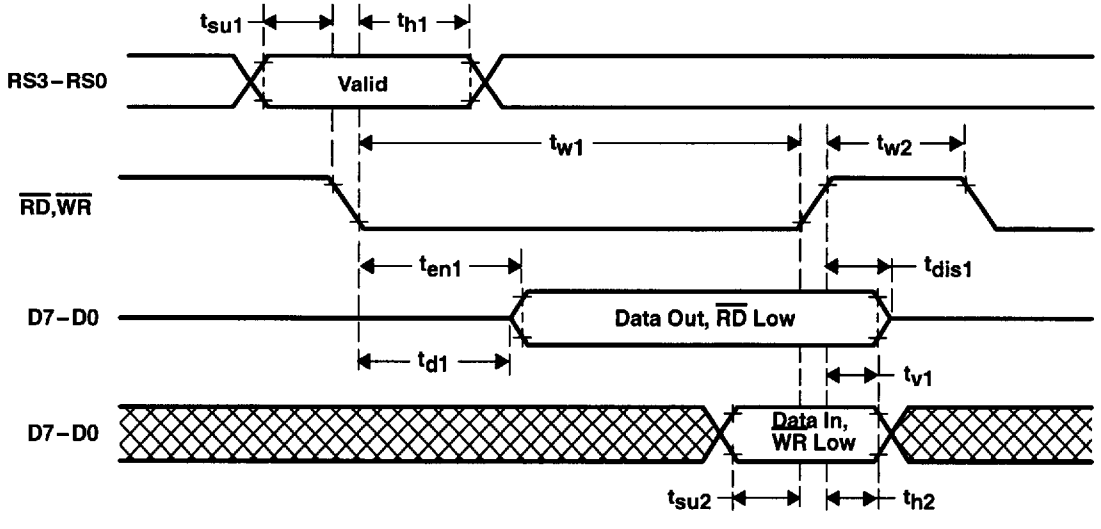

Figure 3–1. MPU Interface Timing and Switching Waveforms

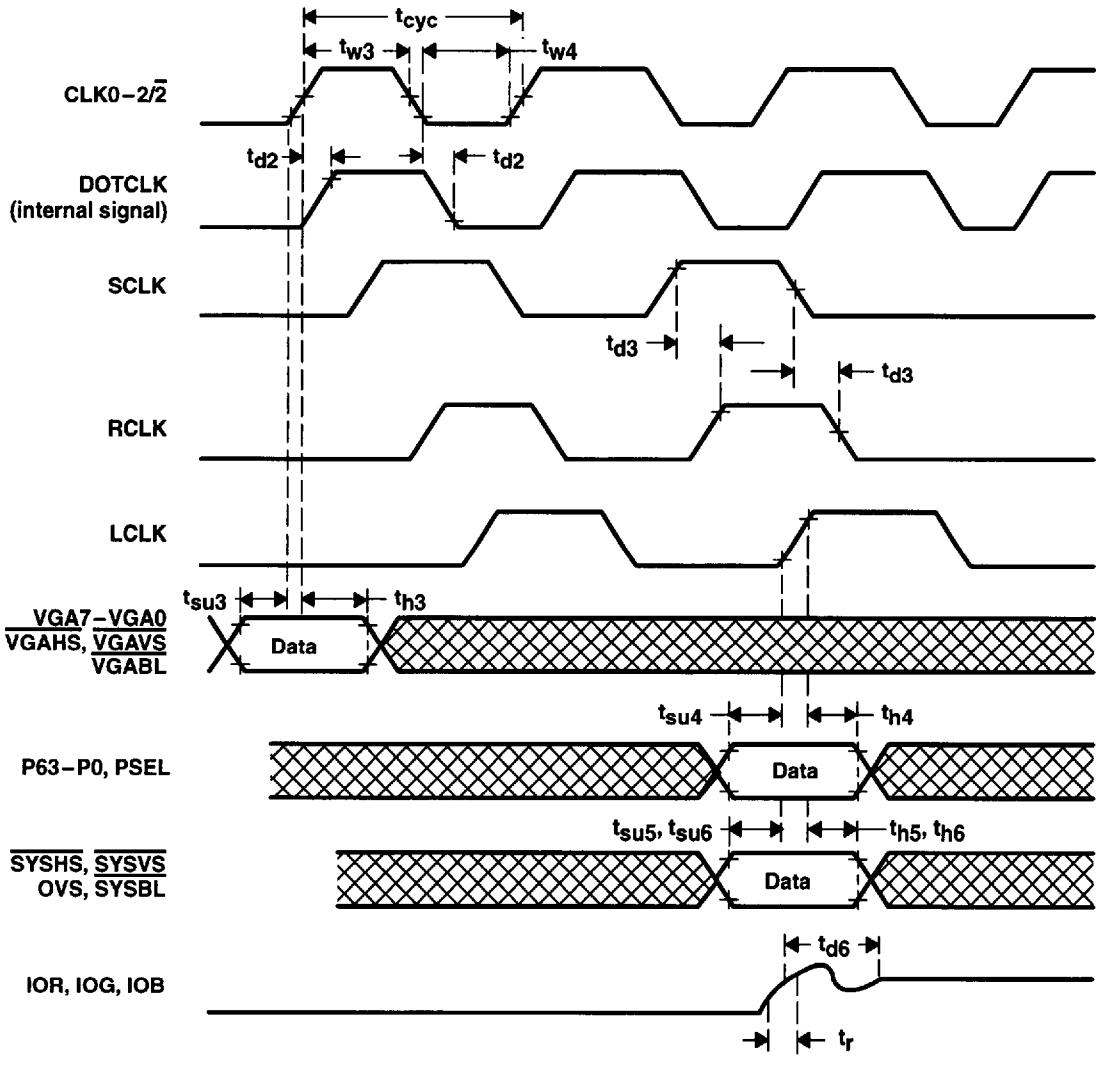

Figure 3–2. Video Input/Output Timing and Switching Waveforms