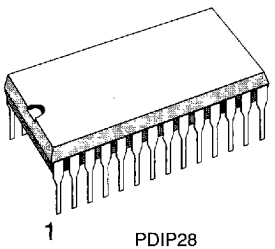
8-BIT EPROM HCMOS MCUs WITH EEPROM

PRELIMINARY DATA

- 3V to 5.5V supply operating range
- 4MHz Maximum Clock Frequency
- Fully static operation
- -25 to +85°C Operating Temperature Range
- Run, Wait, Stop and RAM Retention Modes
- User EPROM: 7168 bytes
  Data RAM: 224 bytes
  EEPROM: 256 bytes
- 28-pin Plastic Dual In Line and SO package for ST72T94 OTP version
- 28-pin Ceramic Dual In Line package for ST72E94 EPROM version
- 22 bidirectional I/O lines
- 6 lines programmable as interrupt wake-up inputs
- 16-bit timer with 1 input capture and 2 output compares
- 2V RAM retention mode
- Master Reset and power on reset
- Full Hardware Emulator
- Compatible with ST7294 (6K) and ST7293 (3.3K) ROM devices
- 8-bit data manipulation
- 74 basic instructions
- 10 main addressing modes
- 8x8 unsigned multiply instruction
- true bit manipulation
- Complete development support on real time emulator with PC/DOS
- Full software package (Cross Assembler, debugger)



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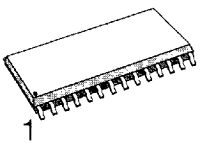

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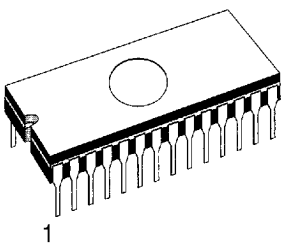

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(Ordering Information at the end of the datasheet)

1 GENERAL DESCRIPTION

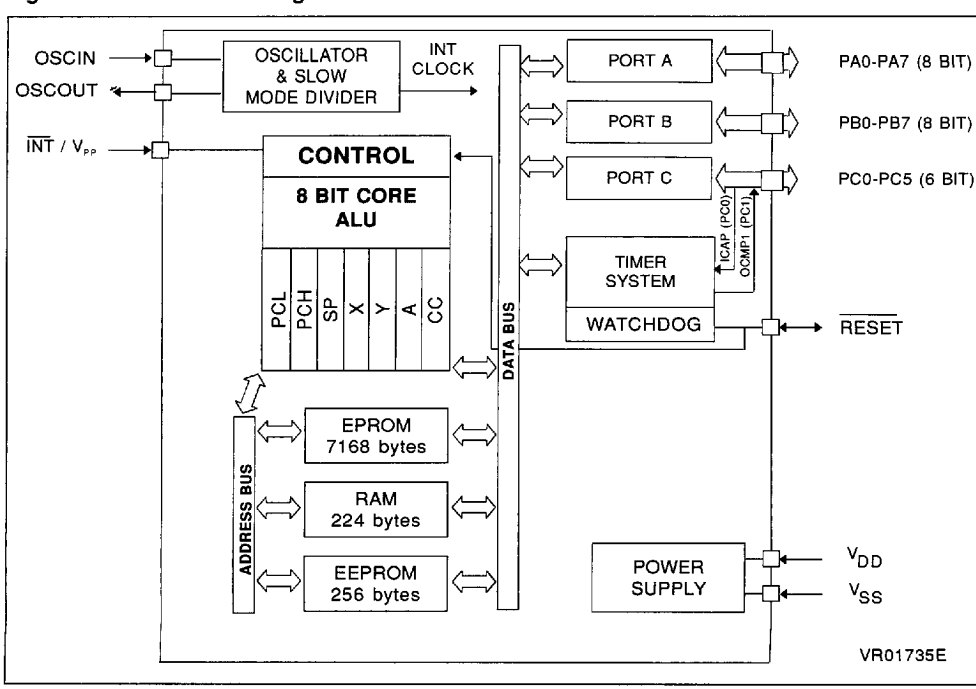
1.1 INTRODUCTION

The ST72E94 and ST72T94 (following mentioned as ST72E94) are EPROM members with EEPROM of the ST72 family of microcontrollers, in windowed ceramic (E) and plastic OTP (T) packages respectively, completely developped and produced by SGS-THOMSON Microelectronics using a n-well proprietary HCMOS process.The EPROM parts are fully compatible with their ROM versions and this datasheet will thus provide only information specific to the EPROM based devices. **THE READER IS ASKED TO REFER TO THE DATASHEET OF THE ST7294 AND ST7293 ROM-BASED DEVICES FOR FURTHER DETAILS.**

The EPROM ST72E94 may be used for the prototyping and the pre-production phases of development, can be configured as either a standalone microcontroller with 7K bytes of on-chip ROM, either as a microcontroller able to manage external memory.

The ST72E94 is a HCMOS microcontroller unit (MCU) from the ST72 family. It is based around an industry standard 8 bit core and offers an enhanced instruction set. The processor runs with an external clock at 4 MHz with a 5V supply and 2MHz with a 3V supply. Due to the fully static design of this device, operation down to DC is possible. Under software control the ST72E94 can be placed in WAIT or HALT mode thus reducing power consumption. The enhanced instruction set and addressing modes afford real programming potential. In addition to standard 8 bit data management the ST72E94 features true bit manipulation, 8x8 unsigned multiplication and indirect addressing modes. The device includes an on-chip oscillator, CPU, EPROM, RAM, EEPROM, I/O, and one timer with 1 input capture and 2 output compare systems.

Figure 1. ST72E94 Block Diagram



1.2 PIN DESCRIPTION

V_{DD}. Single power supply voltage 3 to 5.5V.

V_{SS}. Ground

OSCin, OSCout. Oscillator input and output pins. These pins are to be connected to a parallel resonant crystal or ceramic resonator. An external clock source can also be inputed thru OSCin.

$\overline{RESET}$. The active low input signal forces the initialization of the MCU. This event is the first priority non maskable interrupt. This pin is switched output low when the Watchdog has released. It could be used to reset external peripherals.

$\overline{INT}/V_{PP}$ is the external interrupt signal. Software configuration allows four triggering modes. In the EPROM programming Mode, this pin acts as the programming voltage input V_{PP}.

ICAP (PC0). Input capture signal going to the TIMER system. This signal, according to a mask option, can be an ICAP pin or PC0 pin. When PC0 is defined as ICAP, the internal pull-up resistor is not connected.

OCMP1 (PC1). Output compare signal coming from the TIMER system. This output signal, according to a mask option, can be an OCMP1 pin(for output compare 1 of the timer) or PC1 pin. When PC1 is defined as OCMP1, the internal pull-up resistor is not connected.

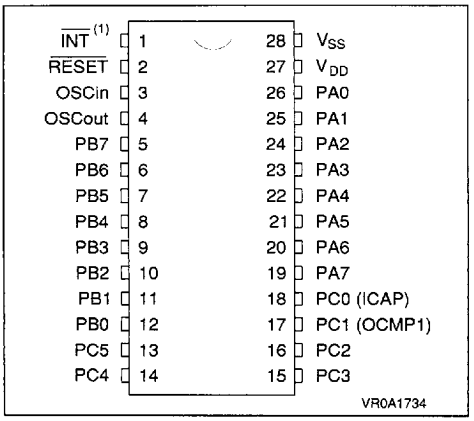
PA0-PA7, PB0-PB7, PC0-PC5. These 22 lines are standard I/O lines, programmable as either input or output.

- PORT A. 8 Standard I/O lines, accessed through DDRA and DRA Registers. According to a bit of the byte option, outputs can be defined as a standard push-pull output port or as an open drain output port. According to a bit of the byte option, a pull-up resistors (250kΩ typical at V_{DD}=3.5V) can be added on each line when it is defined as an input.

- PORT B. 8 Standard I/O lines accessed through DDRB and DRB Registers. According to a bit of the byte option, a pull-up resistor (250kΩ typical at V_{DD}=3.5V) can be added on each line when it is defined as an input.

- PORT C. 6 Standard I/O lines accessed through DDRC and DRC Registers. According to a bit of the byte option, these 6 lines can become 6 falling edge sensitive interrupt lines all linked to a single interrupt vector or 6 standard input ports. When these 6 lines are enabled as inputs, they are tied to V_{DD} through an internal pull-up resistor (250kΩ typical at V_{DD} = 3.5V). These negative edge sensitive interrupt lines can wake-up the ST72E94 from WAIT or HALT mode. This feature allows to build low power applications when the ST72E94 can be waken-up from keyboard push.

Figure 2. Pin Configuration



Note 1. This pin is also the V_{PP} input for EPROM based device

PIN DESCRIPTION (Continued)

Table 1. ST72E94 Pin Configuration

Name	Function	Description	Pin Assignment
$\overline{INT}/V_{PP}$	I	Interrupt / EPROM Programming Voltage	1
$\overline{RESET}$	I/O	Reset	2
OSCin	I	Oscillator	3
OSCout	O	Oscillator	4
PB7	I/O	Standard Port (bit programmable)	5
PB6	I/O	Standard Port (bit programmable)	6
PB5	I/O	Standard Port (bit programmable)	7
PB4	I/O	Standard Port (bit programmable)	8
PB3	I/O	Standard Port (bit programmable)	9
PB2	I/O	Standard Port (bit programmable)	10
PB1	I/O	Standard Port (bit programmable)	11
PB0	I/O	Standard Port (bit programmable)	12
PC5	I/O	Standard Port (falling edge interrupt line)	13
PC4	I/O	Standard Port (falling edge interrupt line)	14
PC3	I/O	Standard Port (falling edge interrupt line)	15
PC2	I/O	Standard Port (falling edge interrupt line)	16
PC1 (OCMP1)	I/O	Standard Port (falling edge interrupt line) or output compare	17
PC0 (ICAP)	I/O	Standard Port (falling edge interrupt line) or input capture	18
PA7	I/O	Standard Port (bit programmable)	19
PA6	I/O	Standard Port (bit programmable)	20
PA5	I/O	Standard Port (bit programmable)	21
PA4	I/O	Standard Port (bit programmable)	22
PA3	I/O	Standard Port (bit programmable)	23
PA2	I/O	Standard Port (bit programmable)	24
PA1	I/O	Standard Port (bit programmable)	25
PA0	I/O	Standard Port (bit programmable)	26
V_{DD}		Power Supply	27
V_{SS}		Ground	28

1.3 CENTRAL PROCESSING UNIT

1.3.1 Introduction

The CPU has a full 8-bit architecture. Six internal registers allow efficient 8-bit data manipulations. The CPU is able to execute 74 basic instructions. It features 10 main addressing modes. It is able to address 8192 bytes of memory and registers with its program counter.

1.3.2 CPU Registers

The 6 CPU registers are shown in the programming model in Figure 3. Following an interrupt, the registers are pushed onto the stack in the order shown in Figure 4. They are popped from stack in the reverse order. The Y register is not affected by these automatic procedures. The interrupt routine must therefore handle it, if needed, through the POP and PUSH instructions.

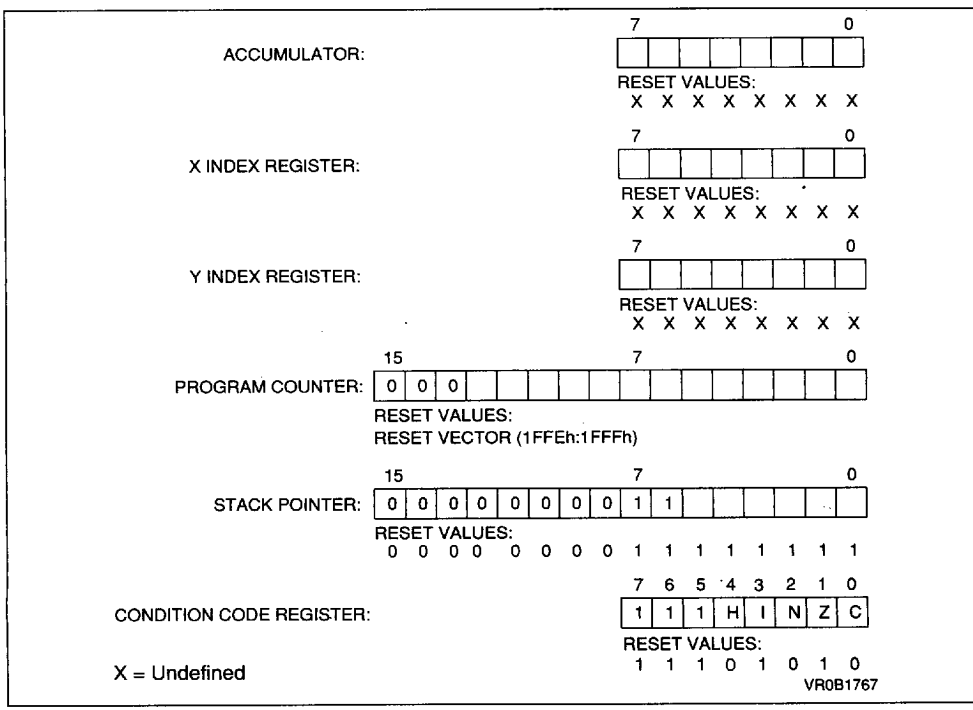
Accumulator (A). The accumulator is an 8-bit general purpose register used to hold operands and the results of the arithmetic and logic calculations as well as data manipulations.

Index Registers (X and Y). These 8-bit registers are used to create effective addresses or as temporary storage area for data manipulations. The cross assembler generates a PRECEDE instruction (PRE) to indicate that the following instruction refers to the Y register. The Y register is never automatically stacked. Interrupt routines must push or pop it by using the POP and PUSH instructions.

Program Counter (PC). The program counter is a 16-bit register containing the address of the next instruction to be executed by the CPU. In the ST72E94, only the 13 low order bits are used, bits 13, 14 and 15 are forced to "0".

Stack Pointer (SP). The stack pointer is a 16-bit register. The 6 least significant bits contain the address of the next free location of the stack. The 10 most significant bits are forced as indicated in Figure 3. They are reserved for future extension of ST72 family.

Figure 3. Programming Model



CENTRAL PROCESSING UNIT (Continued)

The stack is used to save the CPU context on subroutines calls or interrupts. The user can also directly use it through the POP and PUSH instructions.

After a MCU reset or after the reset stack pointer instruction (RSP), the stack pointer is set to its upper value (0FFh). It is then decremented after data has been pushed onto the stack and incremented after data is popped from the stack. When the lower limit is exceeded, the stack pointer wraps around to the stack upper limit. The previously stored information is then over written and therefore lost.

A subroutine call occupies two locations and an interrupt five locations.

1.3.3 Condition Code Register (CC).

The condition code register is a 5 bit register which indicates the result of the instruction just executed as well as the state of the processor. These bits can be individually tested by a program and specified action taken as a result of their state. The following paragraphs describe each bit.

Half carry bit (H). The H bit is set to 1 when a carry occurs between the bits 3 and 4 of the ALU during an ADD or ACC instruction. The H bit is useful in BCD arithmetic subroutines.

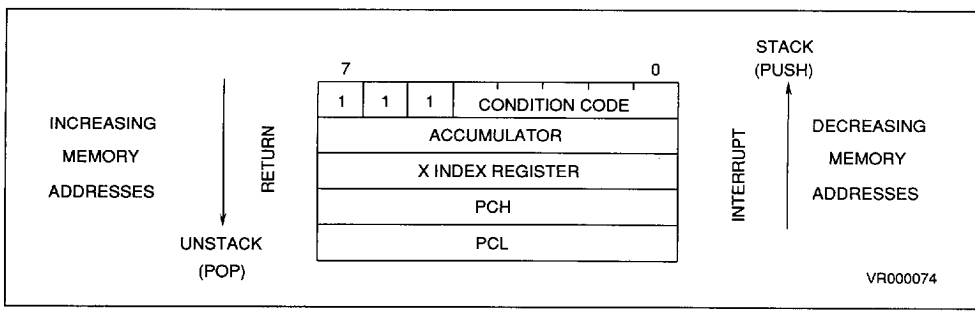
Interrupt mask (I). When the I bit is set to 1, all interrupts are disabled. Clearing this bit enables them. Interrupts requested while I is set are latched and can be processed when I is cleared (only one interrupt request per interrupt enable flag can be latched).

Negative (N). When set to 1, this bit indicates that the result of the last arithmetic, logical or data manipulation is negative (i.e. the most significant bit is a logic 1).

Zero (Z). When set to 1, this bit indicates that the result of the last arithmetic, logical or data manipulation is zero.

Carry/Borrow (C). When set, C indicates that a carry or borrow out of the ALU occurred during the last arithmetic operation. This bit is also affected during bit test, branch, shift and rotate instructions.

Figure 4. Stacking Order



1.4 MEMORY MAP

As shown in Figure 4, the MCU is capable of addressing 8192 bytes of memory and I/O registers. In the ST72E94, 7696 of these bytes are user accessible.

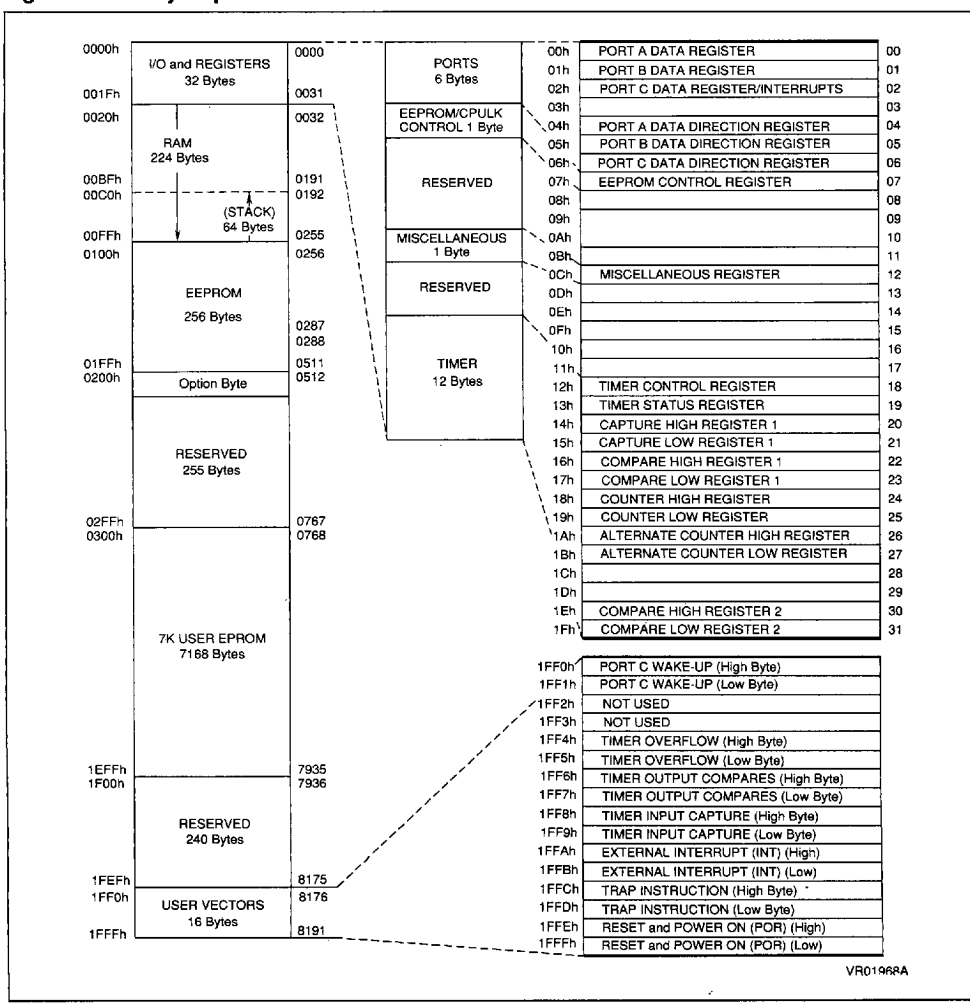
Note:

In the ST7293 only 3.25K bytes are user accessible. This should be taken into account by the user when programming the ST72E94 to emulate the ST7293.

The locations consist of 32 bytes of I/O registers (only 20 are used), 224 bytes of RAM, 256 bytes of EEPROM and 7Kbytes of user ROM. The RAM space includes 64 bytes for the stack from 0FFh to 0C0h. Programs that only use a small part of the allocated stack locations for interrupts and/or subroutine stacking purpose can use the remaining bytes as standard RAM locations.

The highest address bytes contains the user defined reset and interrupt vectors.

Figure 5. Memory Map



1.5 OPTION BYTE

An additional mode is used to configure the part for programming of the EPROM. This is set by a +12.5 voltage applied to the $\overline{INT}/V_{PP}$. The EPROM programming mode is entered during the reset phase if a 12.5 voltage applied to the $\overline{INT}/V_{PP}$ pin with the conditions of pin PC1=1 and pins PC0, PA6 and PA5=0. The 7K byte of EPROM memory may be programmed by using the EPROM Programming Boards (EPB) available from SGS-THOMSON.

The ROM devices of the ST72 family can be configured through mask options. In EPROM devices, most mask options are replaced by EPROM bits grouped in the Option Byte. The configuration of the device is made by programming the Option Byte.

The Option Byte is not in the user memory space. The Option Byte is accessed only if the device is in programming mode and location 0200h is addressed. The EPB provides all the functionality to select and program the Option Byte.

If a device emulated by the ST72E94 does not feature a particular mask option, the corresponding bit is not used. The Timer Clock is defined as $F_{OP}/4$.

7							0
WIW	WDMS	PBIP	PCWS	PC1S	PC0S	PA0S	PAIP

b7 = **WIW:** *Watchdog in Wait.*
1 : Watchdog suspended during Wait
0 : Watchdog active during Wait

b6 = **WDMS:** *Watchdog Mode Select.*
1 : Watchdog in Software Select Mode
0 : Watchdog in auto-enable Mode

b5 = **PBIP:** *Port B Input Pull-up.*
1 : Pull-up enabled or Port B (when Input)
0 : No Pull-up on Port B

b4 = **PCWS:** *Port C Wake-up Select.*
1 : Port C I/O functions enabled
0 : Port C Interrupt Wake-up Inputs enabled

b3 = **PC1S:** *PC1 Select.*
1 : Timer OCMP1 connected to pin 17
0 : PC1 I/O function connected to pin 17

b2 = **PC0S:** *PC0 Select.*
1 : Timer ICAP connected to pin 18
0 : PC0 I/O function connected to pin 18

b1 = **PA0S:** *Port A Output Select.*
1 : Port A Output is Push-pull
0 : Port A Output is Open-drain

b0 = **PAIP:** *Port A Input Pull-up.*
1 : Pull-up enabled on Port A (when Input)
0 : No Pull-up on Port A

1.6 EPROM ERASURE (ST72E94 ONLY)

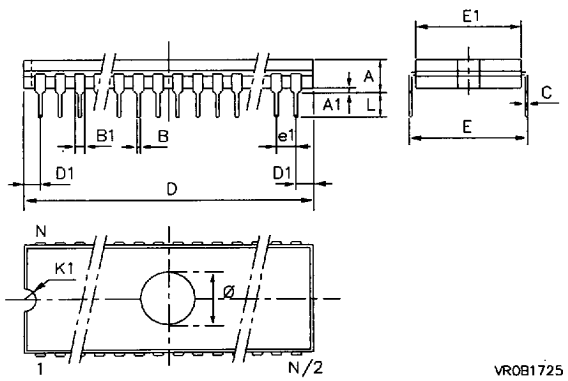
The ST72E94 is erased by exposure to high intensity UV light through the transparent window. This exposure discharges the floating gate to its initial state through induced photo current.

It is recommended that the ST72E94 be kept out of direct sunlight because the UV content of sunlight can cause temporary functional failure. Extended exposure to room level fluorescent lighting will also cause erasure. An opaque coating (paint, tape, label, etc...) should be placed over the package window if the product is to be operated under these lighting conditions. Covering the window also reduces IDD in stop mode due to photo diode currents.

An Ultraviolet source of wave length 2537Å yielding a total integrated dosage of 15 Watt-sec/cm^2 is required to erase the ST72E94. This device will be erased in 15 to 20 minutes if an UV lamp with a 12mW/cm^2 power rating is placed 1 inch from the lamp without filters.

1.7 PACKAGE MECHANICAL DATA

Figure 6. 28-Ceramic Dual In line Package, 600-Mil Width



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			5.71			0.225
A1	0.50		1.78	0.020		0.070
B	0.40		0.55	0.016		0.022
B1	1.17		1.42	.046		.056
C	0.22		0.31	0.009		0.012
D			38.10			1.500
D1	1.52		2.49	.060		.098
E	–	–	–	–	–	–
E1	13.05		13.36	.514		.526
L	3.00			.118		
e1	2.29		2.79	0.090		0.110
Ø	6.86		7.36	.270		.290
	Number of Pins					
N	28					