SSI 32H568
Servo Controller

June, 1989

DESCRIPTION

The SSI 32H568 Servo Controller is a CMOS device intended for use in Winchester disk drive head positioning systems. When used in conjunction with a position reference, such as the SSI 32H567 Servo Demodulator, and a motor driver, such as the SSI 32H569 Servo Motor Driver, the device allows the construction of a high performance, dedicated surface head positioning system which operates under microprocessor control.

The SSI 32H568 generates position and track crossing information from standard di-bit quadrature position signals, derived from a dedicated servo surface. In its seek mode, the controller attempts to match the actual head velocity to a programmed target value, while in its track mode, it keeps the head centered on a track. Internal status and control registers allow a microprocessor to select operating modes, monitor track information and establish velocity targets. (Continued)

FEATURES

- **Servo control for Winchester disk drives with dedicated surface head positioning systems**
- **Accepts standard di-bit quadrature position information**
- **500 KHz maximum servo frame rate**
- **Microprocessor bus interface compatible with 16 MHz 8051**
- **Seek and track modes**
- **Programmable velocity profile and loop gains**
- **Internal offset cancellation capability**
- **Track crossing interrupt**
- **Low power CMOS design**
- **Available in 32-pin DIP or 44-pin PLCC packaging**

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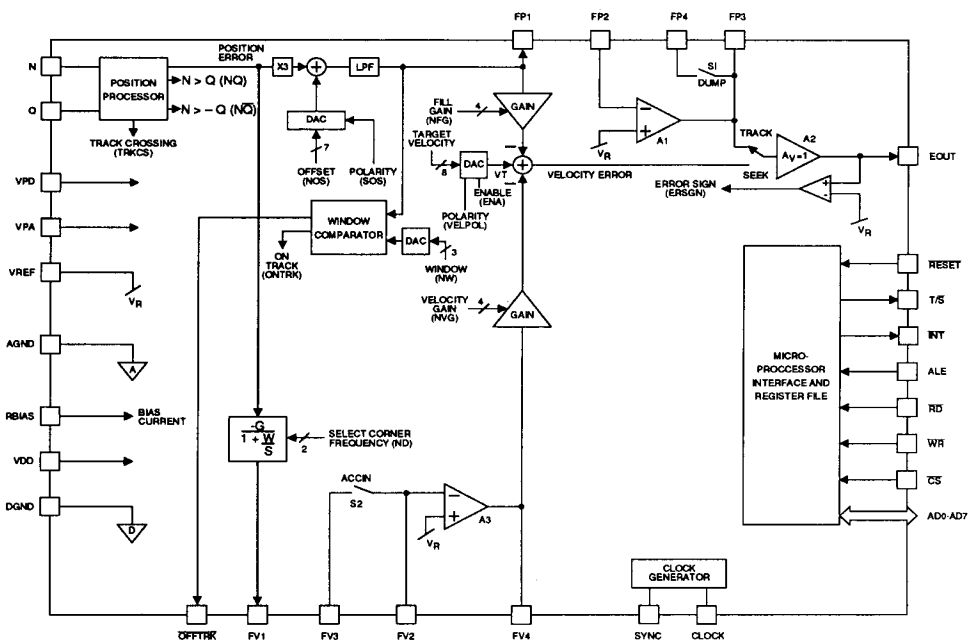
BLOCK DIAGRAM



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DESCRIPTION (Continued)

The microprocessor bus interface is optimized for use with multiplexed address/data bus microprocessors such as Intel's 8051, operating at up to16 MHz.

The SSI 32H568 is a low power, CMOS device and is available in 32-pin DIP and 44-pin PLCC packaging.

FUNCTIONAL DESCRIPTION

The SSI 32H568 receives position information from a servo demodulator through the analog inputs N and Q, which are sampled on the falling edge of SYNC. FSYNC, the maximum SYNC frequency (which is the servo frame rate) is 500 KHz. The position processor compares the analog N signal with both Q and –Q, to generate the digital signals NQ and N$\overline{Q}$. Since the N and Q signals have a period of four tracks, NQ and N$\overline{Q}$ provide additional information on which track the head is positioned over. Figure 6 shows the behavior of various position signals as radial displacement changes. A track crossing signal (TRKCS) may be programmed to provide an indication of each track crossing, or alternate track crossings. Internal timing hysteresis forces the NQ and N$\overline{Q}$ bits to remain constant for at least two servo frames. This prevents noise at the N and Q inputs from causing multiple track crossing indications at low head velocities.

The SSI 32H568 has two modes of operation, track and seek, which are selected under microprocessor control. In the track mode, the control loop drives the position error signal to zero. In the seek mode, the loop attempts to match the head velocity to a velocity target programmed through the microprocessor interface.

In track mode, the head position error signal is summed with an 8-bit programmable offset signal which may be used to null out circuit offsets or to permit reading of off-track data. This adjusted position error signal is available on pin FP1. A lowpass filter with a corner frequency above 0.1 • FSYNC provides a small amount of smoothing. A position loop filter may be constructed from external RC components and amplifier A1, whose output is switched to buffer amplifier A2 while track mode is selected (control bit T/$\overline{S}$=1). Switch S1, controlled by the DUMP bit, is used to keep the feedback capacitor in the position loop filter discharged while the controller is in seek mode. The output of A2 is the error signal (EOUT) which should be connected to the servo motor driver circuitry. The position error is also applied to a window comparator with programmable limits that provide a digital indication of whether the head is on track or not, through the ONTRK bit in the status register. In systems employing the SSI 32H569, EOUT should be connected to the SSI 32H569 ERR- pin through an input resistor.

The SSI 32H568 has a calibration control which permits the cancellation of position error offsets. When the control bit CAL is set, the inputs to the position processor are switched to VREF instead of N and Q. A comparator connected to the EOUT pin senses the sign of the error signal (ERSGN), allowing the microprocessor to alter the offset DAC input word until an LSB change causes ERSGN to change state. At this point internal offsets in the position error path have been cancelled.

In seek mode, the position error is differentiated by a switched capacitor differencer, to produce a velocity estimate. The differencer does not sample the position error immediately after the discontinuity that occurs when a track boundary is crossed. This prevents the discontinuity from disturbing the differentiator output. The velocity estimate is applied to a velocity loop filter consisting of external RC components and amplifier A3. A signal proportional to motor current may also be summed in at A3, to compensate for the fact that during rapid acceleration the high pass filter does not accurately model a differentiator. Switch S2, controlled by the ACCIN bit, allows the motor current feedback to be altered under microprocessor control. A velocity error term is computed as the difference between the velocity target and the actual head velocity. The velocity target is generated by a DAC from the digital word stored in the TARGET register. The output of the velocity loop filter (pin FV4) is proportional to the actual head velocity and is scaled by a 4-bit programmable velocity gain before being subtracted from the velocity target. Also, a fill signal which is generated by multiplying the position error by a 4-bit programmable fill gain is subtracted from the velocity error. The fill signal compensates for the 8-bit quantization of the velocity target signal, which becomes a factor as the head velocity approaches zero. As the head nears the destination track at the end of a seek operation, the target velocity is zero, so if a fill term which is proportional to position error is subtracted from the velocity error term, the velocity loop will cause the head to come to rest at the center of the track. Without this additional fill signal, the velocity loop would not necessarily center the head

in the destination track. In seek mode, the velocity error signal is switched to buffer amplifier A2, which drives the EOUT pin.

The actual velocity profile of the head is determined by the values written to the target velocity DAC. Typically, a new velocity target is written at each track crossing. An automatic update feature (enabled when UPDATE=1) causes the next velocity target to be loaded from a holding register when a track crossing occurs, so that the microprocessor does not have to perform this time-critical operation.

The SSI 32H568 has 8 registers, described in "Register Description", which are accessed through a microprocessor interface optimized for multiplexed address/data bus processors. A 3-bit register address is latched from the bus on the falling edge of ALE (address latch enable) and a bus cycle occurs if $\overline{CS}$ (chip select) and either $\overline{RD}$ (read strobe) or $\overline{WR}$ (write strobe) are asserted. An open drain interrupt line ($\overline{INT}$) may be used to cause a microprocessor interrupt when a track crossing occurs.

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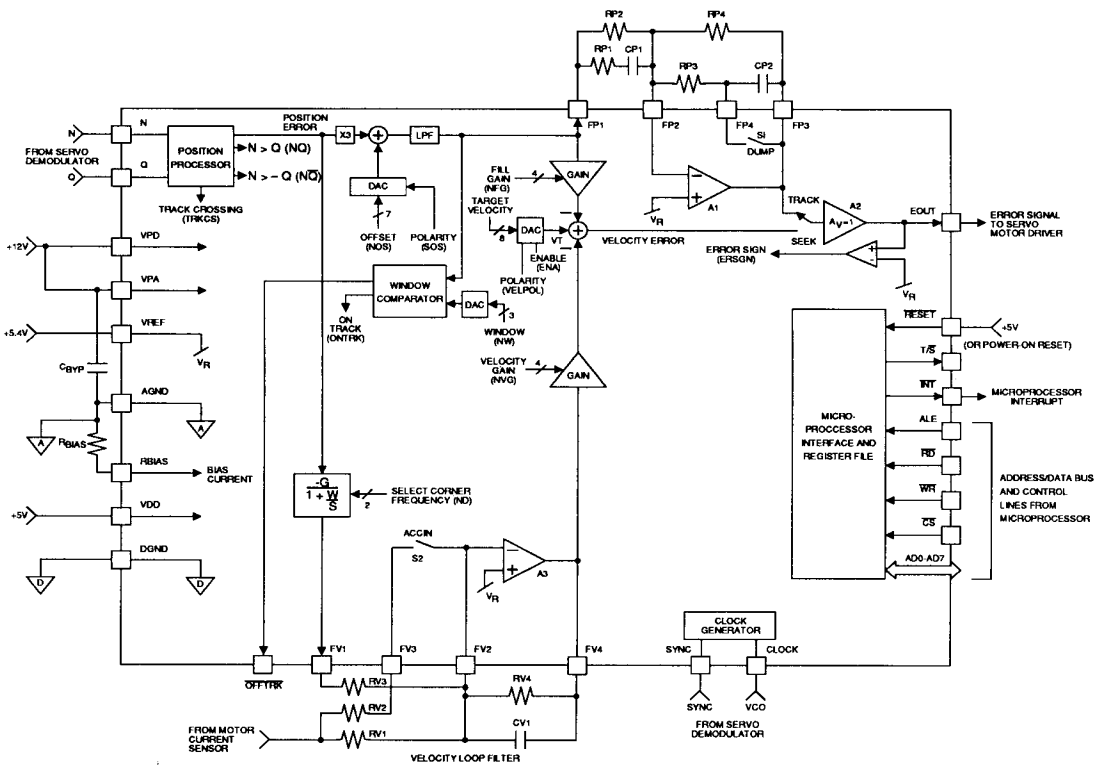

FIGURE 2: SSI 32H568 Typical Application

PIN DESCRIPTION

POWER

NAME	32-pin DIP	44-pin PLCC	TYPE	DESCRIPTION
RBIAS	11	16	I	BIAS INPUT - This input sets the internal opamp bias currents. A 20 KΩ 1% resistor should be connected between RBIAS and AGND.
VREF	12	17	I	REFERENCE VOLTAGE - 5.4V input which is used as the DC reference level for all analog signals. (This level is available as an output from the SSI 32H567).
AGND	13	19		ANALOG GROUND
DGND	18	27		DIGITAL GROUND
VDD	19	28		DIGITAL 5V SUPPLY - 5 volt supply for the microprocessor interface circuitry.
VPD	31	43		DIGITAL 12V SUPPLY - 12 volt supply for the switched capacitor filter clocks.
VPA	32	44		ANALOG 12V SUPPLY - 12 volt supply for all analog circuitry.

POSITION REFERENCE INTERFACE

Q	9	14	I	QUADRATURE INPUT - Analog position signal from servo demodulator.
N	10	15	I	NORMAL INPUT - Analog position signal from servo demodulator (90 degrees or 1 track out of phase with Q signal).
SYNC	29	40	I	SYNC INPUT - The falling edge of this clock causes the analog information on the N, Q inputs to be sampled. There is one SYNC pulse per servo frame and the maximum rate is 500 KHz. This signal is generated by the SSI 32H567.
CLOCK	30	41	I	CLOCK INPUT - This clock must be either 32 or 72 times the rate of the SYNC clock (selected by the FRFMT bit in STATUS register). It is usually supplied by the VCO output of the servo demodulator (eg. SSI 32H567).

MICROPROCESSOR INTERFACE

$\overline{CS}$	14	21	I	CHIP SELECT - Active low signal enables device to respond to microprocessor read or write.
ALE	15	22	I	ADDRESS LATCH ENABLE - Falling edge latches register address from pins AD0-AD2.
$\overline{RD}$	16	23	I	READ STROBE - Active low signal causes the contents of the addressed register to be placed on the address/data bus (AD0–7) if $\overline{CS}$ is also active.

MICROPROCESSOR INTERFACE (Continued)

NAME	32-pin DIP	44-pin PLCC	TYPE	DESCRIPTION
$\overline{WR}$	17	24	I	WRITE STROBE - Active low signal causes the data on the address/data bus to be written to the addressed register if $\overline{CS}$ is also active.
$\overline{INT}$	20	29	O	INTERRUPT - This active low open drain output is asserted when a track crossing is detected. It is released when the internal track crossing status bit (TRKCS) is read by the microprocessor.
T/$\overline{S}$	-	30	O	TRACK/SEEK - This output reflects the state of the T/$\overline{S}$ bit in the STATUS register. It is high when the device is in track mode and low when it is in seek mode (PLCC package only).
AD7 -AD0	21-28	31-32 34-39	I/O	ADDRESS/DATA BUS - 8-bit bus which carries register address information and bi-directional data.
$\overline{RESET}$	-	42	I	RESET - This active low input is used to force all the internal registers to their reset condition (PLCC package only).
$\overline{OFFTRK}$	-	26	O	OFFTRACK - This open drain output is asserted whenever the head position is outside the window specified by NW. It is always asserted in seek mode (PLCC package only).

CONTROL LOOP

FV4	1	1	O	VELOCITY FILTER OUTPUT - This is the output of amplifier A3 which forms part of the velocity loop filter. This signal is internally amplified and compared to the target velocity.
FV3	2	3	I	VELOCITY FILTER INPUT (SWITCHED) - This input is connected to the inverting input of amplifier A3 through a switch which is closed when control bit ACCIN is set and open when ACCIN is cleared.
FV2	3	5	I	VELOCITY FILTER INPUT - Direct connection to the inverting input of amplifier A3.
FV1	4	7	O	ESTIMATED VELOCITY OUTPUT - Output of the position error differentiating high pass filter.
EOUT	5	9	O	LOOP ERROR SIGNAL - Buffered output which is the position error in track mode (T/$\overline{S}$ = 1) or the velocity error in seek mode (T/$\overline{S}$ = 0). This signal should be connected to the servo motor driver circuitry. In systems using the SSI 32H569 servo driver, EOUT is connected to the SSI 32H569 pin ERR- through a resistor.
FP4	*	11	O	POSITION FILTER CAPACITOR - The external position loop filter feedback capacitor should be connected between this pin and FP3. When the DUMP bit in register WINDOW is set, an internal switch (S1) shorts FP3 to FP4. This allows the external capacitor to be kept discharged during seek mode.

CONTROL LOOP (Continued)

NAME	32-pin DIP	44-pin PLCC	TYPE	DESCRIPTION
FP3	6	10	O	POSITION FILTER OUTPUT - Output of position loop filter amplifier A1. In track mode this signal is the position error and is internally connected to buffer amplifier A2.
FP2	7	12	I	POSITION FILTER INPUT - Inverting input to opamp A1.
FP1	8	13	O	POSITION ERROR OUTPUT - Offset-corrected output of the position processing circuitry, which is proportional to the radial displacement of the head from the center of the current track.
The actual transfer function from N, Q to FP1 is: $H(z) = \frac{3}{2z-1} \frac{\sin(\omega T/2)}{\omega T/2}$ where: $T = 1/FSYNC$, $z = e^{sT}$				
This transfer function exhibits a high frequency roll off with a 3dB point at f = 0.11 FSYNC.				
Unused pins on PLCC package: 2,4,6,8,18,20,25,33				
* FP4 tied to FP2, Pin 7, internally on 32 pin DIP package.				

REGISTER DESCRIPTION

The SSI 32H568 has 8 internal registers which contain status, control and loop parameter information. A three bit register address is latched from inputs AD0-AD2 on the falling edge of ALE. The corresponding register is accessed if $\overline{CS}$ is then asserted, with the direction of access being determined by $\overline{RD}$ or $\overline{WR}$. The registers are summarized in Figure 3.

REGISTER	ADDRESS	ACCESS	D7	D6	D5	D4	D3	D2	D1	D0
GAIN	0	READ/ WRITE	NFG				NVG			
TARGET	1	READ/ WRITE	TARGET VELOCITY							
NEXT	2	READ/ WRITE	NEXT TARGET VELOCITY							
VELCON	3	READ/ WRITE	UNUSED			ND		UPDATE	ENA	VELPOL
WINDOW	4	READ/ WRITE	CAL	UNUSED	DUMP	T/$\overline{S}$	UNUSED	NW		
STATUS	5	AS NOTED	ERSGN (READ ONLY)	ACCIN (READ/WRITE)	CSMOD (READ/WRITE)	FRFMT (READ/WRITE)	ONTRK (READ ONLY)	NQ (READ ONLY)	NQ (READ ONLY)	TRKCS (READ ONLY)
OFFSET	6	READ/ WRITE	SOS	NOS						
RESET	7	WRITE ONLY	RESET (ANY VALUE)							

FIGURE 3: SSI 32H568 Register Map

REGISTER DESCRIPTION (Continued)

GAIN **Address 0** **Read/Write**

GAIN SETTINGS - Used to set the velocity gain and fill gain. These settings are only significant in the seek mode.

BIT	NAME	DESCRIPTION
0-3	NVG0-3	VELOCITY GAIN - 4-bit quantity which sets the gain applied to the velocity signal at the output of opamp A3.
4-7	NFG0-3	FILL GAIN - 4-bit quantity which sets the gain applied to the position error which is added to the velocity signal.

If NVG and NFG are represented as integers ranging from 0 to 15, then for a zero velocity target, the error output in seek mode is given by:

$$EOUT - VREF = \frac{NVG}{15}(FV4 - VREF) + \frac{NFG}{255}(FP1 - VREF)$$

TARGET **Address 1** **Read/Write**

CURRENT VELOCITY TARGET - This register selects the 8 bit velocity target which is subtracted from the actual velocity to yield velocity error in seek mode. The sign of the velocity target is determined by the VELPOL bit in register VELCON. If TARGET is represented as an integer from 0 to 255, then the voltage at the output of the velocity target DAC, VT, is given by:

$$VT = VREF\left(1 - \frac{TARGET}{340}\right), VELPOL = 0$$

$$VREF\left(1 + \frac{TARGET}{340}\right), VELPOL = 1$$

The SSI 32H568 has an update feature which allows this register to be loaded automatically with the contents of the next target register when a track crossing occurs. The target register may also be written to directly by the microprocessor to cause an immediate change in target velocity.

NEXT **Address 2** **Read/Write**

NEXT TARGET VELOCITY - This register contains an 8-bit value that will be loaded automatically into the velocity target register when a track crossing occurs, if the UPDATE bit in VELCON is set. This register is unused if UPDATE is cleared.

REGISTER DESCRIPTION (Continued)

VELCON Address 3 Read/Write

BIT	NAME	DESCRIPTION
0	VELPOL	VELOCITY TARGET POLARITY - If this bit is set, the velocity target will be positive (with respect to VREF) and if it is reset, the velocity target will be negative.
1	ENA	ENABLE VELOCITY TARGET DAC - If ENA is set, the velocity target DAC will be enabled and if it is cleared the output of the DAC will be clamped to VREF.
2	UPDATE	UPDATE MODE SELECT - When this bit is set, the contents of the NEXT register will be transferred to TARGET automatically when a track crossing occurs. If it is cleared, new velocity targets must be written directly to the TARGET register by the microprocessor.
3-4	ND0-ND1	DIFFERENTIATOR CHARACTERISTIC SELECT - These bits select the characteristic of the differentiator high pass filter as follows: $H(s) = \frac{-G}{1 + \frac{W}{s}}$, $W = \frac{1}{2T}\left(1 + \frac{ND}{1.75}\right)$ rad/sec $G = 14.3$ Where T is the period of the SYNC clock input in seconds, s is the complex frequency variable in radians/second and ND is an integer from 0 to 3. For s<<W the high pass filter H(s) acts like a differentiator. For a SYNC rate of 500 kHz, the corner frequency W will be: ND1 | ND0 — W/2π (kHz) 00 — 39.8 01 — 62.5 10 — 85.3 11 — 108
		The actual transfer function from N, Q, to FV1 is: $H(z) = \frac{-100(z-1)}{z[7(z-1)+(3.5+2ND)z]} \frac{\sin(\omega T/2)}{\omega T/2}$ where: $T = 1/FSYNC$, $z = e^{sT}$ This transfers function is approximated throughout this data sheet with an s domain approximation that is accurate for f< .05 • FSYNC.
5-7	unused	

REGISTER DESCRIPTION (Continued)

WINDOW Address 4 Read/Write

WINDOW CONTROL - This register is used to program the on-track window comparator and also contains several control bits.		
BIT	**NAME**	**DESCRIPTION**
0-2	NW0-NW2	WINDOW SELECT BITS - This 3 bit word selects the window comparator threshold voltage. The on track indicator bit will be true as long as: $\|FP1 - VREF\| < VREF[(1 + NW)/32]$ where NW is an integer from 0 to 7.
3	unused	
4	T/S	TRACK/SEEK MODE SELECT - When this bit is set, track mode is selected and when it is reset, seek mode is selected.
5	DUMP	POSITION LOOP FILTER DUMP CONTROL - When this bit is set, pins FP3 and FP4 are switched together internally by S1. This causes the external position loop filter feedback capacitor to be discharged.
6	unused	
7	CAL	CALIBRATION MODE - When this bit is reset, the N and Q inputs are connected to the position processor and normal operation occurs. When CAL is set, the processor inputs are connected to VREF, causing the FP1 output to reflect the offset voltage errors in the position sensing path.

STATUS Address 5 Read/Write access as noted

STATUS REGISTER - Contains track status information and several control bits.		
BIT	**NAME**	**DESCRIPTION**
0	TRKCS	TRACK CROSSING INDICATOR - The function of TRKCS is determined by the CSMOD bit in this register. When CSMOD is set, TRKCS will be set every time NQ or $N\overline{Q}$ change state (ie. on every track crossing). When CSMOD is reset, TRKCS will be set every time NQ changes state (ie. on alternate track crossings). TRKCS is reset every time STATUS is read by the microprocessor. The $\overline{INT}$ interrupt output is the inverse of TRKCS. (TRCKS is read only.)
1	$N\overline{Q}$	TRACK QUADRANT - This bit is set when: N-VREF > VREF-Q and reset otherwise. ($N\overline{Q}$ is read only)
2	NQ	TRACK QUADRANT - This bit is set when: N-VREF > Q-VREF and reset otherwise. (NQ is read only)

REGISTER DESCRIPTION (Continued)

BIT	NAME	DESCRIPTION
3	ONTRK	ON TRACK INDICATOR - This bit is set when the voltage on pin FP1 is within the window selected by the WINDOW register. It is reset otherwise (ONTRK is read only).
4	FRFMT	FRAME FORMAT - Used to indicate the relationship between CLOCK and SYNC. If this bit is set, the VCO clock rate must be 32 times the SYNC clock rate. If it is reset, the VCO clock rate must be 72 times the SYNC clock rate. (FRFMT is read/write).
5	CSMOD	CROSSING INDICATOR MODE - If this bit is reset, TRKCS will be set on alternate track crossings. If it is set, TRKCS will be set on every track crossing. (CSMOD is read/write).
6	ACCIN	ACCELERATION INPUT CONTROL - When this bit is set, the FV3 and FV2 inputs are connected internally. This allows motor current feedback to be switched in and out of the velocity loop under microprocessor control. (ACCIN is read/write).
7	ERSGN	ERROR VOLTAGE SIGN - This bit is set when: EOUT-VREF < 0 and reset otherwise. It is used to determine the sign of the offset voltage during calibration. (ERSGN is read only.)

OFFSET Address 6 Read/Write

OFFSET VOLTAGE REGISTER - The 8-bit value in this register drives the offset DAC which adds a correcting voltage to the position error signal.

BIT	NAME	DESCRIPTION
0-6	NOS0-NOS6	OFFSET MAGNITUDE
7	SOS	OFFSET SIGN

The offset correction voltage, VOS, is given by:

$$VOS = -0.89 \left(\frac{NOS}{127}\right) V, \quad SOS=0$$

$$0.89 \left(\frac{NOS}{127}\right) V, \quad SOS=1$$

RESET Address 7 Write only

RESET REGISTER - When any value is written to this register, all writeable register bits in the SSI 32H568 are reset.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

(Maximum limits indicate where permanent device damage occurs. Continous operation at these limits is not intended and should be limited to those conditions specified in the DC operating characteristics.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VPA		0		14	V
Voltage on any pin		0		VPA+0.1V	V
Storage Temp.		-45		165	°C
Solder Temp.	10 sec duration			260	°C

RECOMMENDED OPERATION CONDITIONS (Unless otherwise noted, the following conditions are valid throughout this document.)

VPA, VPD		10.8		13.2	V
VDD		4.5		5.5	V
VREF		5.1	5.4	5.7	V
Operating temp.		0		70	°C
RBIAS, bias resistor to AGND		22.3	22.6	22.9	KΩ

DC CHARACTERISTICS

IVP	Total VPA and VPD current				40	mA
IDD	VDD current				10	mA
IREF	VREF current				3	mA

DIGITAL I/O

Digital Inputs					
VIH	|IIH|<10uA	2			V
VIL	|IIL|<10uA			0.7	V
Digital Outputs (AD0-AD7, T/$\overline{S}$)					
VOH	|IOH|<40uA	2.4			V
VOL	|IOL|<1.6mA			0.4	V
Open Drain Digital Outputs ($\overline{INT}$, $\overline{OFFTRK}$)					
VOL	|IOL|<1.6mA			0.4	V
Off leakage	VOH = VPD			10	µA

MICROPROCESSOR INTERFACE TIMING (see figure 4(a) and figure 4(b)). (Timing measurements for digital signals are measured at 1.3V, unless otherwise noted.)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
TLHLL	ALE pulse width		45			ns
TAVLL	Address setup time		8			ns
TLLAX	Address hold time		20			ns
TRLVD	$\overline{RD}$ to data valid				145	ns
TRHDX	data hold time after $\overline{RD}$		0		50	ns
TRLRH	$\overline{RD}$ pulse width		200			ns
TLLWL	ALE to $\overline{RD}$ or $\overline{WR}$		25			ns
TRLCL	$\overline{RD}$ or $\overline{WR}$ to $\overline{CS}$ low				20	ns
TRHCH	$\overline{RD}$ or $\overline{WR}$ to $\overline{CS}$ high		10			ns
TWLWH	$\overline{WR}$ pulse width		100			ns
TQVWH	data set up to $\overline{WR}$ high		70			ns
TWHQX	data hold after $\overline{WR}$ high		10			ns

ANALOG I/O

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
N, Q Inputs						
Input resistance			50			KΩ
Input capacitance					25	pF
Offset voltage			-15		15	mV
Common mode range		About VREF	4			V
N, Q Timing (see figure 5)						
Fc	VCO input frequency		4		16	MHz
TSKW	SYNC skew		0		6	ns
TSYNC	SYNC pulse width		40			ns
Nc	VCO/SYNC	FRFMT=1	32		32	
	frequency ratio	FRFMT=0	72		72	
TADS	N or Q analog setup time		260			ns
TADH	N or Q analog hold time		180			ns

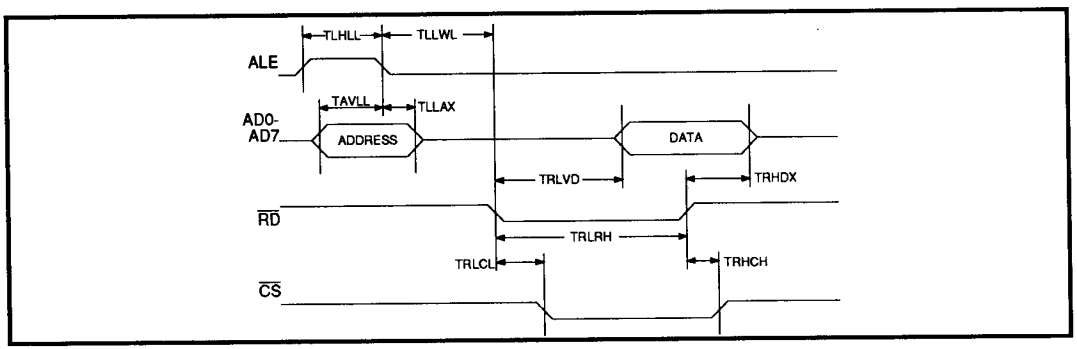

FIGURE 4(a): Read Cycle Timing

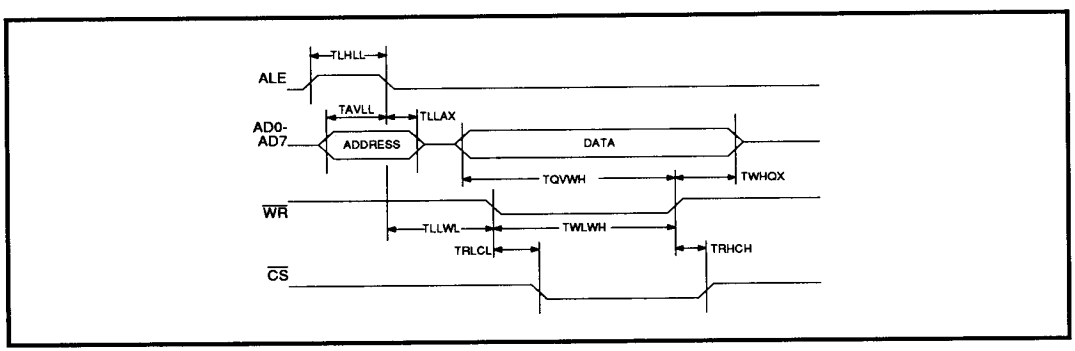

FIGURE 4(b): Write Cycle Timing

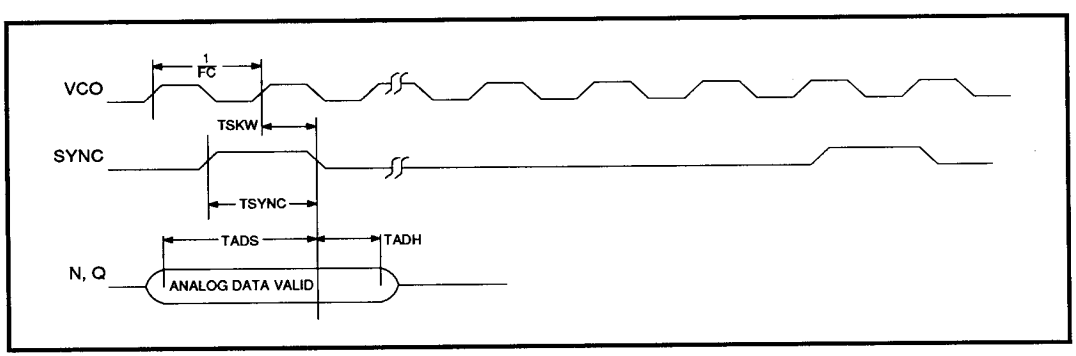

FIGURE 5: Analog Timing

ANALOG I/O (Continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
FP2, FV2, FV3 Inputs					
Input resistance	About VREF	100			KΩ
Input capacitance				20	pF
Offset voltage		-15		15	mV
Switch resistance (S1, S2)				100	Ω
Analog Outputs					
Output impedance	|Vo-VREF|<3V			20	Ω
Resistive loading	About VREF	5			KΩ
Capacitive loading				40	pF
Output swing (FP1, FV1)	About VREF	4			V
Output swing (FP3, FV4)	About VREF	3.5			V
Output swing (EOUT)	About VREF	3.7			V
Gain (FP1 from N or Q)		9.45	9.55	9.65	dB
Gain (Amplifier A1, A3)	Open loop DC gain	66			dB
Gain (Amplifier A2)		-0.1		0.1	dB
Unity gain bandwidth (Amplifier A1, A3)	Open loop	1			MHz
Unity gain bandwidth (Amplifier A2)	Open loop	0.5			MHz

WINDOW COMPARATOR

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Threshold step size accuracy	Nominal=VREF/32	-30		30	%

FILL GAIN

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum gain	NFG=15	58	59	60	mV/V
Gain step size		3	4	5	mV/V

VELOCITY GAIN

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum gain	NVG=15	.98	1	1.02	V/V
Gain step size		48	67	82	mV/V

TARGET VELOCITY DAC

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Full scale/VREF	VELPOL=1	1.72	1.75	1.78	V/V
	VELPOL=0	.22	.25	.28	V/V
Step size/VREF		1.9	2.9	3.7	mV/V
Offset Match	TARGET=0 VELPOL=0, 1			20	mV

OFFSET CORRECTION DAC

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Full scale/VREF	NOS=127, SOS=1	.15	.16	.18	V/V
	NOS=127, SOS=0	-0.15	-0.16	-0.18	V/V
Step size/VREF		.83	1.3	1.76	mV/V

DIFFERENTIATOR

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
High pass gain		13.7	14.3	14.9	V/V
Corner frequency	FSYNC = 500 KHz				
	ND=0	37.4		42.2	KHz
	ND=1	57.3		66	KHz
	ND=2	81.2		89.9	KHz
	ND=3	102.7		113.8	KHz

APPLICATIONS INFORMATION

In the example shown in figure 7, the SSI 32H568 is used with its companion devices, the SSI 32H567 and SSI 32H569, as well as a microprocessor and some external components, to implement a complete head positioning system.

Position Reference

The position feedback signal for the servo loop is generated by a servo demodulator from information prerecorded on the disk drive's servo surface. The SSI 32H567 provides quadrature position signals (N and Q), recovered clocks (SYNC and VCO) and an analog reference level (VREF) for the rest of the system. The SSI 32H567 translates the radial displacement of the servo read head to a voltage with a gain of 2 volts/track. The SSI 32H568 has a front end gain of 3, so the gain from actual position error to the voltage at pin FP1 (the input to the position loop filter) is 6 volts/track.

In order to produce the position error signal illustrated in figure 6, the position processor in the SSI 32H568 selects either N, Q or an inverted signal, based on the value of the digital signals NQ and $N\overline{Q}$. The resulting error signal is zero (equal to VREF) when the head is perfectly centered on a track. The error signal has a maximum absolute value in the vicinity of a track boundary (ie. when the head is displaced one half track from a track center) and has a polarity that indicates the direction of the position error.

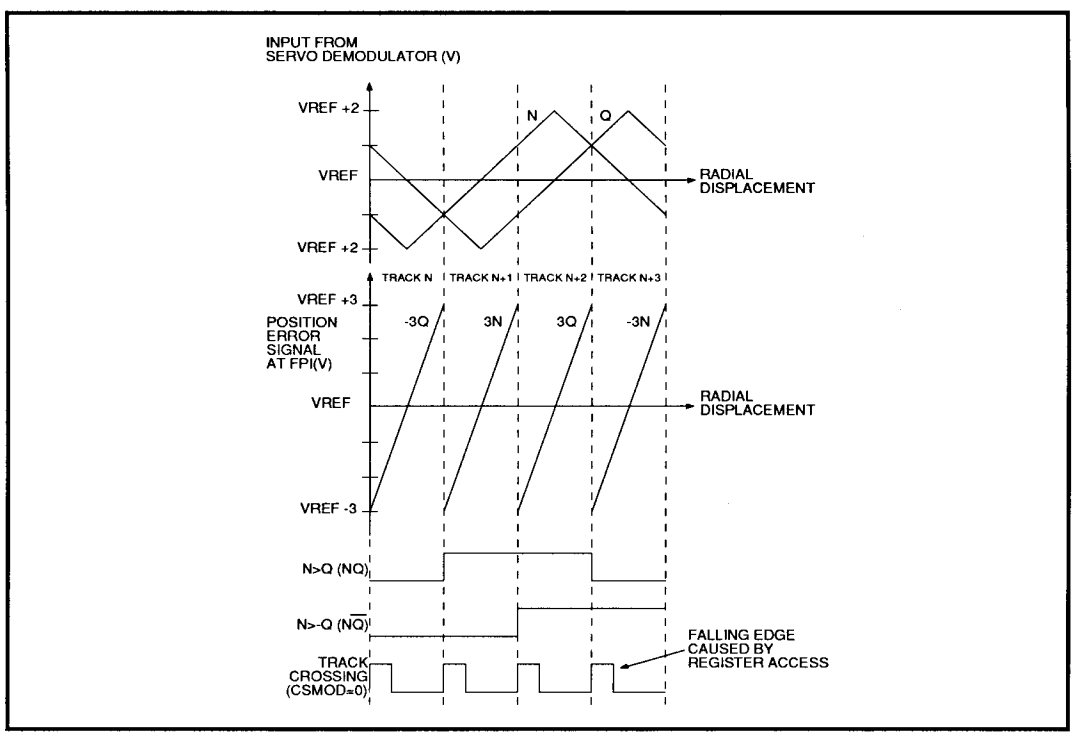

FIGURE 6: Position Signal Waveforms

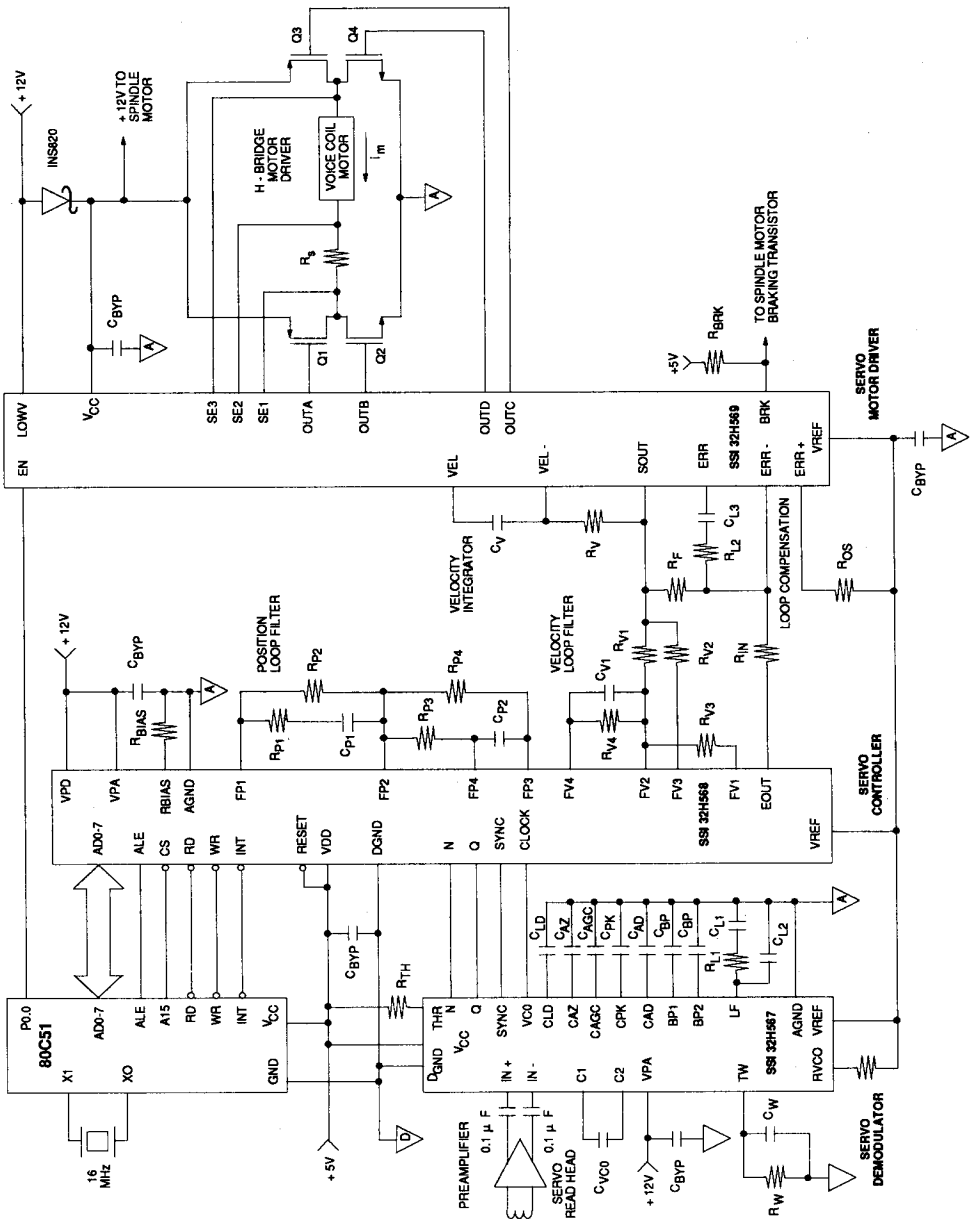

Figure 7: Complete Example Of Servo Path Electronics Using SSI 32H567/568/569 Chip Set

Servo Motor and Driver

For the purposes of illustration, the following simple model for the servo motor in figure 7 is assumed.

$$i_m = \frac{J\theta}{K_m} \cdot \frac{d\omega}{dt} \quad e = K_e \cdot \omega$$

Definition of terms:

im	Armature current (A)
ω	Motor speed (rad/s)
Jθ	Rotor moment of inertia (kg • m²)
Km	Torque constant (N - m/A)
e	Motor back EMF (V)
Lm	Winding inductance (H)
Rm	Winding resistance (Ohm)
Ke	Motor voltage constant V/rad/s

Numerically Ke and Km are equal

Under the assumption that the electrical and mechanical poles of the motor above are widely separated ($Rm/Lm >> J\theta \cdot Rm/Km^2$), the servo driver loop compensation components, R_{L2} and C_{L3}, may be chosen to cancel the effect of Lm, as follows:

$$C_{L3} = \frac{68\,R_S}{2\pi R_F (R_m + R_S) BW}, \quad R_{L2} = \frac{L_m}{C_{L3}(R_m + R_S)}$$

where BW is the desired servo driver open loop bandwidth (Hz). This results in the following relationship between motor current (im) and error voltage at the servo controller output (EOUT).

$$\frac{i_m}{EOUT}(s) = \frac{-R_F}{4\,R_{in}\,R_S\left(1 + \frac{s}{2\pi BW}\right)}$$

This simple first order approximation of the servo motor behaviour neglects effects such as resonance due to the motor inductance, Lm, or the pole due to servo driver transconductance. However, it is sufficient to illustrate the design goals for the velocity and position loop filters that are required with the SSI 32H568. A more detailed description of the SSI 32H569 may be found in the SSI 32H569 data sheet.

TRACK MODE

Loop Compensation

Track mode is engaged when the head has reached its destination and the current position must be maintained. The control objective is to drive the position error signal at FP1 to zero and minimize excursions of the head due to noise and other perturbations of the system. The transfer function of the complete servo loop in track mode is shown in figure 8(a), using the servo motor model derived above. The gain G_1 is the combined effect of the SSI 32H567 and the front end gain of the SSI 32H568, and has a nominal value of 6 volts/track. The gain G_2 is a property of the head transport system, and has units of tracks/radian for rotary servo motors and tracks/meter for linear motors. (The nomenclature chosen for the motor model is that of rotary motors but the results are applicable to linear motors as well, if appropriate units are substituted). To ensure that the control loop has negative feedback, positive motor current (as indicated in figure 7) must result in negative motor acceleration. This inversion is accomplished in the prerecorded servo pattern and is accounted for in the transfer function by showing G2 to be negative.

Since the servo driver/motor combination has a double pole at the origin and an additional real pole at frequency BW (which is selectable with external components in the SSI 32H569), the position loop filter is essential to ensure a stable system. The effect of the position filter used in this example is to provide lag-lead compensation. Systems of this type are usually designed by trial and error, but a further simplification of the transfer function may be made to obtain an initial solution. If the pole at BW is ignored, RP4 is removed and RP2 made large (RP2 is necessary to provide a DC path for leakage current at pin FP2) then the system illustrated in figure 8(b) is obtained. The compensation has been reduced to lead compensation only. If the following quantities are defined:

$$Gtot = \left(\frac{G_1 G_2 C_{P1}}{C_{P2}}\right)\left(\frac{R_F}{4\,R_{In}\,R_s}\right)\left(\frac{K_m}{J\theta}\right)(s^{-2})$$

PM = Desired closed loop phase margin (degrees)

FB = Desired open loop unity gain bandwidth (rad/s)

then appropriate values for the time constants of the lead compensation circuit (T_1, T_2) may be chosen using the following relationships, assuming $1/T_2 << FB << 1/T_1$:

$FB = Gtot \cdot T_2$ (rad/s)

$PM = 90 - \arctan(FB \cdot T_1)$ (degrees)

The values for T_1 and T_2 thus chosen form a starting point for the selection of appropriate values for the more complex lag-lead compensator required by the real system.

Position Loop Filter Initialization

Switch S1, which is controlled by the DUMP bit in the WINDOW register, may be used to short out the external feedback capacitor C_{P2}, discharging it. S1 is usually closed during seek a operation, so that when the system is switched to track mode no sudden transients occur due to charge stored on C_{P2}. Disturbances to the position signal when the system is switching to track mode can greatly extend the disk drive's access time, since the system response is much slower in this mode.

Offset Cancellation

The position error path in the servo loop is DC coupled and can be affected by offset voltages internal to the SSI 32H568, especially during a transition from seek to track mode. The following procedure may be used to cancel out any offsets in the position error path:

1) Set T/$\overline{S}$. (Enter track mode).
2) Set both the CAL and DUMP bits. (This switches the N and Q inputs to VREF and shorts out C_{P2}).
3) Set NOS=0. (This sets the offset DAC magnitude to zero).
4) Copy the ERSGN bit to SOS. (If the offset causes EOUT to be negative, then it is necessary to make

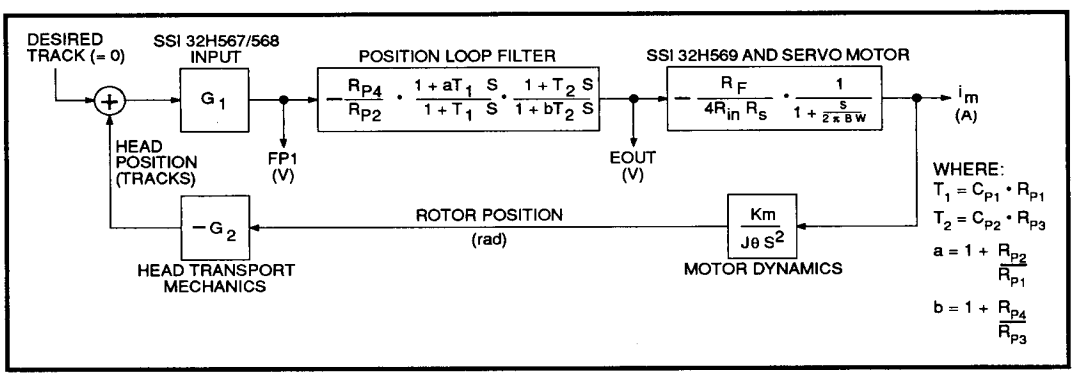

FIGURE 8(a): System Transfer Function In Track Mode

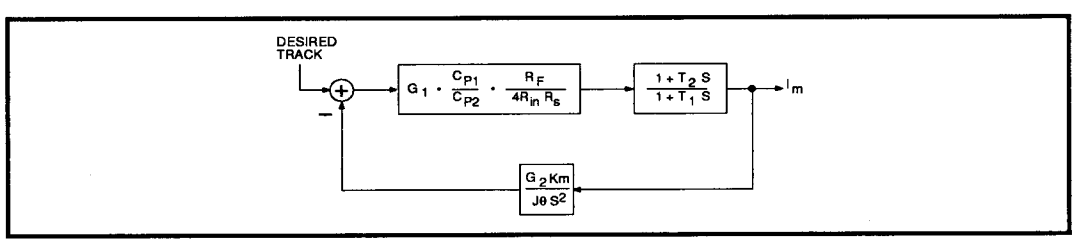

FIGURE 8(b): Simplified Track Mode Transfer Function

the input of inverting amplifier A1 more negative, and vice versa).

5) Increase NOS in steps of one LSB until ERSGN changes sign. At this point the position error offset will have been cancelled to the greatest extent possible.
6) Clear both DUMP and CAL to resume normal track mode operation.

On Track Window

The on track window comparator may be used to monitor the positioning accuracy of the head. The position error voltage at pin FP1 is compared to a signal selected by the bits NW0-2 in the WINDOW register. The ONTRK bit in register STATUS is set if the position error is within the specified limits and cleared if it is outside the limits (in either the positive or the negative direction). The programmable excursion limits (expressed as a percentage of a track) range from 2.8% to 22.5% in 8 equal steps. By monitoring the ONTRK bit, the microprocessor can determine when the head has settled sufficiently for read and write operations to commence. The ONTRK bit may also be used to decide when it is appropriate to switch from seek to track mode at the end of a period of decceleration.

SEEK MODE

Velocity Profile

The velocity profile that results in the shortest seek time, subject to motor current and head velocity limitations, is as follows:

1) Maximum acceleration (maximum motor current) until the half-way point or maximum velocity is reached.
2) Constant velocity motion until it is time to commence decceleration (if maximum velocity was reached).
3) Maximum decceleration until head comes to rest over the destination track. The decceleration period is of approximately the same duration as the acceleration period.

The microprocessor computes a velocity profile according to the rules above, based on the current head location and destination track. During the final approach to the destination track, updates to the velocity DAC become more infrequent since the track crossing rate is approaching zero. The fill signal which is derived from the position error can be used to provide a smooth target velocity profile between track crossing updates.

Figure 9 shows a set of typical waveforms as the head approaches the destination track. The fill gain is adjusted at each track crossing so that the fill signal interpolates smoothly between target DAC settings. In the destination track, where the target DAC output is zero, the fill signal is especially important, since it becomes zero only when the head is centered on the track. The velocity control loop thus causes the head to come to rest at the center of the destination track.

Loop Compensation

The transfer function for the controller electronics of figure 7 is shown in figure 10(a). This transfer function may be simplified as shown in figure 10(b), under the following conditions:

$$\omega^2 >> \frac{(GG_1G_2)(K_m R_X)}{J\theta R_{V3}}$$

$$R_{V4} C_{V1} = \frac{J\theta \omega R_{V3}}{(GG_1G_2)(K_m R_X)}$$

where Rx is RV1 (ACCIN=0) or RV1//RV2 (ACCIN=1)

The value of ω, the corner frequency of the internal position differentiator, is dependent on the sync rate, but the above condition is generally satisfied by most systems. The condition on RV4 and CV1 sets the position of the zero due to the external components in the velocity loop filter, whose function is described below. The resulting system has two real poles, one of which is at the origin, and is thus unconditionally stable.

The position of the SSI 32H568 internal differentiator pole is selectable under microprocessor control. It is desireable to select as low a frequency as is consistent with the required seek performance. This pole prevents the differentiator from amplifiying high frequency noise. In order to provide feedback of a velocity signal for frequencies above the differentiator pole, the external velocity loop filter is configured to act as an integrator which integrates the motor current sense output of the SSI 32H569, SOUT. Since SOUT is proportional to motor acceleration, this integration produces a signal proportional to velocity. Thus, at low frequencies the velocity feedback is generated by differentiating the position error signal and at high frequencies, the velocity term results from integrating motor current. It is more accurate to estimate velocity from a direct observation of head position, but at higher frequencies it is necessary to provide increased noise immunity. The system described above balances these two considerations.

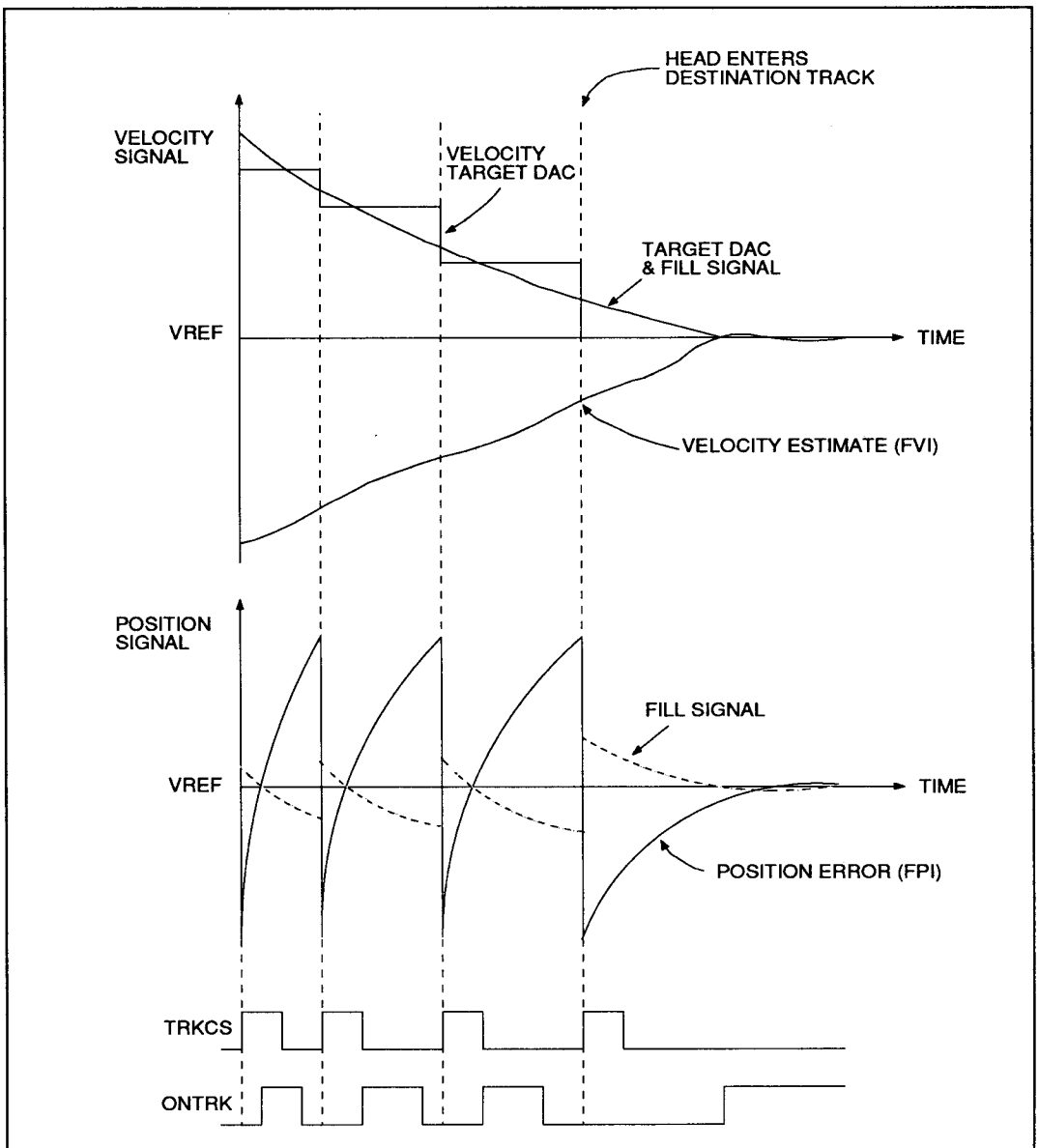

FIGURE 9: Typical Waveforms During Final Deceleration Mode

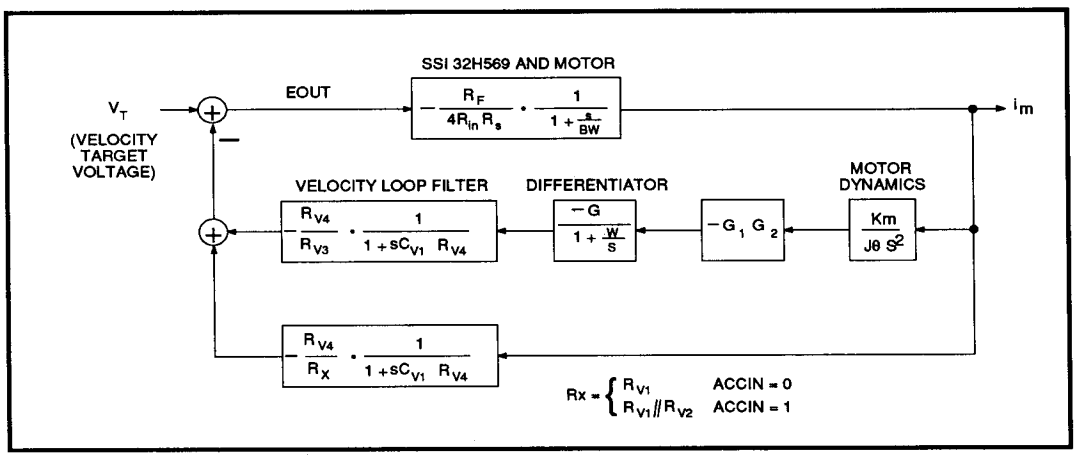

FIGURE 10(a): Transfer Functions of SSI 32H568 In Seek Mode

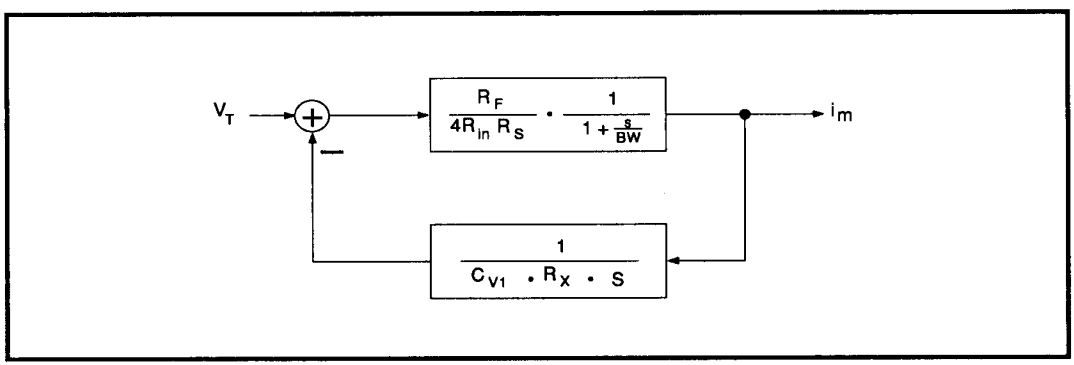

FIGURE 10(b): Simplified Transfer Function of SSI 32H568 In Seek Mode

$$\omega^2 >> \frac{(GG_1G_2)(K_m R_X)}{J\theta R_{V3}}$$

$$R_{V4}C_{V1} = \frac{J\theta \omega R_{V3}}{(GG_1G_2)(K_m R_X)}$$

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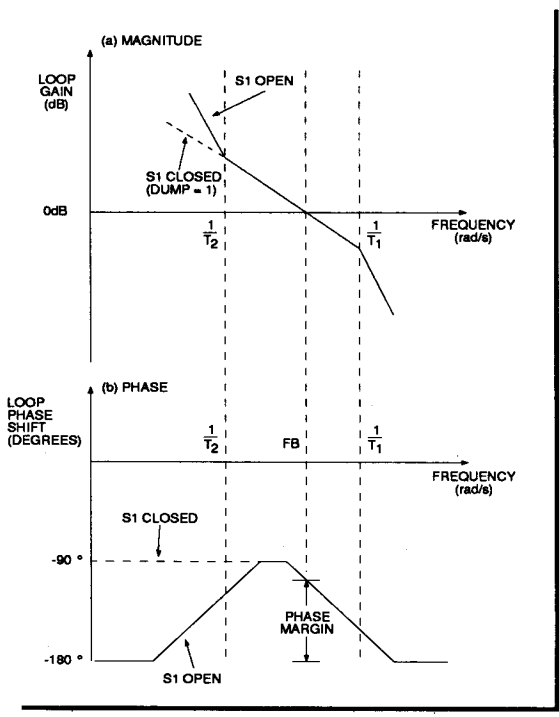


FIGURE 11: Bode Plot of Simplified Track Mode Transfer Function

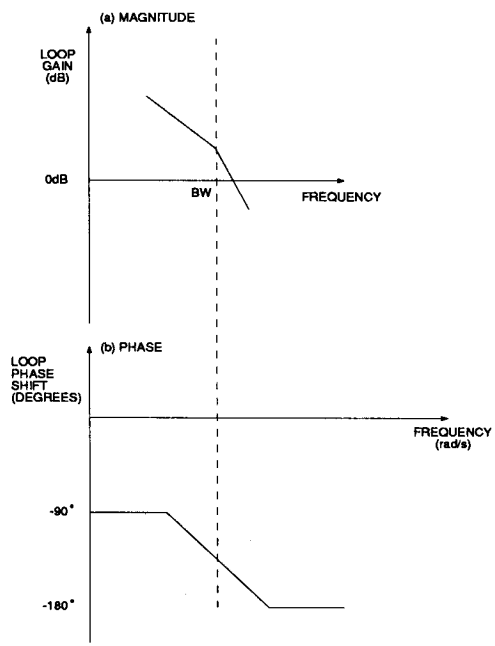
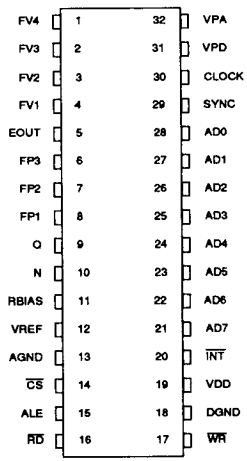


FIGURE 12: Bode Plot of Simplified Seek Mode Transfer Function

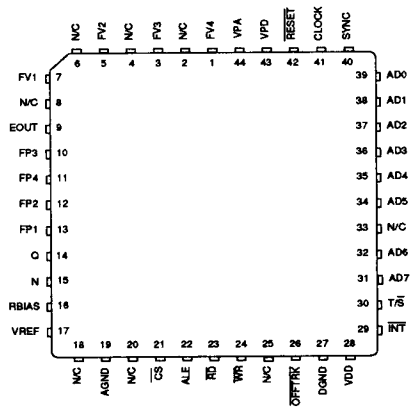
SSI 32H568
Servo Controller

PACKAGE PIN DESIGNATIONS
(TOP VIEW)

CAUTION: Use handling procedures necessary for a static sensitive component.



32-Pin DIP



44-Pin PLCC

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32H568, Servo Controller		
32-Pin DIP	SSI 32H568-CP	32H568-CP
44-Pin PLCC	SSI 32H568-CH	32H568-CH