Features

- Complete 2.4GHz High performance Radio Transceiver
- No external trimming is required in production
- Bluetooth wireless technology, 2.4 GHz license-free band
- Compliant to the Bluetooth™ specification v1.1
- Bluetooth Class 2, 3 Level Output Power
- High Receive sensitivity -85 dBm typ.
- Communications of up to 10m range in free space
- Frequency Hopping Spread Spectrum (FHSS) with Gaussian Frequency Shift Keying (GFSK)
- Transmission scheme TDD – time division duplex.
- Frequency 2402 to 2480 MHz
- Channel intervals 1 MHz
- Number of channels 79 CH
- Symbol rate 1M symbol/s
- Compliant to FCC, CE, ETSI and other countries' EMI standards
- Very good data quality--tolerates blocking by other services
- Internal 16MHz crystal and clock oscillator
- Integrated RF bandpass filter
- SPI interface for installing and configuring the module
- Low Power standby modes to enable very efficient power management
- Available for either external antenna or internal patch_antenna
- Power supply voltage 2.7 V and 3.3V
- Operation Temperature: 0 ~ 40°C
- Small size, lightweight, size 33mm X 20mm X 1.5mm
- Available in small quantities

Application

- Laptop and Desktop PCs
- Computer Accessories (Compact Flash, PCMCIA and SD cards)
- Cordless game controllers
- Printers, FAX, WebPAD
- Personal Digital Assistants (PDAs)
- Cordless Headsets
- Digital camera
- USB Dongle /RS232 adaptor
- And many other computer peripherals or embedded devices applications, including wireless keyboard, mouse, joystick etc.

General Descriptions

The PT8R2401 is well suited to applications that fall within the 2.4 GHz radio spectrum designated as Industrial, Scientific and Medical (ISM).

Transmission scheme TDD – time division duplex. Spreading type FHSS – frequency hopping spread spectrum. Number of channels 79. Channel intervals 1 MHz [(f = 2.402 + k) GHz, k = 0,1,2,…78]. Hop rate 1.6k hops/second. Modulation Method GFSK 0.5BT Gaussian. Support point-to-multipoint functionality.

The PT8R2401 control interface consists of a data interface and a control interface for transmitting and receiving data, and a serial interface for programming the internal registers of the PT8R2401.

There are two subsections of the interface:
• RF data and control path
• Register control interface (serial).

Six signals are used in the RF data and control path (TXDATA, RXDATA, TXACTIVE, RXACTIVE, TXDATA_EN, SYNCDETECT). Four in the serial register control interface (TDI, TDO, TMS, TCK), one system clock (DATACLK) and one reset signal (RET). All of the signals are unidirectional.

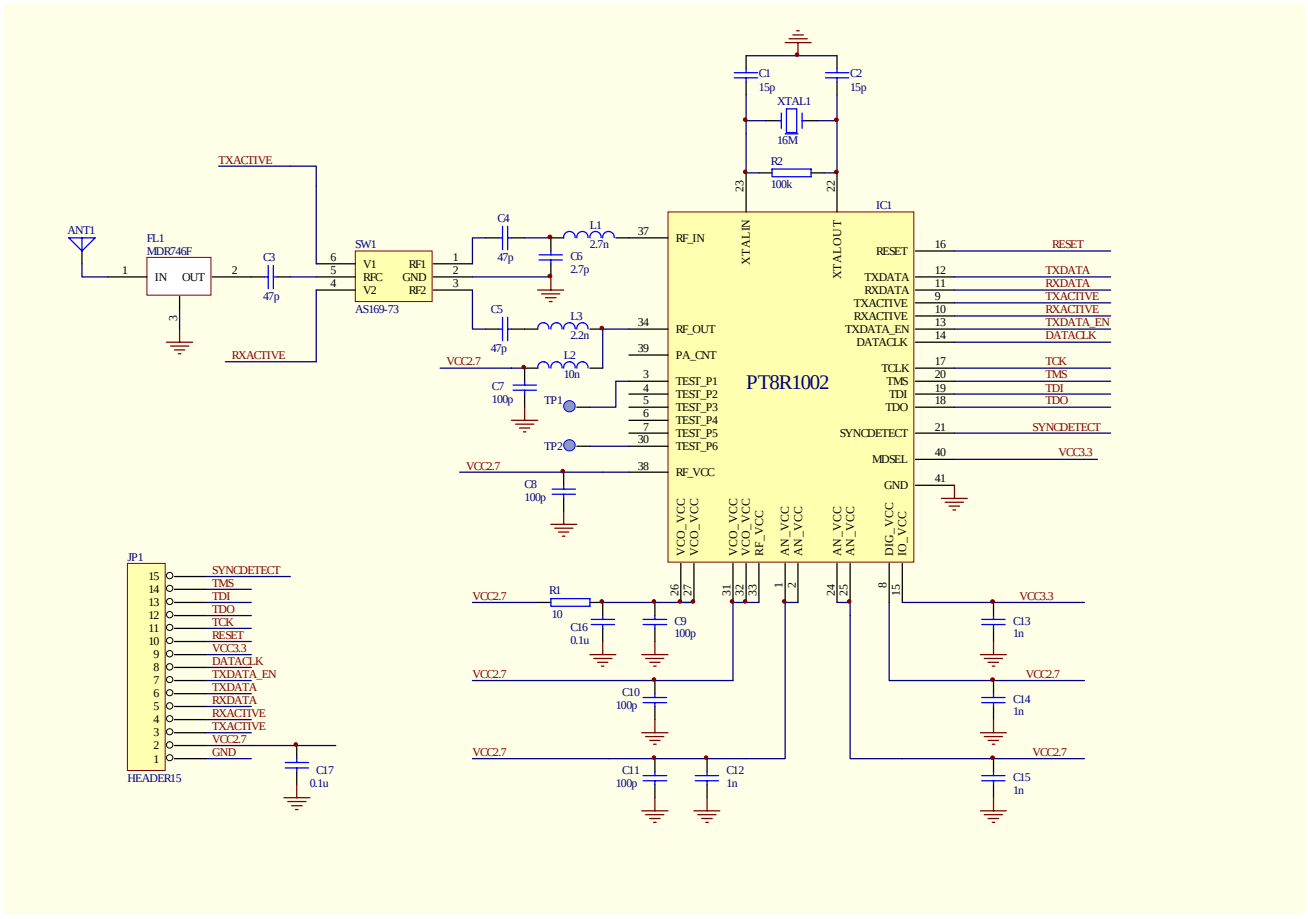
Standard PT8R2401 has built-in antenna. Option PT8R2401N has no built-in antenna. Customer can use external antenna.

These modules can be integrated into almost any radio electrical device for wireless data communications, including PDAs, mobile phones, laptop computers, and game pad devices.

Ordering Information

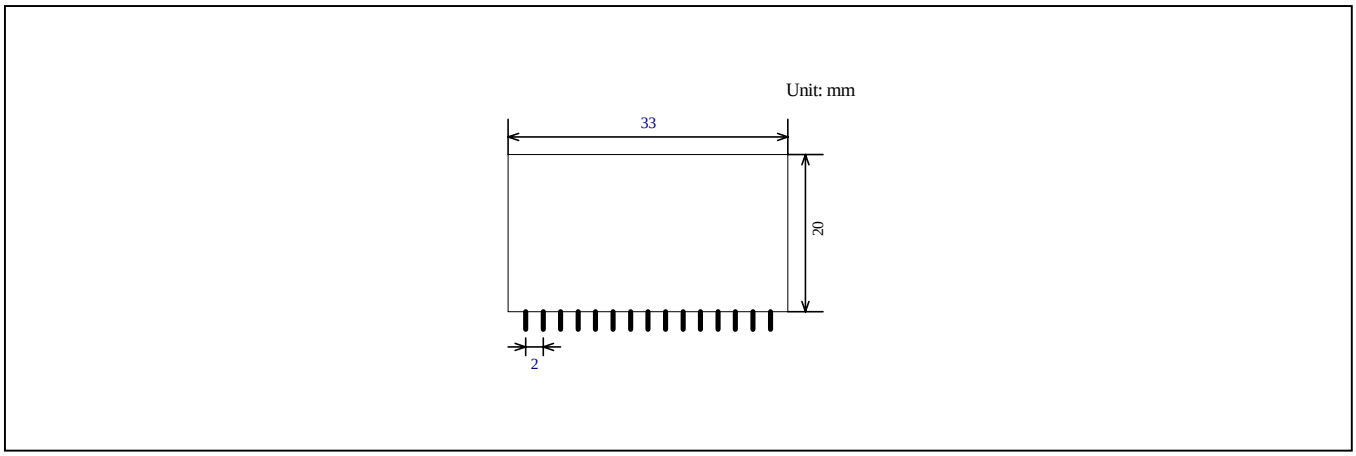
Device	Description		Order Number
	Type	Size	
PT8R2401	Have built-in antenna	33X20X1.5 (mm)	**PT8R2401MD**
PT8R2401N	No built-in antenna	33X20X1.5 (mm)	**PT8R2401MD**

Block Diagram



Pin Information

Package Diagram



Size 33X20X1.5 (mm)

Pin Descriptions

Pin	PIN Name	TYPE	Description
1	GND	Power	GND
2	VCC2.7	Power	2.7V Power Supply
3	TXACTIVE	I	Transmitter enable
4	RXACTIVE	I	Receiver enable
5	RXDATA	O	Receive data
6	TXDATA	I	Transmit data
7	TXDATA_EN	I	Timing reference of valid data
8	DATACLK	O	Reference data clock
9	VCC3.3	Power	3.3V Power Supply
10	RESET	I	Reset
11	TCK	I	A serial register interface clock
12	TDO	O	Phy control register serial data output
13	TDI	I	Phy control register serial data input
14	TMS	I	Control signal of Phy's TAP controller
15	SYNCDETECT	I	Indication of SYNC word detection

I/O Description

RF interface

The radio interface establishes the connection of antenna-to-LNA in receiving mode and antenna-to-power amplifier in transmitting mode. An antenna filter is located between the antenna and SPDT (Single Pole Double Throw) switch. The antenna filter blocks unwanted signals in receive mode and suppresses harmonics in the transmit mode. The filter can be either a discrete component or fully integrated in ceramic substrate. The SPDT switch isolates the transmit path and the receive path and thus impedance can be matched for entire signal path. A matching circuit is placed between LNA_IN pin and SPDT switch to match the 50 ohm source to the complex input impedance of the LNA. Another external matching circuit is required at PA_OUT to transfer maximum power to the antenna.

Unidirectional interface

The interface connections for unidirectional mode are shown as follows: the unidirectional interface can be split into two subsections: RF data and control path, register control interface. In RF interface, ten signals are used in the RF data and control path, and four in the register control interface.

All of the signals are unidirectional.

The unidirectional interface requires that the PT8R2401 control registers interface to the Baseband via an IEEE 1149.1 JTAG interface. The unidirectional interface requires that the Baseband portion of the interface is referenced to a Baseband generated clock.

Transmit Operation In Unidirectional Interface

The primary signal for data transmit is TXACTIVE signal. The actual data transmission starts after TXDATA_EN provided by baseband. During transmit mode,

DATACLK is sent from PT8R2401 to baseband as a timing reference. The baseband circuit transmits data to the PT8R2401 at the falling edge of DATACLK, whereas the PT8R2401 latches the data at the rising edge of DATACLK.

The state of PT8R2401 transits from the **idle state** when the baseband drives TXACTIVE HIGH. TXACTIVE enables all the transmit circuitry except for the final output stage. TXACTIVE is driven high at a time $T_{TuningTX}$ before the hop frequency synthesizer has settled to allow any frequency offsets caused by the TX circuitry to be eliminated. Either when, or just before, the TX circuitry has correctly settled on frequency, the baseband drives TXDATA_EN HIGH, which enables the PA stage, and causes the unidirectional interface to enter the **transmit data state**. The baseband drives data to the PT8R2401 on the falling edge of DATACLK, and the PT8R2401 reads the transmit data on the rising edge. When all the data has been transmitted, the baseband drives TXDATA_EN and TXACTIVE LOW to disable the PA stage and return to the **idle state**.

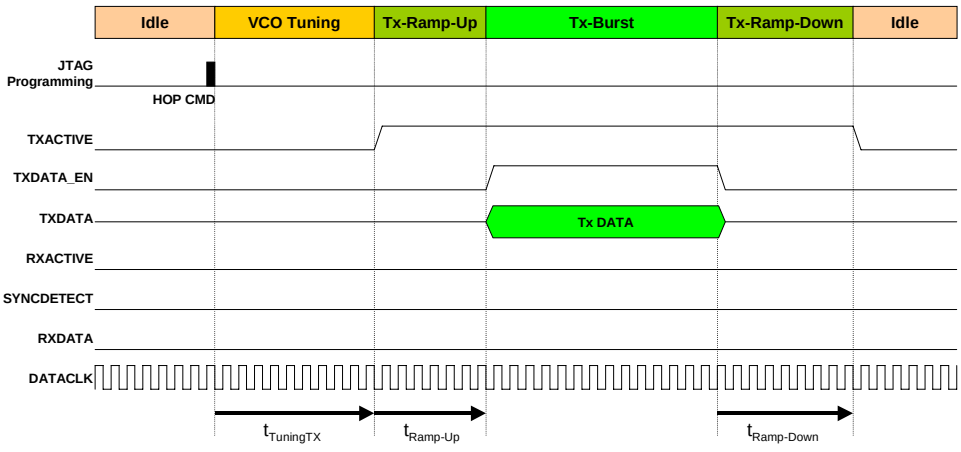


Figure 2. Transmit procedure timing diagram in unidirectional interface

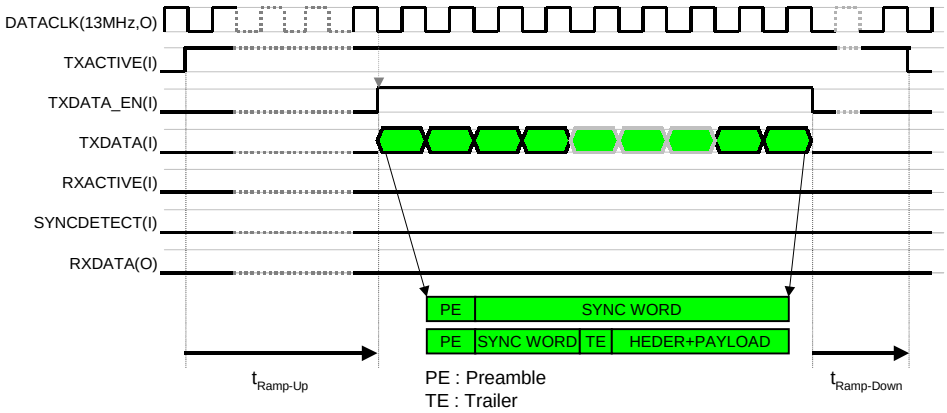


Figure 3. Transmit signal timing diagram in unidirectional interface

Receive Operation In Unidirectional Interface

The primary signal for data reception is RXACTIVE signal. When RXACTIVE goes to high, the RF circuitry starts to operate and send data after fixed time from RXACTIVE. The baseband receives data and searches for the access code. During receive mode, DATACLK is sent from PT8R2401 to baseband as a timing reference. The PT8R2401 circuit sends the data to baseband at the rising edge of DATACLK, where the baseband latches the data at the falling edge of DATACLK. Prior to receiving information over air, the baseband transfers control information including the hop frequency over the JTAG interfaces, and enters PT8R2401 into **search access code state** after fixed time to turn on receiver circuitry by driving RXACTIVE HIGH. In the **search access code state**, the baseband performs all of the tasks required to correlate with the access code from the receive data. When the baseband has correlated the access code, then it drives SYNCDETECT HIGH and makes PT8R2401 enter into **receive payload state**. During the payload, PT8R2401 eliminates any frequency offset between local and remote Bluetooth devices based on its measurement during syncword acquisition. PT8R2401 transmits demodulated data to the baseband at half frequency of DATACLK, which can be read by the baseband using appropriate timing recovery algorithm. The unidirectional interface is returns to the **idle state** with the baseband driving RXACTIVE LOW after a fixed interval of T_{RxOff}.

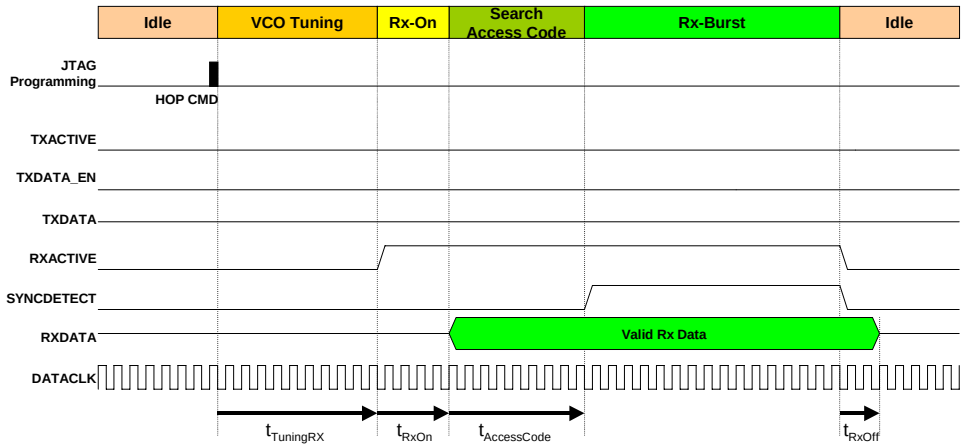


Figure 4. Receiver procedure timing-diagram in unidirectional interface

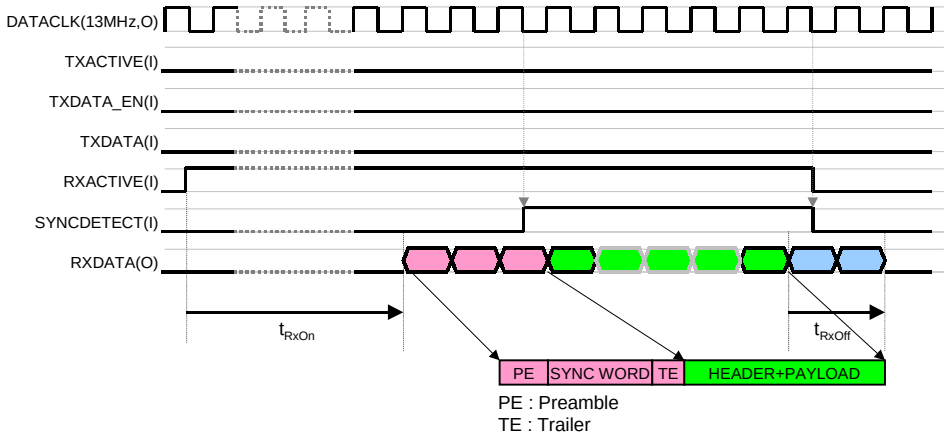


Figure 5. Receiver signal timing diagram in unidirectional interface

Power-Up Sequence

The power-up sequence of PT8R2401 is very simple mechanism. After power is applied to the PT8R2401, the activating RESET signal into LOW for t_{RESET} is the only required operation. After this procedure, PT8R2401 will come into idle mode for waiting transmit or receive operation indicated by Bluetooth baseband. Before this normal operation, all SPI register value should be initialized even though its value is set by the default value. The initialized value will be provided by PTI. After activating RESET signal, 13 or 16MHz baseband reference signal, DATACLK will be activated until execution of external power down command through SPI interface.

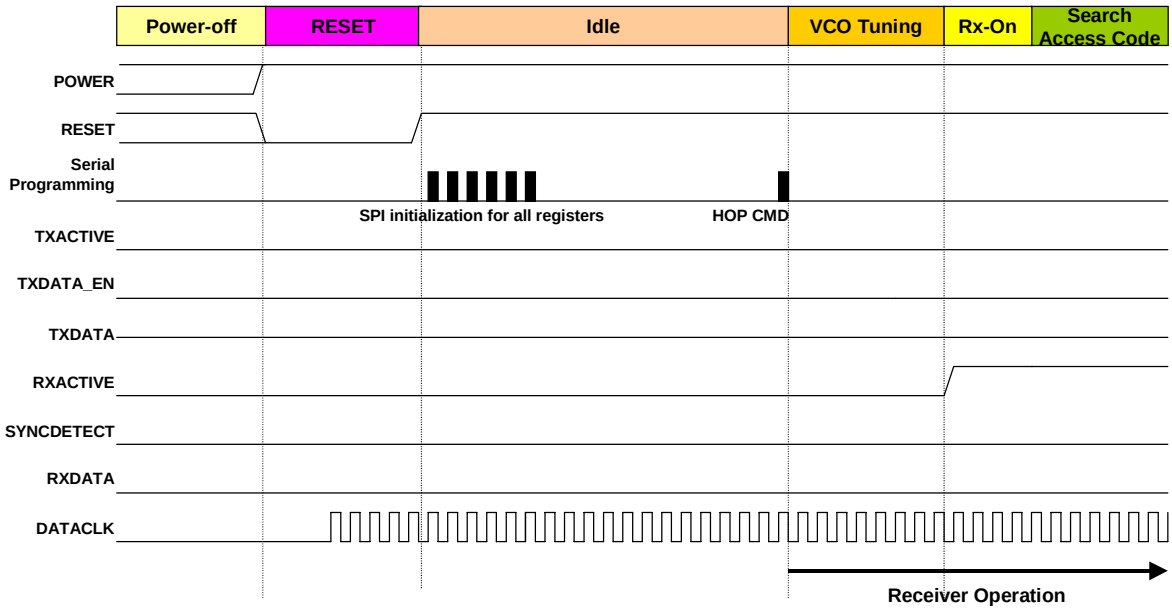


Figure 6. Power-up sequence procedure timing-diagram

Power-Down Sequence

The lowest operation power state of PT8R2401 is **Sleep state**, where all clocks including RF and baseband and circuits in the PT8R2401 is placed in their minimum power mode. In this mode, the control register can be accessed through serial interface logic and retain their programmed value. To enter into **Sleep state**, power-down command which sets power-down of clock generator including crystal buffer should be programmed through the serial interface. After power-down command, the DATACLK from the PT8R2401 will stop until it comes back to **Idle state**. To escape from **Sleep state**, power-up command which sets power-up of clock generator should be programmed through the serial interface. After power-up command, the DATACLK will start again from the PT8R2401 into external baseband.

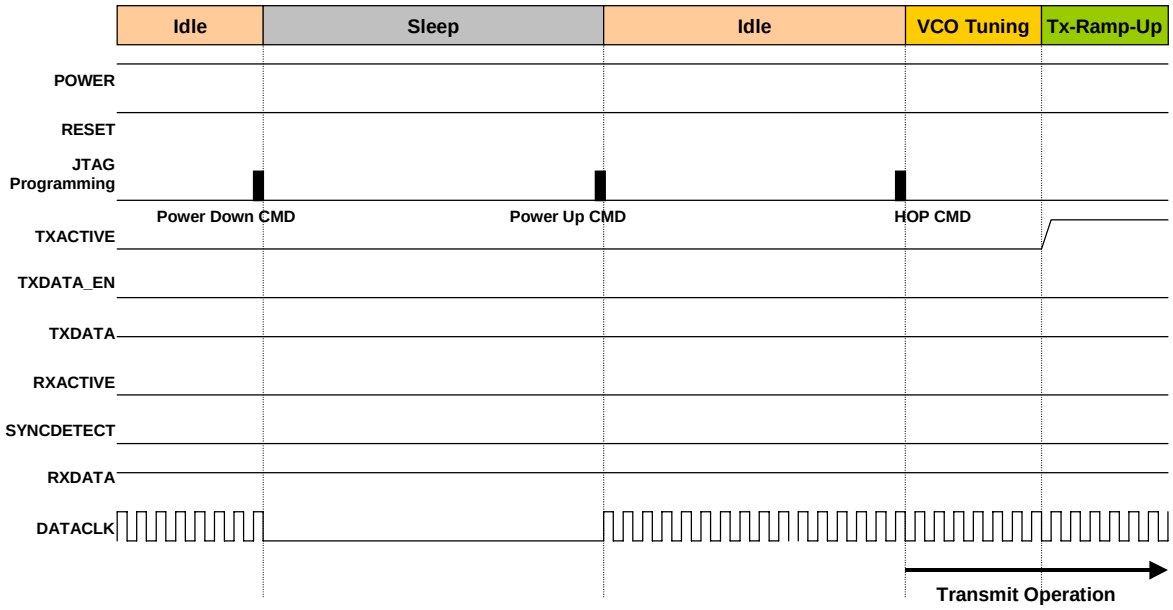


Figure 7. Power-down sequence procedure timing-diagram

Power Control

In the PT8R2401, there are five different states with different current consumption; **Sleep**, **Idle**, **VCO active**, **TX active**, and **RX active**. Upon reset, the PT8R2401 stays in the **Idle state** to wait for the command through serial programming interface from the baseband controller. In the Idle state, there is DATACLK from the radio to the baseband controller. In the **Idle mode**, all RF circuits are shut down to reduce the static current consumption. Only the reference clock oscillator and DATACLK pump to the baseband is active. After HOP set command through the serial programming, the VCO will operate to lock the programmed channel frequency. Owing to the signal such as RXACTIVE or TXACTIVE, the PT8R2401 will enter into the active state such as **TX active state** and **RX active state**. In those state, all RF circuits and GFSK modem will operate and result in the maximum current consumption. In the unidirectional mode, the falling signal of RXACTIVE or TXACTIVE will make the PT8R2401 into **Idle state** automatically. In the bidirectional mode, the explicit command to stop receive or transmission through serial programming will make the PT8R2401 into **Idle state**. The PT8R2401 enters into **Sleep state** by power down command through serial programming. **Sleep state** is the least power consumption among other states and all clocks include reference oscillator will stop the operation as well as the power down of all RF circuits. In **Sleep state**, only the serial programming interface logic can operate which uses clock from external device. However, the value of all registers will sustain until the wake up from **Sleep state**. Following figure shows the state transition in terms of power control.

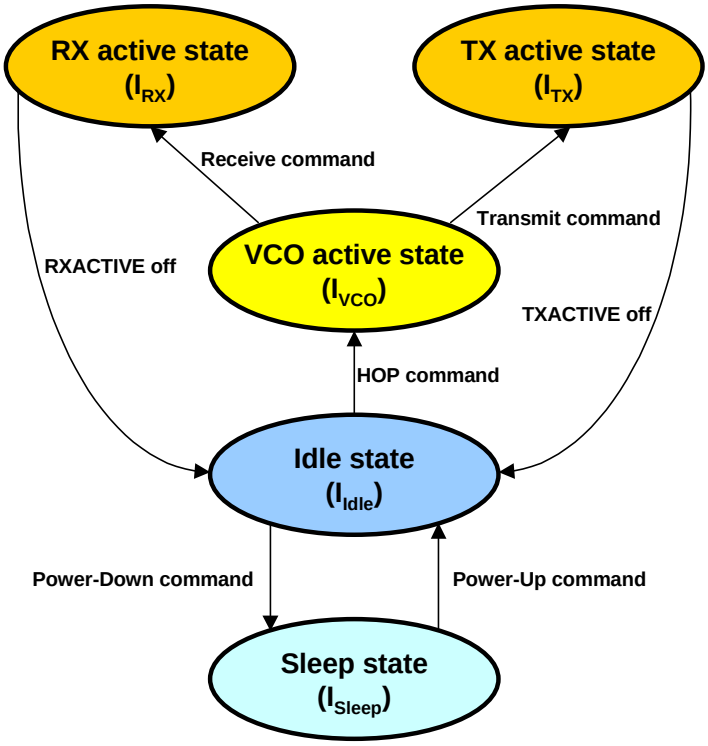


Figure 8. State transition diagram for power control

Serial Programming Interface (JTAG interface)

The serial programming interface is a JTAG boundary-scan architecture compliant with IEEE 1149.1. Interconnection between the serial interface and external baseband consists of four 1-bit digital signals : control data input(TDI), control mode select (TMS), control clock (TCK) and control data output (TDO). You must refer to the full IEE std 1149.1-1990 Standard Test Access Port and Boundary-Scan Architecture document for a complete, definitive description of the operation of the fundamentals of the JTAG interface. PT1002 support TCK up to 16MHz.

Table 1. TAP instructions

Instruction	Opcode	Description
EXTEST	0x000000	EXTEST initiates testing of external circuitry, typically board-level interconnects and off chip circuitry. EXTEST connects the Boundary-Scan register between TDI and TDO in the SHIFT_DR state only. When EXTEXT is selected, all output signal pin values are driven by values shifted into the Boundary-Scan register and may change only on the falling-edge of TCK in the Update_DR state. Also, when EXTEST is selected, all system input pin states must be loaded into the Boundary-Scan register on the rising-edge of TCK in the Capture_DR state. Values shifted into input latches in the Boundary-Scan register are never used by the processor's internal logic.
SAMPLE / PRELOAD	0x000001	SAMPLE / PRELOAD performs two functions: • When the TAP controller is in the Capture-DR state, the SAMPLE instruction occurs on the rising edge of TCK and provides a snapshot of the component's normal operation without interfering with that normal operation. The instruction causes Boundary-Scan register cells associated with outputs to SAMPLE the value being driven by or to the processor. • When the TAP controller is in the Update-DR state, the PRELOAD instruction occurs on the falling edge of TCK. This instruction causes the transfer of data held in the Boundary-Scan cells to the slave register cells. Typically the slave-latched data is then applied to the system outputs by means of the EXTEST instruction.
IDCODE	0x011111	IDCODE is used in conjunction with the device identification register. It connects the identification register between TDI and TDO in the Shift_DR state. When selected, IDCODE parallel-loads the hard-wired identification code (32 bits) on TDO into the identification register on the rising edge of TCK in the Capture_DR state. NOTE: The device identification register is not altered by data being shifted in on TDI.
REGISTER PROGRAMMING	0x1SSSSS	REGISTER PROGRAMMING instruction select the REGISTER with address indicator SSSSS. • When the TAP controller is in the Capture-DR state, the REGISTER PROGRAMMING instruction occurs on the rising edge of TCK and executes a snapshot of register addressed SSSSS into serial register. • When the TAP controller is in the Update-DR state, the REGISTER PROGRAMMING instruction occurs on the falling edge of TCK. This instruction causes the transfer of data held in serial register to register addressed SSSSS.
BYPASS	0x111111	BYPASS instruction selects the Bypass register between TDI and TDO pins while in SHIFT_DR state, effectively bypassing the processor's test logic. 0 is captured in the CAPTURE_DR state. While this instruction is in effect, all other test data registers have no effect on the operation of the system. Test data registers with both test and system functionality perform their system functions when this instruction is selected.

SPI Register Map

The values of all registers except read-only are set by default values after rest. The default values can be overrided by accessing each register. Typical register values are subject to change and should be obtained from PTI. During normal operation, SPI access should occur to address the following functions only.

- Programming PLL hop frequency of BT_RF_PLL_CTRL0
- Setting Tx power control value of BT_RF_TX_CTRL in the transmit mode
- Reading receive signal strength indication of BT_RSSI_STA in the receive mode
- Programming TXA or RXA of BT_RF_PLL_CTRL1 to indicate transmit or receive mode in bidirectional interface

Table 2. SPI register address map

Address	Name	Attribute	Description
0x00	BT_SOFT_RESET	write	RESET by serial interface*
0x01	BT_MODEM_CTRL	read/write	Modem control register
0x02	BT_RF_RX_CTRL	read/write	RF receiver control register
0x03	BT_RF_TX_CTRL	read/write	RF transmitter control register
0x04	BT_RF_BB_CTRL0	read/write	RF baseband control0 register
0x05	BT_RF_BB_CTRL1	read/write	RF baseband control1 register
0x06	BT_RF_PLL_CTRL0	read/write	RF PLL control0 register
0x07	BT_RF_PLL_CTRL1	read/write	RF PLL control1 register
0x08	BT_RF_PLL_CTRL2	read/write	RF PLL control2 register
0x09	BT_RF_PLL_CTRL3	read/write	RF PLL control3 register
0x0A	BT_RF_TIM_CTRL0	read/write	RF timing adjustment configuration0 register
0x0B	BT_RF_TIM_CTRL1	read/write	RF timing adjustment configuration1 register
0x0C	BT_RF_TIM_CTRL2	read/write	RF timing adjustment configuration2 register
0x0D	BT_RF_TIM_CTRL3	read/write	RF timing adjustment configuration3 register
0x0E	BT_RF_TIM_CTRL4	read/write	RF timing adjustment configuration4 register
0x0F	BT_RF_TIM_CTRL5	read/write	RF timing adjustment configuration5 register
0x10	BT_RF_AUX_CTRL0	read/write	RF auxiliary control0 register
0x11	BT_RF_AUX_CTRL1	read/write	RF auxiliary control1 register
0x12	BT_RSSI_STA	read	Modem RSSI register
0x13	BT_RF_STA	read	RF status register
0x14	BT_DAC_TEST_CTRL	read/write	DAC test register
0x15	BT_PWD_CTRL0	read/write	MODEM power detector register0
0x16	BT_PWD_CTRL1	read/write	MODEM power detector register1
0x17~0x1D	-	-	Reserved
0x1E	BT_PWDN	write	Power down register
0x1F	IDCODE	read	IDCODE

* Equivalent to hardware reset by asserting RESET pin.

* The values in all registers are the recommended initial value to be set by the serial programming interface, since some of them may be different value with the default configuration by hardware after reset. Also, these value can be changed in order to be optimized for special purpose. Please contact PTI semiconductor to get up-to-date configuration.

0x01 BT_MODEM_CTRL

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS														TEPM	
0	01011b					0111b				0	1	1	1	00b	

TEPM	External power amp drive enable mode 00 : off 01 : on 10/11 : on during TXACTIVE is high
CKS	Reference clock select flag 0 : 13MHz 1 : 16MHz

0x02 BT_RF_RX_CTL

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
01b		0	01b		1000b				0b	000000b					

0x03 BT_RF_TX_CTL

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
			OS					TPG					TAG		
		1	0	0111b				11111b					001b		

OS	Output DATACLK PAD strength 0 : The driving capability of DATACLK is low 1 : The driving capability of DATACLK is high
TPG	External power amp gain control 00000b (1mA) ~ 11111b(0mA) with 32uA step
TAG	Transmission AGC gain control 000b(-3dB), 001b(-1.5dB), 010b(0dB), 011b(1.5dB), 100b(3dB), 101b(4.5dB), 110(6dB), 111(7.5dB)

0x04 BT_RF_BB_CTRL0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	0	0	1	1	0	1	11b		0	0011b				0

0x05 BT_RF_BB_CTRL1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1010b				0	111b			011b			0000b			

0x06 BT_RF_PLL_CTRL0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TXA	RXA	TG							CH						
0	0	0111111b							0000000b						

TXA	Internal TXACTIVE signal generation in bidirectional interface. Writing HIGH For more detail operation, refer to I/O description of transmit operation. This field does not affect in unidirectional interface.
RXA	Internal RXACTIVE signal generation in bidirectional interface. For more detail operation, refer to I/O description of receiver operation. This field does not affect in unidirectional interface.
TG[6]	Internal pre power amp gain control with bias change 1 : gain increase, 0 : gain decrease
TG[5:0]	Internal pre power amp gain control with driving ability 000000b(minimum gain) ~ 111111b(maximum gain)
CH	Frequency channel selection 0000000b : 0 channel(2402MHz), 0000001b : 1 channel(2403MHz), …

0x07 BT_RF_PLL_CTRL1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	0	00000000								00000				

0x08 BT_RF_PLL_CTRL2

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	00b		11b		001b			00b		10b		1	010b		

0x09 BT_RF_PLL_CTRL3

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1000000000b										00b		00b		0	0

0x0A BT_RF_TIM_CTRL0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TBD				TBD				TBD				TBD			

0x0B				BT_RF_TIM_CTRL1											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TBD				TBD				TBD				TBD			

0x0C				BT_RF_TIM_CTRL2											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TBD				TBD				TBD				TBD			

0x0D				BT_RF_TIM_CTRL3											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TBD				TBD				TBD				TBD			

0x0E				BT_RF_TIM_CTRL4											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TBD				TBD				TBD				TBD			

0x0F				BT_RF_TIM_CTRL5											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TBD		TBD		TBD		TBD			TBD		TBD		TBD		

0x10				BT_RF_AUX_CTRL0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	01b		0	1000b				1	1	000000b					

0x11				BT_RF_AUX_CTRL1											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
												PVN	PVL		
1	000b			01b		01b		1	0	0	0	0	100b		

PVN	Pre power amp output power detection enable 0 : disable 1 : enable
PVL	Pre power amp power detector reference level 000b(-7dBm), 001b(-5dBm), 010b(-3dBm), 011b(-1dBm) 100b(0dBm), 101b(1dBm), 110b(2dBm), 111b(3dBm)

0x12				BT_RSSI_STA											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PVO	RSSI_PO3						RSSI_RF				RSSI_AGC			

PVO	1 : The current power of pre power amp is more than PVL 0 : The current power of pre power amp is less than PVL
RSSI_AGC	AGC gain value with 3dB step from –3dB(0000b) to 42dB(1111b)

0x13				BT_POW_STA											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
						CSS									

0x14				BT_DAC_TEST_CTRL											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
			DE	DACI						DACQ					
			0	000000b						000000b					

0x15				BT_PWD_CTRL0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
						PWD_START								AFS	DSS
						10000010b								1	1

0x16				BT_PWD_CTRL1											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
			PBD	PWR_TH3				PWR_TH2				PWR_TH1			
			0	1010b				0100b				0110b			

0x1E				BT_ PWDN											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
															PD
															0

PD	1 : Power down mode enable 0 : Power down mode disable

0x1F				IDCODE											
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
IDCODE[31:16]															
0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IDCODE[15:0]															
0x0001															

JTAG Registers Programming Timing Diagram In Unidirectional Interface

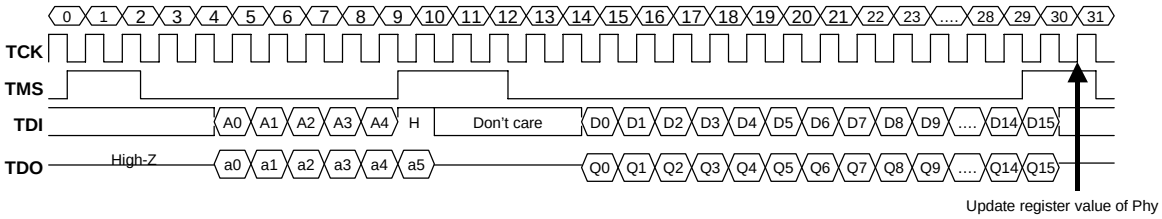


Figure 9. Serial register write programming timing diagram in JTAG

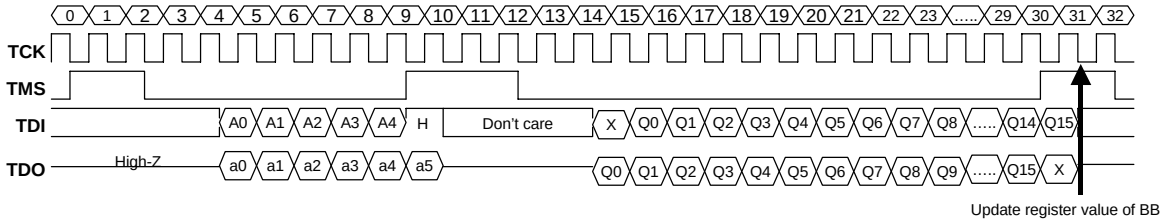


Figure 10. Serial register read programming timing diagram in JTAG

Electrical Specifications

Absolute Maximum Rating

Parameter	Symbol	Test condition	Min	typ	max	Unit
Storage Temperature			-40		85	°C
Ambient Temperature with Power Applied			-20		65	°C
Supply Voltage (no damage)			0.8		3.9	**V**
DC Input Voltage			-0.3		Vcc +0.3	**V**
DC Voltage applied to Outputs in High-Z State			-0.3		Vcc +0.3	**V**
Digital Inputs			Vcc – 0.4V		Vcc+0. 4V	**V**
Static Discharge Voltage (Digital) [1]					2000	**V**
Static Discharge Voltage (RF) [1]					500	**V**
Latch-up Current			-200		200	**mA**

Note: Rating measured using the Human Body Model (HBM).

Recommended Operating Conditions

Parameter	Symbol	Test condition	min	typ	max	Unit
Supply Voltage		VCC2.7		2.7		V
		VCC3.3		3.3		V
Temperature			0		40	°C
Humidity					95	%

DC/AC Specification

Power Consumption

Parameter	Symbol	Test condition	min	typ	max	Unit
Radio Transmit Current		DH1 pakaet with PRBS9 payload, no hops			60	mA
Radio Receive Current		DH1 pakaet with PRBS9 payload, no hops			60	mA
Radio Transmit Peak current		DH1 pakaet with PRBS9 payload, 1.6k hops			70	mA
Radio Receive Peak current		DH1 pakaet with PRBS9 payload, 1.6k hops			70	mA
Idle Current		Tx and Rx no active			20	mA
Deep Sleep Current		Deep Sleep Mode			20	uA

Common Radio Specifications

Parameter	symbol	Test condition	min	typ	max	Unit
Operating Frequency		f = (2.402 + k) GHz, k = 0,1,2,…78	2402		2480	MHz
Channel intervals				1		MHz
Channel		Number of channels		79		
Duplexing slot time		Transmission scheme TDD – time division duplex		625		us
Symbol Rate				1M		symbol /s
Modulation Data Polarity		“H”		Fc +dF		
		“L”		Fc –dF		
Hop Rate				1600		hops/sec
Antenna interface output impedance				50		ohm

Radio Receiver Specifications

Parameter	symbol	Test condition	min	typ	max	Unit
Sensitivity		0.1% BER DH1 pakaet with PRBS9 payload,no hops, at 2402,2441,2480 MHz		-85	-80	dBm
Maximum received signal		0.1% BER DH1 pakaet with PRBS9 payload,no hops, at 2402,2441,2480 MHz	-20	-5.0		dBm
Self channel selectivity		C/I Co-channel (1)		9	11	dBc
Adjacent channel selectivity		C/I 1MHz (1)		-2.0	0	dBc
2nd adjacent channel selectivity		C/I 2MHz (1)		-34	-30	
3rd adjacent channel selectivity		C/I •3MHz (1) (2)		-43	-40	
Image rejection		C/I (1) (3)		-12	-9	
Maximum level of intermodulation interferes		(1) (4)	-39	-30		dBm
Maximum level of GSM signal at 1.8GHz		0.1% BER with wanted input at –67dBM, and with the RF filter removed from the circuit, DH1 pakaet with PRBS9 payload, 1.6k hops		-7.0		dBm
Maximum level of W-CDMA signal at 1.8GHz				-9.5		
Maximum level of W-CDMA signal at 2.2GHz				-11		dBm

Radio Transmitter Specifications

Parameter	symbol	Test condition	min	typ	max	Unit
RF transmit power level		DH1 pakaet with PRBS9 payload,no hops, single slot packets, at 2402,2441,2480 MHz				dBm
RF power control range		DH1 pakaet with PRBS9 payload,no hops, single slot packe, at 2441 MHz	16	30		dB
RF power range control resolution				2.0		
20 dB bandwidth for modulated carrier		DH1 pakaet with PRBS9 payload,no hops, single slot packets, at 2402,2480 MHz		900	1000	kHz
Initial Carrier Freq Tolerance		DH1 pakaet with PRBS9 payload, no hops, single slot packe, at 2441 MHz		+/- 25	+/- 75	KHz
Frequency Deviation		single slot, Continue 101010 pattern, 11110000 pattern, at 2441 MHz	90		175	kHz
Zero Crossing Error		single slot, Continue 101010 pattern, 11110000 pattern, at 2441 MHz	-125		125	ns
2nd adjacent channel transmit power		Second Channel Power (±2 MHz), DH1 pakaet with PRBS9 payload,no hops, single slot packets at 2441 MHz		-52	-20	dBm
>3rd adjacent channel transmit power		Third Channel Power (>3 MHz), DH1 pakaet with PRBS9 payload,no hops, single slot packets, at 2441 MHz		-57	-40	dBm
Non-harmonically Related Spurious		30 MHz – 12.75 GHz at 2441 MHz		–57		dBm
2nd Harmonic Spurious		at 2441 MHz			-26	dBm
3rd Harmonic Spurious		at 2441 MHz			-30	dBm
4th Harmonic Spurious		at 2441 MHz			-37	dBm

Notes:
(1) Measured according to the Bluetooth specification.
(2) Up to five spurious responses within Bluetooth limits are allowed
(3) At carrier –3MHz.
(4) Measured at f1 – f2 = 5MHz.
(5) For 0.1% BER with wanted input at –67dBM, and with the RF filter removed from the circuit.

Notes

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