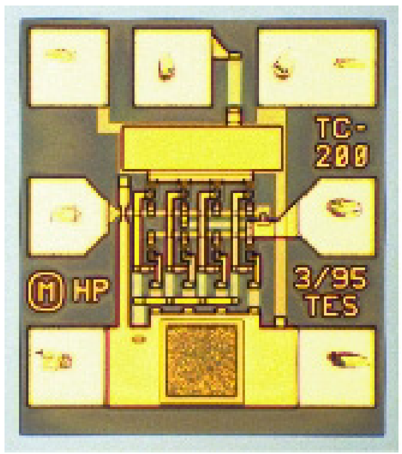
Agilent HMMC-5200 DC–20 GHz HBT Series–Shunt Amplifier

Data Sheet



Features

- **High Bandwidth, F_{-1dB}: 21 GHz Typical**
- **Moderate Gain: 9.5 dB ±1 dB @ 1.5 GHz**
- **P_{-1dB} @ 1.5 GHz: 12.5 dBm Typical**
- **Low I/f Noise Corner: <20 kHz Typical**
- **Single Supply Operation: >4.75 volts @ 44 mA Typ.**
- **Low Power Dissipation: 190 mW Typ. for chip**

Chip Size:	410 × 460 µm (16.1 × 18.1 mils)
Chip Size Tolerance:	± 10 µm (± 0.4 mils)
Chip Thickness:	127 ± 15 µm (5.0 ± 0.6 mils)
Pad Dimensions:	70 × 70 µm (2.8 × 2.8 mils), or larger

Description

The HMMC-5200 is a DC to 20 GHz, 9.5 dB gain, feedback amplifier designed to be used as a cascadable gain block for a variety of applications. The device consists of a modified Darlington feedback pair which reduces the sensitivity to process variations and provides 50 ohm input/output port matches. Furthermore, this amplifier is fabricated using MWTC's Heterojunction Bipolar Transistor (HBT) process which provides excellent process uniformity, reliability and 1/f noise performance. The device requires a single positive supply voltage and generally operates Class–A for good distortion performance.

Absolute Maximum Ratings[1]

Symbol	Parameters/Conditions	Min.	Max.	Units
V_{CC}	VDC Pad Voltage		8.0	Volts
V_{PAD}	Output Pad Voltage		3.5	Volts
P_{in}	RF Input Power, Continuous		+6	dBm
TJ	Junction Temperature		+150	°C
T_{op}	Operating Temperature	–55	+85	°C
T_{st}	Storage Temperature	–65	+165	°C
T_{max}	Max. Assembly Temperature		+300	°C

Notes:

1. Operation in excess of any one of these ratings may result in permanent damage to this device. For normal operation, all combined bias and thermal conditions should be chosen such that the maximum Junction Temperature (T_J) is not exceeded. T_A=25°C except for T_{op}, T_{st}, and T_{max}.

DC Specifications/Physical Properties[1]

(Typicals are for V_{CC} = + 5V, R_{out} = 64Ω)

Symbol	Parameters/Conditions	Min.	Typ.	Max.	Units
V_{CC}	Supply Voltage	4.75	6.0		Volts
I_{C1}	Stage–One Supply Current	14.5	17	20	mA
I_{C2}	Stage–Two Supply Current	26	29	32	mA
$I_{C1}+I_{C2}$	Total Supply Current		46		mA
$\theta_{J\text{-}bs}$	Thermal Resistance[1] (Junction–to–Backside at TJ = 150°C)[2]		340		°C/Watt

Notes:

1. Backside ambient operating temperature $T_A = T_{op}$ = 25°C unless otherwise noted.
2. Thermal resistance (in °C/Watt) at a junction temperature T(°C) can be *estimated* using the equation:

$\theta(T) \cong \theta(T_J)$ [T(°C)+273] / [T_J(°C)+273] where θ (T_J=150°C) = $\theta_{J\text{-}bs}$.

RF Specifications

(T_A = 25°C, V_{CC} = + 5V, R_{out} = 64Ω, 50Ω system)

Symbol	Parameters/Conditions	Min.	Typ.	Max.	Units
BW	Operating Bandwidth (f_{-3db})	20			GHz
BW	Operating Bandwidth (ff_{-1db})		21		GHz
S_{21}	Small Signal Gain (@1.5 GHz)	8.5	9.7	10.5	dB
Δ Gain	Small Signal Gain Flatness (DC–5 GHz)		± 0.2		dB
	Small Signal Gain Flatness (DC–20 GHz)		± 1		dB
TC	Temperature Coefficient of Gain (DC–13 GHz)		0.004		dB/°C
	Temperature Coefficient of Gain (13–20 GHz)		0.02		dB/°C
$(RL_{in})_{MIN}$	Minimum Input Return Loss (DC–15 GHz)		–15		dB
	Minimum Input Return Loss (15–20 GHz)		–12		dB
$(RL_{out})_{MIN}$	Minimum Output Return Loss		–15		dB
Isolation	Reverse Isolation		–15		dB
Pf_{-1dB}	Output Power at 1dB Gain Compression:				dBm
	(@ 1.5 GHz)		12.5		
	(@ 5 GHz)		12.5		
	(@ 10 GHz)		11.7		
	(@ 15 GHz)		10.6		
	(@ 20 GHz)		8.0		
P_{SAT}	Saturated Output Power (@ 1.5 GHz)		13		dBm
NF	Noise Figure:				dB
	(@ 1 GHz)		6.5		
	(@ 6 GHz)		6.8		
	(@ 10 GHz)		7		
	(@ 15 GHz)		7.5		
	(@ 16 GHz)		8		
	(@ 18 GHz)		8.5		

Applications

The HMMC-5200 can be used for a variety of applications requiring moderate amounts of gain and low power dissipation in a 50Ω system.

Biasing and Operation

The HMMC-5200 can be operated from a single positive supply. This supply must be connected to two points on the chip, namely the V_{CC} pad and the output pad. The supply voltage may be directly connected to the V_{CC} pad as long as the voltage is between +4.75 to +7 volts; however, if the supply is higher than +7 volts, a series resistor (R_{CC}) should be used to reduce the voltage to the V_{CC} pad. See the bonding diagram for the equation used to select R_{CC}. In the case of the output pad, the supply voltage must be connected to the output transmission line through a resistor and an inductor. The required value of the resistor is given by the equation:

$$R_{out} = 35.7V_{supply} - 114.3\Omega,$$

where V_{supply} is in volts. If R_{OUT} is greater than 300Ω, the inductor may be omitted, however, the amplifier's gain may be reduced by ~0.5 dB. Figure 4 shows a recommended bonding strategy.

The chip contains a backside via to provide a low inductance ground path; therefore, the ground pads on the IC should not be bonded.

The voltage at the IN and OUT pads of the IC will be approximately 3.2 volts; therefore, DC blocking caps should be used at these ports.

Assembly Techniques

It is recommended that the RF input and RF output connections be made using 0.7 mil diameter gold wire. The chip is designed to operate with 0.1–0.3 nH of inductance at the RF input and output. This can be accomplished by using 10 mil bond wire lengths on the RF input and output. The bias supply wire can be a 0.7 mil diameter gold wire attached to the V_{CC} bonding pad.

GaAs MMICs are ESD sensitive. ESD preventive measures must be employed in all aspects of storage, handling, and assembly.

MMIC ESD precautions, handling considerations, die attach and bonding methods are critical factors in successful GaAs MMIC performance and reliability.

Agilent application note #54, "GaAs MMIC ESD, Die Attach and Bonding Guidelines" provides basic information on these subjects.

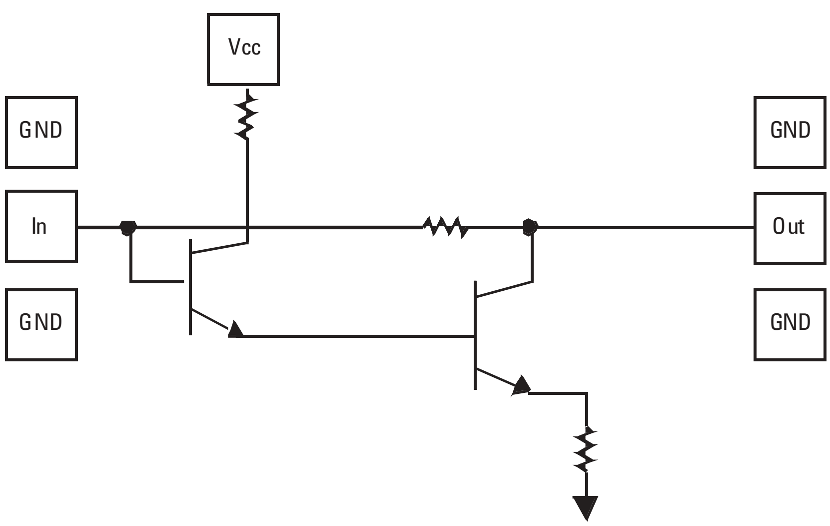


Figure 1.
Simplified Schematic Diagram

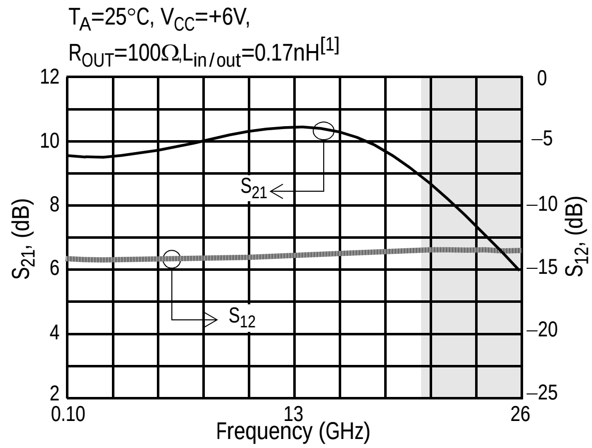


Figure 2.
Typical S_{21} and S_{12} Response

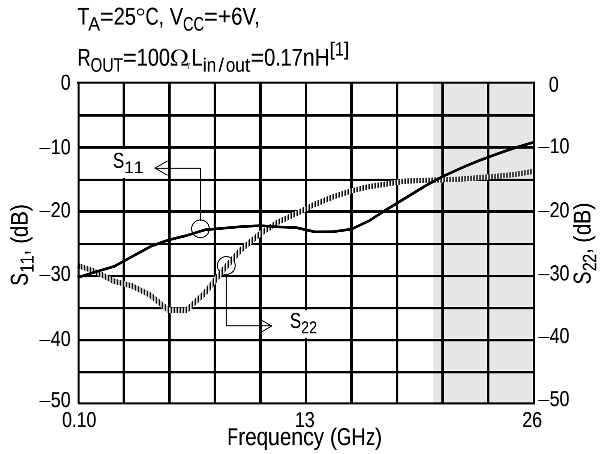


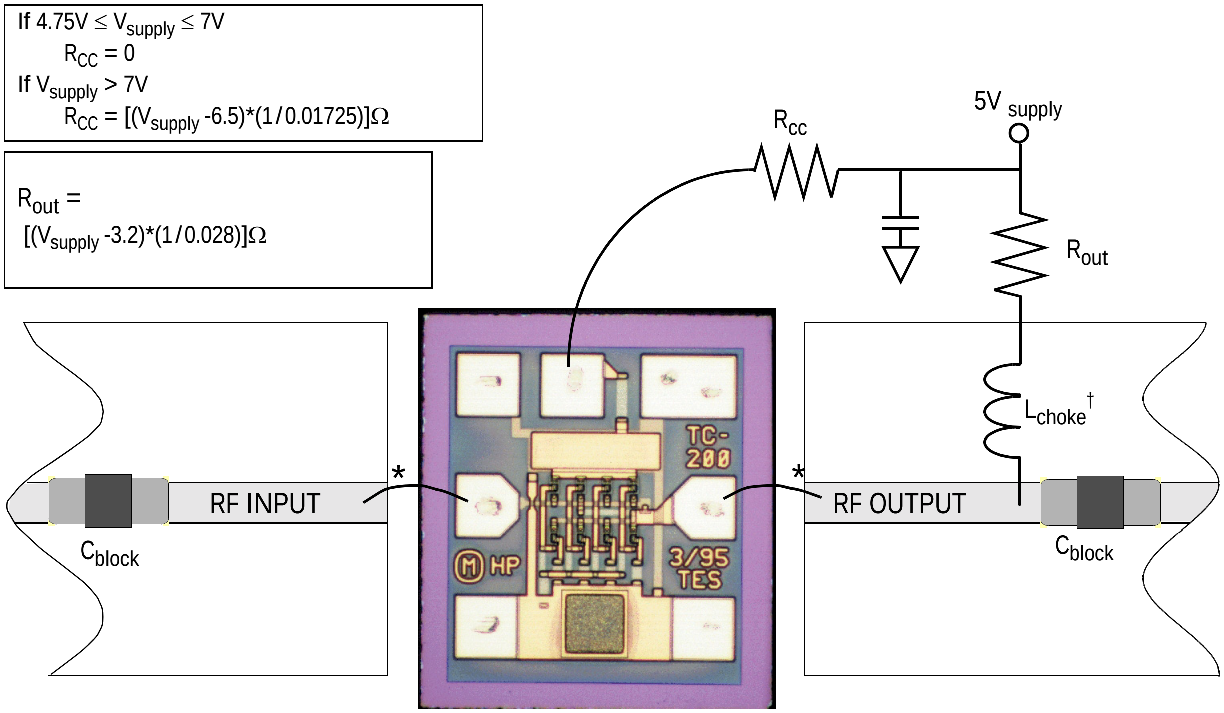
Figure 3.
Typical S_{11} and S_{22} Response

S–Parameters[1] (T_A = 25°C, V_{CC} = + 6V, R_{OUT} = 100Ω,$L_{in/out}$=0.17nH)

Freq. (GHz)	S_{11}			S_{12}			S_{21}			S_{22}		
	dB	mag	ang	dB	mag	ang	dB	mag	ang	dB	mag	ang
0.0	−30.4	0.030	28.9	−14.1	0.197	0.0	9.5	3.013	179.9	−28.4	0.038	−1.5
1.0	−29.5	0.033	24.9	−14.1	0.195	−2.0	9.5	2.999	171.5	−29.3	0.034	−7.049
2.0	−28.7	0.037	27.3	−14.2	0.194	−4.1	9.5	2.992	163.2	−30.8	0.029	−15.233
3.0	−27.2	0.043	33.5	−-14.2	0.195	−6.2	9.5	3.009	155.0	−31.5	0.026	−23.9
4.0	−25.6	0.052	32.4	−14.1	0.195	−8.3	9.6	3.036	146.7	−33.6	0.022	−42.7
5.0	−24.8	0.058	33.3	−14.1	0.195	−10.4	9.7	3.062	138.2	−35.8	0.016	−72.8
6.0	−24.0	0.063	31.1	−14.1	0.196	−12.6	9.8	3.097	129.6	−36.6	0.015	−109.3
7.0	−23.1	0.070	27.1	−14.1	0.197	−14.7	9.9	3.135	120.9	−34.1	0.020	−143.3
8.0	−22.6	0.074	21.9	−14.0	0.197	−16.9	10.0	3.181	112.0	−30.1	0.031	−166.4
9.0	−22.5	0.074	15.7	−14.0	0.198	−19.1	10.1	3.225	102.9	−26.9	0.045	176.1
10.0	−22.3	0.076	8.55	−14.0	0.199	−21.4	10.2	3.266	93.5	−24.4	0.060	164.4
11.0	−22.4	0.076	−0.36	−13.9	0.200	−23.6	10.3	3.298	83.9	−22.5	0.075	154.2
12.0	−22.5	0.075	−13.5	−13.9	0.201	−25.8	10.4	3.322	74.2	−20.9	0.090	147.9
13.0	−22.8	0.072	−27.9	−13.8	0.203	−28.2	10.4	3.338	64.4	−19.5	0.105	141.1
14.0	−23.2	0.069	−47.1	−13.8	0.204	−30.6	10.4	3.332	54.2	−18.3	0.121	134.2
15.0	−22.9	0.071	−-69.7	−13.7	0.205	−33.1	10.3	3.306	44.0	−17.5	0.133	128.4
16.0	−22.5	0.075	−93.4	−13.6	0.207	−35.7	10.2	3.253	33.7	−16.7	0.145	122.0
17.0	−20.8	0.091	−115.1	−13.6	0.208	−37.9	10.0	3.181	23.5	−16.0	0.158	118.6
18.0	−19.2	0.109	−134.4	−13.5	0.210	−40.8	9.7	3.085	13.4	−15.5	0.167	112.3
19.0	−17.4	0.134	−149.6	−13.4	0.212	−43.8	9.4	2.975	3.5	−15.3	0.172	109.7
20.0	−15.8	0.161	−161.7	−13.4	0.213	−46.8	9.0	2.844	−6.0	−15.2	0.172	106.0
21.0	−14.4	0.190	−172.3	−13.4	0.213	−49.8	8.6	2.706	−15.4	−14.9	0.179	105.1
22.0	−13.1	0.220	178.7	−13.4	0.213	−52.9	8.1	2.560	−24.4	−14.9	0.178	104.0
23.0	−12.0	0.250	170.7	−13.4	0.212	−55.6	7.6	2.416	−33.0	−14.7	0.183	103.0
24.0	−11.0	0.281	163.3	−13.4	0.212	−58.3	7.1	2.272	−41.3	−14.5	0.187	104.9
25.0	−10.1	0.313	157.0	−13.5	0.211	−61.2	6.5	2.134	−49.2	−14.2	0.193	105.7
26.0	−9.29	0.343	150.8	−13.4	0.212	−63.9	6.0	1.997	−56.9	−13.8	0.203	106.8

Notes:

1. S–parameter data obtained from on–wafer device measurement plus simulation of input and output wire bond inductance.

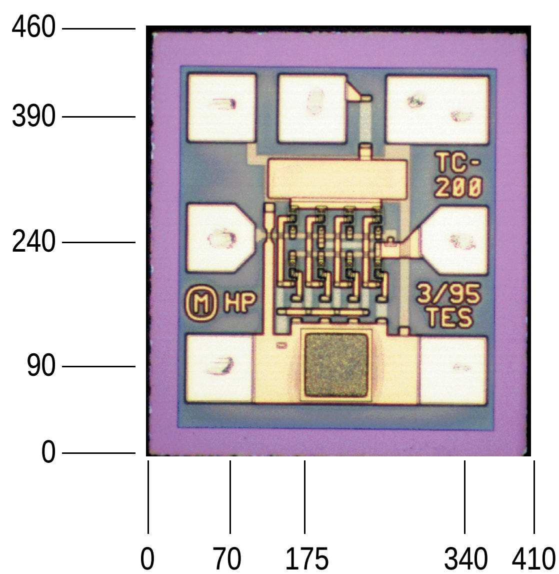


Note: Blocking Cap required on input and output.

Figure 4.
Assembly Diagram

* Note: For optimum performance, the input and output bond wire inductances should each be 0.1–0.3 nH. (bond wire has about 20 pH/mil of inductance).

† L_{choke} is optional if R_{out} is greater than 300Ω, however, gain will be reduced by about 0.5 dB.



Note:
All dimensions in microns.

Figure 5.
Bonding Pad Positions

This data sheet contains a variety of typical and guaranteed performance data. The information supplied should not be interpreted as a complete list of circuit specifications. In this data sheet the term *typical* refers to the 50th percentile performance. For additional information contact your local Agilent Technologies' sales representative.

www.agilent.com/semiconductors

For product information and a complete list of distributors, please go to our web site.

For technical assistance call:

Americas/Canada: +1 (800) 235-0312 or (408) 654-8675

Europe: +49 (0) 6441 92460

China: 10800 650 0017

Hong Kong: (+65) 6271 2451

India, Australia, New Zealand: (+65) 6271 2394

Japan: (+81 3) 3335-8152(Domestic/International), or 0120-61-1280(Domestic Only)

Korea: (+65) 6271 2194

Malaysia, Singapore: (+65) 6271 2054

Taiwan: (+65) 6271 2654

Data subject to change.

October 10, 2003
5988-3202EN

Agilent Technologies