Section 20 Electrical Specifications

20.1 Absolute Maximum Ratings

Table 20-1 lists the absolute maximum ratings.

Table 20-1 Absolute Maximum Ratings

Item		Symbol	Rating	Unit
Supply voltage		V_{CC}	–0.3 to +7.0	V
I/O buffer supply voltage		$V_{CC}B$	–0.3 to +7.0	V
Flash memory programming voltage		FV_{PP}	–0.3 to +13.0	V
Programming voltage		V_{PP}	–0.3 to +13.5	V
Input voltage	Ports 1 to 6, 8, 9	V_{in}	–0.3 to V_{CC} + 0.3	V
	Port 7	V_{in}	–0.3 to AV_{CC} + 0.3	V
Reference supply voltage		AV_{ref}	–0.3 to AV_{CC} + 0.3	V
Analog supply voltage		AV_{CC}	–0.3 to +7.0	V
Analog input voltage		V_{AN}	–0.3 to AV_{CC} + 0.3	V
Operating temperature		T_{opr}	Regular specifications: –20 to +75	°C
			Wide-range specifications: –40 to +85	°C
Storage temperature		T_{stg}	–55 to +125	°C

Note: Exceeding the absolute maximum ratings shown in table 20-1 can permanently destroy the chip.

20.2 Electrical Characteristics

20.2.1 DC Characteristics

Table 20-2 lists the DC characteristics of the 5-V version. Table 20-3 lists the DC characteristics of the 3 V version. Table 20-4 gives the allowable current output values of the 5-V version. Table 20-5 gives the allowable current output values of the 3-V version. Bus drive characteristics common to both 5 V and 3 V versions are listed in table 20-6.

Table 20-2 DC Characteristics (5-V Version) — Preliminary —

Conditions: $V_{CC} = V_{CC}B = 5.0\ V \pm 10\%$, $AV_{CC} = 5.0\ V \pm 10\%$*1, $AV_{ref} = 4.5\ V$ to AV_{CC}, $V_{SS} = AV_{SS} = 0\ V$, Ta = –20 to 75°C (regular specifications), Ta = –40 to 85°C (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Schmitt trigger input voltage (1)	$P6_7$–$P6_0$*4, PA_7–PA_0*4, $\overline{IRQ_2}$–$\overline{IRQ_0}$*5, $\overline{IRQ_7}$–$\overline{IRQ_3}$, SCL, SDA	V_T^-	1.0	—	—	V	
		V_T^+	—	—	$V_{CC} \times 0.7$		
		$V_T^+ - V_T^-$	0.4	—	—		
Input high voltage (2)	RES, STBY, NMI MD_1, MD_0 EXTAL	V_{IH}	$V_{CC} - 0.7$	—	$V_{CC} + 0.3$	V	
	$P7_7$–$P7_0$		2.0	—	$AV_{CC} + 0.3$		
Input high voltage	Input pins other than (1) and (2)	V_{IH}	2.0	—	$V_{CC} + 0.3$		
Input low voltage (3)	RES, STBY MD_1, MD_0	V_{IL}	–0.3	—	0.5	V	
Input low voltage	Input pins other than (1) and (3) above	V_{IL}	–0.3	—	0.8		
Output high voltage	All output pins (except RESO)*6	V_{OH}	$V_{CC} - 0.5$	—	—	V	$I_{OH} = -200\ \mu A$
			3.5	—	—		$I_{OH} = -1.0\ mA$
Output low voltage	All output pins (except RESO)*6	V_{OL}	—	—	0.4	V	$I_{OL} = 1.6\ mA$
	Ports 1 and 2		—	—	1.0		$I_{OL} = 10.0\ mA$
	RESO		—	—	0.4		$I_{OL} = 2.6\ mA$
Input leakage current	RES, STBY	$\lvert I_{in} \rvert$	—	—	10.0	μA	$V_{in} = 0.5\ V$ to $V_{CC} - 0.5\ V$
	NMI, MD_1, MD_0		—	—	1.0		
	$P7_7$–$P7_0$		—	—	1.0		$V_{in} = 0.5\ V$ to $AV_{CC} - 0.5\ V$
Leakage current in 3-state (off state)	Ports 1, 2, 3 4, 5, 6, 8, 9, A, B, RESO	$\lvert I_{TSI} \rvert$	—	—	1.0	μA	$V_{in} = 0.5\ V$ to $V_{CC} - 0.5\ V$
Input pull-up MOS current	Ports 1, 2, 3	$-I_P$	30	—	250	μA	$V_{in} = 0\ V$
	Ports 6, A, B		60	—	500		

Table 20-2 DC Characteristics (5-V Version) (cont) — **Preliminary** —

Conditions: $V_{CC} = V_{CC}B = 5.0\ V \pm 10\%$, $AV_{ref} = 4.5\ V$ to AV_{CC}, $AV_{CC} = 5.0\ V \pm 10\%$*1, $V_{SS} = AV_{SS} = 0\ V$, Ta = –20 to 75°C (regular specifications), Ta = –40 to 85°C (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	RES, STBY	C_{in}	—	—	60	pF	$V_{in} = 0\ V$ f = 1 MHz Ta = 25°C
	NMI, MD_1		—	—	30		
	All input pins except RES, STBY, NMI, and MD_1		—	—	15		
Current dissipation*2	Normal operation	I_{CC}	—	24	50	mA	f = 12 MHz
			—	32	60		f = 16 MHz
	Sleep mode		—	16	30		f = 12 MHz
			—	20	40		f = 16 MHz
	Standby modes*3		—	0.01	5.0	μA	
Analog supply current	During A/D conversion	AI_{CC}	—	1.2	2.0	mA	
	During A/D or D/A conversion		—	1.2	2.0		
	Waiting		—	0.01	5.0	μA	$AV_{CC} = 2.0\ V$ to 5.5 V
Reference supply voltage	During A/D conversion	AI_{ref}	—	0.3	0.6	mA	
	During A/D or D/A conversion		—	1.3	3.0		
	Waiting		—	0.01	5.0	μA	$AV_{ref} = 2.0\ V$ to 5.5 V
Analog supply voltage*1		AV_{CC}	4.5	—	5.5	V	During operation
			2.0	—	5.5		During wait state or when not in use
RAM standby voltage		V_{RAM}	2.0	—	—	V	

Notes on next page.

Notes:
1. Even when the A/D and D/A converters are not used, connect AV_{CC} to power supply V_{CC} and keep the applied voltage between 2.0 V and 5.5 V. At this time, make sure $AV_{ref} \leq AV_{CC}$.
2. Current dissipation values assume that $V_{IH\ min} = V_{CC} - 0.5$ V, $V_{IL\ max} = 0.5$ V, all output pins are in the no-load state, and all input pull-up transistors are off.
3. For these values it is assumed that $V_{RAM} \leq V_{CC} < 4.5$ V and $V_{IH\ min} = V_{CC} \times 0.9$, $V_{IL\ max} = 0.3$ V.
4. $\overline{P6_7}$ to $P6_0$ and PA_7 to PA_0 include supporting module inputs multiplexed with them.
5. $\overline{IRQ_2}$ includes ADTRG multiplexed with it.
6. Applies when IICS = IICE = 0. The output low level is determined separately when the bus drive function is selected.

Table 20-3 DC Characteristics (3-V Version) — **Preliminary** —

Conditions: $V_{CC} = V_{CC}B = 2.7$ V to 3.6 V, $AV_{CC} = 2.7$ V to 5.5 V*1, $AV_{ref} = 2.7$ V to AV_{CC}, $V_{SS} = AV_{SS} = 0$ V, Ta = –20 to 70°C

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Schmitt trigger input voltage*4 (1)	$P6_7$–$P6_0$*5, PA_7–PA_0*5, $\overline{IRQ_2}$–$\overline{IRQ_0}$*6, $\overline{IRQ_7}$–$\overline{IRQ_3}$, SCL, SDA	V_T^-	$V_{CC} \times 0.15$	—	—	V	
		V_T^+	—	—	$V_{CC} \times 0.7$		
		$V_T^+ - V_T^-$	0.2	—	—		
Input high voltage*4 (2)	RES, STBY MD_1, MD_0 EXTAL, NMI	V_{IH}	$V_{CC} \times 0.9$	—	$V_{CC} + 0.3$	V	
	$P7_7$–$P7_0$		$V_{CC} \times 0.7$	—	$AV_{CC} + 0.3$		
Input high voltage	Input pins other than (1) and (2) above		$V_{CC} \times 0.7$	—	$V_{CC} + 0.3$		
Input low voltage*4 (3)	RES, STBY MD_1, MD_0	V_{IL}	–0.3	—	$V_{CC} \times 0.1$	V	
Input low voltage	Input pins other than (1) and (3) above		–0.3	—	$V_{CC} \times 0.15$		
Output high voltage	All output pins (except RESO)*7	V_{OH}	$V_{CC} - 0.4$	—	—	V	$I_{OH} = -200$ µA
			$V_{CC} - 0.9$	—	—		$I_{OH} = -1.0$ mA
Output low voltage	All output pins (except RESO)*7	V_{OL}	—	—	0.4	V	$I_{OL} = 0.8$ mA
	Ports 1 and 2		—	—	0.4		$I_{OL} = 1.6$ mA
	RESO		—	—	0.4		$I_{OL} = 1.6$ mA
Input leakage current	RES, STBY	$\lvert I_{in} \rvert$	—	—	10.0	µA	$V_{in} = 0.5$ V to $V_{CC} - 0.5$ V
	NMI, MD_1, MD_0		—	—	1.0		
	$P7_7$–$P7_0$		—	—	1.0		$V_{in} = 0.5$ V to $AV_{CC} - 0.5$ V
Leakage current in 3-state (off state)	Ports 1, 2, 3 4, 5, 6, 8, 9, A, B, RESO	$\lvert I_{TSI} \rvert$	—	—	1.0	µA	$V_{in} = 0.5$ V to $V_{CC} - 0.5$ V
Input pull-up MOS current	Ports 1, 2, 3	$-I_p$	3	—	120	µA	$V_{in} = 0$ V
	Ports 6, A, B		30	—	250		

Refer to notes at the end of the table.

Table 20-3 DC Characteristics (3-V Version) (cont) — **Preliminary** —

Conditions: $V_{CC} = V_{CC}B = 2.7$ V to 3.6 V, $AV_{CC} = 2.7$ V to 5.5 V*1, $AV_{ref} = 2.7$ V to AV_{CC}, $V_{SS} = AV_{SS} = 0$ V, Ta = –20 to 70°C

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	RES, STBY	C_{in}	—	—	60	pF	$V_{in} = 0$ V, f = 1 MHz, Ta = 25°C
	NMI, $\overline{MD_1}$		—	—	30		
	All input pins except RES, STBY, NMI, and MD_1		—	—	15		
Current dissipation*2	Normal operation	I_{CC}	—	12	—	mA	f = 6 MHz
			—	20	40		f = 10 MHz
	Sleep mode		—	8	—		f = 6 MHz
			—	12	24		f = 10 MHz
	Standby modes*3		—	0.01	5.0	μA	
Analog supply current	During A/D conversion	AI_{CC}	—	1.2	2.0	mA	
	During A/D or D/A conversion		—	1.2	2.0		
	Waiting		—	0.01	5.0	μA	$AV_{CC} = 2.0$ V to 5.5 V
Reference supply voltage	During A/D conversion	AI_{ref}	—	0.3	0.6	mA	
	During A/D or D/A conversion		—	1.3	3.0		
	Waiting		—	0.01	5.0	μA	$AV_{ref} = 2.0$ V to 5.5 V
Analog supply voltage*1		AV_{CC}	2.7	—	5.5	V	During operation
			2.0	—	5.5		During wait state or when not in use
RAM backup voltage (in standby modes)		V_{RAM}	2.0	—	—	V	

Notes on next page.

Notes:
1. Even when the A/D and D/A converters are not used, connect AV_{CC} to power supply V_{CC} and keep the applied voltage between 2.0 V and 5.5 V. At this time, make sure $AV_{ref} \leq AV_{CC}$.
2. Current dissipation values assume that $V_{IH\ min} = V_{CC} - 0.5$ V, $V_{IL\ max} = 0.5$ V, all output pins are in the no-load state, and all input pull-up transistors are off.
3. For these values it is assumed that $V_{RAM} \leq V_{CC} < 2.7$ V and $V_{IH\ min} = V_{CC} \times 0.9$, $V_{IL\ max} = 0.3$ V.
4. In the range 3.6 V < V_{CC} < 4.5 V, for the input levels of V_{IH} and V_T^+, apply the higher of the values given for the 5 V and 3 V versions. For V_{IL} and V_T^-, apply the lower of the values given for the 5 V and 3 V versions.
5. $\overline{P6_7}$ to $P6_0$ and PA_7 to PA_0 include supporting module inputs multiplexed with them.
6. $\overline{IRQ_2}$ includes ADTRG multiplexed with it.
7. Applies when IICS = IICE = 0. The output low level is determined separately when the bus drive function is selected.

Table 20-4 Allowable Output Current Values (5-V Version) **— Preliminary —**

Conditions: $V_{CC} = V_{CC}B = 5.0\ V \pm 10\%$, $AV_{CC} = 5.0\ V \pm 10\%$, $AV_{ref} = 4.5\ V$ to AV_{CC}, $V_{SS} = AV_{SS} = 0\ V$, Ta = –20 to 75°C (regular specifications), Ta = –40 to 85°C (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit
Allowable output low current (per pin)	SCL, SDA, PA_4 to PA_7 (bus drive selection)	I_{OL}	—	—	20	mA
	Ports 1 and 2		—	—	10	
	RESO		—	—	3	
	Other output pins		—	—	2	
Allowable output low current (total)	Ports 1 and 2, total	ΣI_{OL}	—	—	80	mA
	Total of all output		—	—	120	
Allowable output high current (per pin)	All output pins	$-I_{OH}$	—	—	2	mA
Allowable output high current (total)	Total of all output	$\Sigma -I_{OH}$	—	—	40	mA

Table 20-4 Allowable Output Current Values (3-V Version)

Conditions: $V_{CC} = V_{CC}B = 2.7$ to 3.6 V, $AV_{CC} = 2.7\ V$ to 5.5 V, $AV_{ref} = 2.7\ V$ to AV_{CC}, $V_{SS} = AV_{SS} = 0\ V$, Ta = –20 to 75°C

Item		Symbol	Min	Typ	Max	Unit
Allowable output low current (per pin)	SCL, SDA, PA_4 to PA_7 (bus drive selection)	I_{OL}	—	—	10	mA
	Ports 1 and 2		—	—	2	
	RESO		—	—	1	
	Other output pins		—	—	1	
Allowable output low current (total)	Ports 1 and 2, total	ΣI_{OL}	—	—	40	mA
	Total of all output		—	—	60	
Allowable output high current (per pin)	All output pins	$-I_{OH}$	—	—	2	mA
Allowable output high current (total)	Total of all output	$\Sigma -I_{OH}$	—	—	30	mA

Note: To avoid degrading the reliability of the chip, be careful not to exceed the output current values in tables 20-4 and 20-5. In particular, when driving a darlington transistor pair or LED directly, be sure to insert a current-limiting resistor in the output path. See figures 20-1 and 20-2.

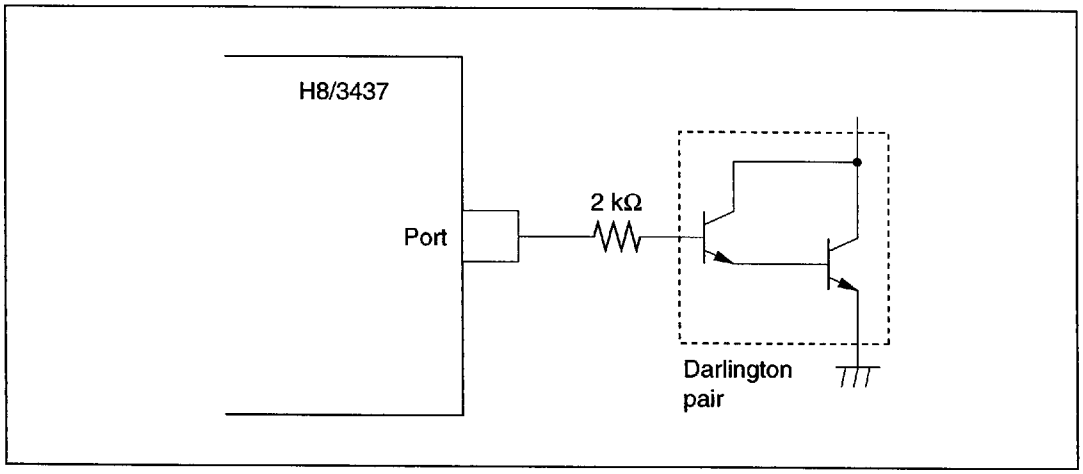


Figure 20-1 Example of Circuit for Driving a Darlington Pair (5-V Version)

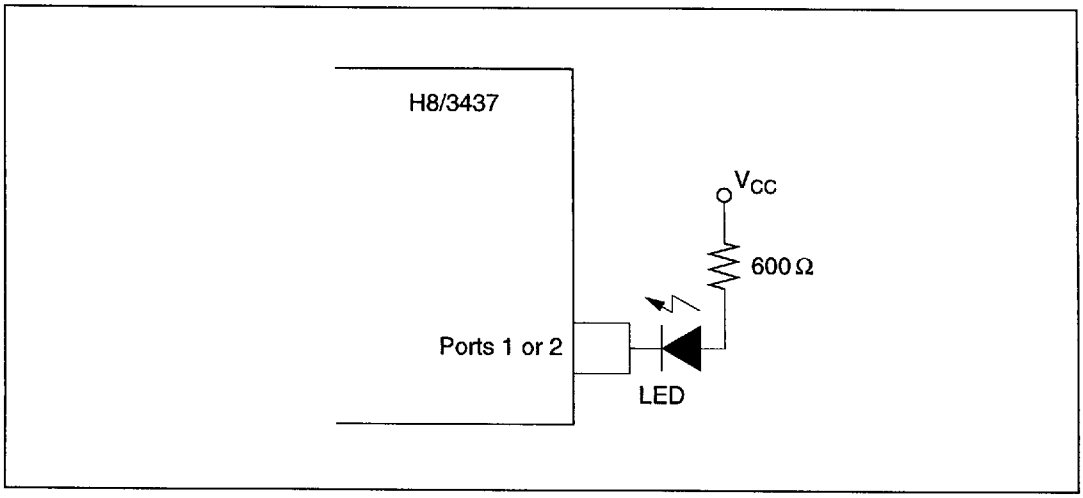


Figure 20-2 Example of Circuit for Driving an LED (5-V Version)

Table 20-6 Bus Drive Characteristics — **Preliminary** —

Conditions: V_{CC} = 2.7 to 5.5 V, V_{SS} = 0 V, Ta = –20 to +75°C

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Output low level voltage	SCL, SDA PA_4, PA_7 (bus drive selection)	V_{OL}	—	—	0.5	V	$V_{CC}B$ = 5 V ±10% I_{OL} = 16 mA
			—	—	0.5		$V_{CC}B$ = 2.7 V to 3.6 V I_{OL} = 8 mA

20.2.2 AC Characteristics

The AC characteristics are listed in four tables. Bus timing parameters are given in table 20-7, control signal timing parameters in table 20-8, and timing parameters of the on-chip supporting modules in table 20-9, amd I^2C bus timing parameters in table 20-10.

Table 20-7 Bus Timing — **Preliminary** —

Condition A: $V_{CC} = V_{CC}B = 5.0\ V \pm 10\%$, $V_{SS} = 0\ V$, $\phi = 2.0$ MHz to maximum operating frequency, Ta = –20 to 75°C (regular specifications), Ta = –40 to 85°C (wide-range specifications)

Condition B: $V_{CC} = V_{CC}B = 2.7\ V$ to $3.6\ V$, $V_{SS} = 0\ V$, $\phi = 2.0$ MHz to maximum operating frequency, Ta = –20 to 75°C

		Condition B		Condition A					
		10 MHz		12 MHz		16 MHz			Test
Item	Symbol	Min	Max	Min	Max	Min	Max	Unit	Conditions
Clock cycle time	t_{cyc}	100	500	83.3	500	62.5	500	ns	Fig. 20-4
Clock pulse width low	t_{CL}	35	–	30	–	20	–	ns	Fig. 20-4
Clock pulse width high	t_{CH}	35	–	30	–	20	–	ns	Fig. 20-4
Clock rise time	t_{Cr}	–	15	–	10	–	10	ns	Fig. 20-4
Clock fall time	t_{Cf}	–	15	–	10	–	10	ns	Fig. 20-4
Address delay time	t_{AD}	–	50	–	35	–	30	ns	Fig. 20-4
Address hold time	t_{AH}	20	–	15	–	10	–	ns	Fig. 20-4
Address strobe delay time	t_{ASD}	–	40	–	35	–	30	ns	Fig. 20-4
Write strobe delay time	t_{WSD}	–	50	–	35	–	30	ns	Fig. 20-4
Strobe delay time	t_{SD}	–	50	–	35	–	30	ns	Fig. 20-4
Write strobe pulse width*	t_{WSW}	120	–	95	–	65	–	ns	Fig. 20-4
Address setup time 1*	t_{AS1}	15	–	10	–	10	–	ns	Fig. 20-4
Address setup time 2*	t_{AS2}	65	–	50	–	40	–	ns	Fig. 20-4
Read data setup time	t_{RDS}	35	–	20	–	20	–	ns	Fig. 20-4
Read data hold time*	t_{RDH}	0	–	0	–	0	–	ns	Fig. 20-4
Read data access time*	t_{ACC}	–	170	–	160	–	110	ns	Fig. 20-4
Write data delay time	t_{WDD}	–	75	–	60	–	60	ns	Fig. 20-4
Write data setup time	t_{WDS}	5	–	5	–	5	–	ns	Fig. 20-4
Write data hold time	t_{WDH}	20	–	20	–	20	–	ns	Fig. 20-4
Wait setup time	t_{WTS}	40	–	35	–	30	–	ns	Fig. 20-5
Wait hold time	t_{WTH}	10	–	10	–	10	–	ns	Fig. 20-5

Note: * Values at maximum operating frequency

Table 20-8 Control Signal Timing — Preliminary —

Condition A: $V_{CC} = V_{CC}B = 5.0\ V \pm 10\%$, $V_{SS} = 0\ V$, $\phi = 2.0$ MHz to maximum operating frequency, Ta = –20 to 75°C (regular specifications), Ta = –40 to 85°C (wide-range specifications)

Condition B: $V_{CC} = V_{CC}B = 2.7\ V$ to $3.6\ V$, $V_{SS} = 0\ V$, $\phi = 2.0$ MHz to maximum operating frequency, Ta = –20 to 75°C

		Condition B		Condition A					
		10 MHz		12 MHz		16 MHz			
Item	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
RES setup time	t_{RESS}	300	–	200	–	200	–	ns	Fig. 20-6
RES pulse width	t_{RESW}	10	–	10	–	10	–	t_{cyc}	Fig. 20-6
RESO output delay time	t_{RESD}	—	200	—	100	—	100	ns	Fig. 20-22
RESO output pulse width	t_{RESOW}	132	—	132	—	132	—	t_{cyc}	
NMI setup time (NMI, $\overline{IRQ_0}$ to $\overline{IRQ_7}$)	t_{NMIS}	300	–	150	–	150	–	ns	Fig. 20-7
NMI hold time (NMI, $\overline{IRQ_0}$ to $\overline{IRQ_7}$)	t_{NMIH}	10	–	10	–	10	–	ns	Fig. 20-7
Interrupt pulse width for recovery from software standby mode (NMI, $\overline{IRQ_0}$ to $\overline{IRQ_2}$)	t_{NMIW}	300	–	200	–	200	–	ns	Fig. 20-7
Crystal oscillator settling time (reset)	t_{OSC1}	20	–	20	–	20	–	ms	Fig. 20-8
Crystal oscillator settling time (software standby)	t_{OSC2}	8	–	8	–	8	–	ms	Fig. 20-9

- **Measurement Conditions for AC Characteristics**

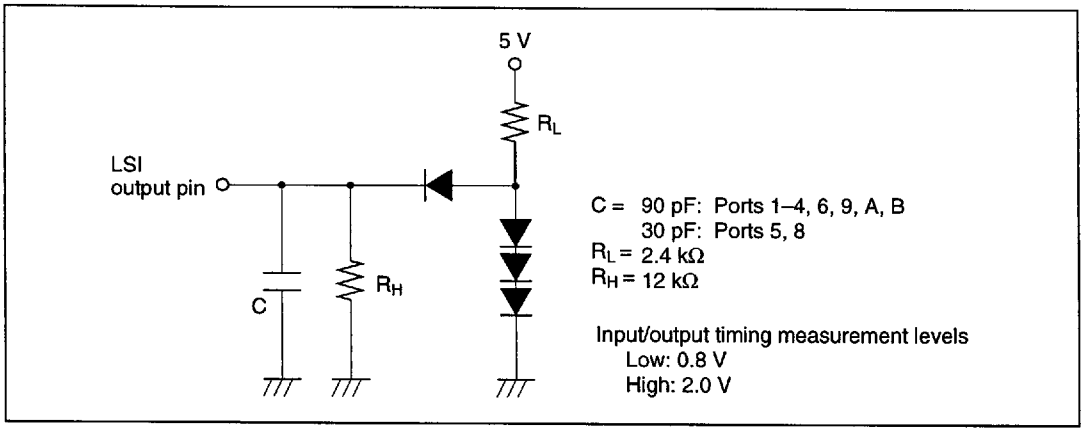


Figure 20-3 Measurement Conditions for A/C Characteristics

Table 20-9 Timing Conditions of On-Chip Supporting Modules **— Preliminary —**

Condition A: $V_{CC} = V_{CC}B = 5.0\ V \pm 10\%$, $V_{SS} = 0\ V$, $\phi = 2.0$ MHz to maximum operating frequency, Ta = –20 to 75°C (regular specifications), Ta = –40 to 85°C (wide-range specifications)

Condition B: $V_{CC} = V_{CC}B = 2.7\ V$ to $3.6\ V$, $V_{SS} = 0\ V$, $\phi = 2.0$ MHz to maximum operating frequency, Ta = –20 to 75°C

			Condition B		Condition A					
			10 MHz		12 MHz		16 MHz			
Item		Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
FRT	Timer output delay time	t_{FTOD}	–	150	–	100	–	100	ns	Fig. 20-10
	Timer input setup time	t_{FTIS}	80	–	50	–	50	–	ns	Fig. 20-10
	Timer clock input setup time	t_{FTCS}	80	–	50	–	50	–	ns	Fig. 20-11
	Timer clock pulse width	t_{FTCWH} t_{FTCWL}	1.5	–	1.5	–	1.5	–	t_{cyc}	Fig. 20-11
TMR	Timer output delay time	t_{TMOD}	–	150	–	100	–	100	ns	Fig. 20-12
	Timer reset input setup time	t_{TMRS}	80	–	50	–	50	–	ns	Fig. 20-14
	Timer clock input setup time	t_{TMCS}	80	–	50	–	50	–	ns	Fig. 20-13
	Timer clock pulse width (single edge)	t_{TMCWH}	1.5	–	1.5	–	1.5	–	t_{cyc}	Fig. 20-13
	Timer clock pulse width (both edges)	t_{TMCWL}	2.5	–	2.5	–	2.5	–	t_{cyc}	Fig. 20-13
PWM	Timer output delay time	t_{PWOD}	–	150	–	100	–	100	ns	Fig. 20-15
SCI	Input clock cycle (Async)	t_{Scyc}	4	–	4	–	4	–	t_{cyc}	Fig. 20-16
	(Sync)	t_{Scyc}	6	–	6	–	6	–	t_{cyc}	Fig. 20-16
	Transmit data delay time (Sync)	t_{TXD}	–	200	–	100	–	100	ns	Fig. 20-16
	Receive data setup time (Sync)	t_{RXS}	150	–	100	–	100	–	ns	Fig. 20-16
	Receive data hold time (Sync)	t_{RXH}	150	–	100	–	100	–	ns	Fig. 20-16
	Input clock pulse width	t_{SCKW}	0.4	0.6	0.4	0.6	0.4	0.6	t_{Scyc}	Fig. 20-17
Ports	Output data delay time	t_{PWD}	–	150	–	100	–	100	ns	Fig. 20-18
	Input data setup time	t_{PRS}	80	–	50	–	50	–	ns	Fig. 20-18
	Input data hold time	t_{PRH}	80	–	50	–	50	–	ns	Fig. 20-18

Table 20-9 Timing Conditions of On-Chip Supporting Modules (cont) **— Preliminary —**

Condition A: $V_{CC} = V_{CC}B = 5.0\ V \pm 10\%$, $V_{SS} = 0\ V$, $\phi = 2.0$ MHz to maximum operating frequency, Ta = –20 to 75°C (regular specifications), Ta = –40 to 85°C (wide-range specifications)

Condition B: $V_{CC} = V_{CC}B = 2.7\ V$ to $3.6\ V$, $V_{SS} = 0\ V$, $\phi = 2.0$ MHz to maximum operating frequency, Ta = –20 to 75°C

			Condition B		Condition A					
			10 MHz		12 MHz		16 MHz			
Item		Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
HIF read cycle	CS/HA_0 setup time	t_{HAR}	10	—	10	—	10	—	ns	Fig. 20-19
	CS/HA_0 hold time	t_{HRA}	10	—	10	—	10	—	ns	Fig. 20-19
	IOR pulse width	t_{HRPW}	220	—	120	—	120	—	ns	Fig. 20-19
	HDB delay time	t_{HRD}	—	200	—	100	—	100	ns	Fig. 20-19
	HDB hold time	t_{HRF}	0	40	0	25	0	25	ns	Fig. 20-19
	HIRQ delay time	t_{HIRQ}	—	200	—	120	—	120	ns	Fig. 20-19
HIF write cycle	CS/HA_0 setup time	t_{HAW}	10	—	10	—	10	—	ns	Fig. 20-20
	CS/HA_0 hold time	t_{HWA}	10	—	10	—	10	—	ns	Fig. 20-20
	IOW pulse width	t_{HWPW}	100	—	60	—	60	—	ns	Fig. 20-20
	HDB setup time	t_{HDW}	50	—	30	—	30	—	ns	Fig. 20-20
	HDB hold time	t_{HWD}	25	—	15	—	15	—	ns	Fig. 20-20
	GA_{20} delay time	t_{HGA}	—	180	—	90	—	90	ns	Fig. 20-20

Table 20-10 I²C Bus Timing — Preliminary —

Conditions: V_{CC} = 2.7 V to 5.5 V, $V_{CC}B$ = 5 V ±10%, V_{SS} = 0 V, Ta = –20 to +75°C

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Note
SCL clock cycle time	t_{SCL}	12 t_{cyc}	—	—	ns		Fig. 20-2
SCL clock high pulse width	t_{SCLH}	3 t_{cyc}	—	—	ns		Fig. 20-2
SCL clock low pulse width	t_{SCLL}	5 t_{cyc}	—	—	ns		Fig. 20-2
SCL and SDA rise time	t_{Sr}	—	—	1000	ns	Normal mode 100 kbits/s (max)	Fig. 20-2
		20 + 0.1C_b	—	300		High-speed mode 400 kbits/s (max)	
SCL and SDA fall time	t_{Sf}	—	—	300	ns	Normal mode 100 kbits/s (max)	Fig. 20-2
		20 + 0.1C_b	—	300		High-speed mode 400 kbits/s (max)	
SDA bus-free time	t_{BUF}	7 t_{cyc} – 300	—	—	ns		Fig. 20-2
SCL start condition hold time	t_{STAH}	3 t_{cyc}	—	—	ns		Fig. 20-2
SCL resend start condition setup time	t_{STAS}	3 t_{cyc}	—	—	ns		Fig. 20-2
SDA stop condition setup time	t_{STOS}	3 t_{cyc}	—	—	ns		Fig. 20-2
SDA data setup time	t_{SDAS}	3 t_{cyc} + 50	—	—	ns		Fig. 20-2
SDA data hold time	t_{SDAH}	0	—	—	ns		Fig. 20-2
SDA load capacitance	C_b	—	—	400	pF		Fig. 20-2

20.2.3 A/D Converter Characteristics

Table 20-11 lists the characteristics of the on-chip A/D converter.

Table 20-11 A/D Converter Characteristics **— Preliminary —**

Condition A: $V_{CC} = V_{CC}B = 5.0\ V \pm 10\%$, $AV_{CC} = 5.0\ V \pm 10\%$, $AV_{ref} = 4.5\ V$ to AV_{CC}, $V_{SS} = AV_{SS} = 0\ V$, $\phi = 2.0$ MHz to maximum operating frequency, Ta = –20 to 75°C (regular specifications), Ta = –40 to 85°C (wide-range specifications)

Condition B1: $V_{CC} = V_{CC}B = 2.7\ V$ to $3.6\ V$, $AV_{CC} = 5.0\ V \pm 10\%$, $AV_{ref} = 4.5\ V$ to AV_{CC}, $V_{SS} = AV_{SS} = 0\ V$, $\phi = 2.0$ MHz to maximum operating frequency, Ta = –20 to 75°C

Condition B2: $V_{CC} = V_{CC}B = 2.7\ V$ to $3.6\ V$, $AV_{CC} = 2.7\ V$ to $3.6\ V$, $AV_{ref} = 2.7\ V$ to AV_{CC}, $V_{SS} = AV_{SS} = 0\ V$, $\phi = 2$ MHz to maximum operating frequency, Ta = –20 to 75°C

	Condition B2			Condition B1			Condition A			
	10 MHz			10 MHz			16 MHz			
Item	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
Resolution	8	8	8	8	8	8	8	8	8	Bits
Conversion time (single mode)*	—	—	13.4	—	—	13.4	—	—	8.4	µs
Analog input capacitance	—	—	20	—	—	20	—	—	20	pF
Allowable signal source impedance	—	—	5	—	—	10	—	—	10	kΩ
Nonlinearity error	—	—	±6.0	—	—	±3.0	—	—	±3.0	LSB
Offset error	—	—	±4.0	—	—	±2.0	—	—	±2.0	LSB
Full-scale error	—	—	±4.0	—	—	±2.0	—	—	±2.0	LSB
Quantizing error	—	—	±0.5	—	—	±0.5	—	—	±0.5	LSB
Absolute accuracy	—	—	±8.0	—	—	±4.0	—	—	±4.0	LSB

Note: * Values at maximum operating frequency

20.2.4 D/A Converter Characteristics

Table 20-12 lists the characteristics of the on-chip D/A converter.

Table 20-12 D/A Converter Characteristics **— Preliminary —**

Condition A: $V_{CC} = V_{CC}B = 5.0\ V \pm 10\%$, $AV_{CC} = 5.0\ V \pm 10\%$, $AV_{ref} = 4.5\ V$ to AV_{CC}, $V_{SS} = AV_{SS} = 0\ V$, $\phi = 2.0$ MHz to maximum operating frequency, Ta = –20 to 75°C (regular specifications), Ta = –40 to 85°C (wide-range specifications)

Condition B1: $V_{CC} = V_{CC}B = 2.7\ V$ to $3.6\ V$, $AV_{CC} = 5.0\ V \pm 10\%$, $AV_{ref} = 4.5\ V$ to AV_{CC}, $V_{SS} = AV_{SS} = 0\ V$, $\phi = 2.0$ MHz to maximum operating frequency, Ta = –20 to 75°C

Condition B2: $V_{CC} = V_{CC}B = 2.7\ V$ to $3.6\ V$, $AV_{CC} = 2.7\ V$ to $3.6\ V$, $AV_{ref} = 2.7\ V$ to AV_{CC}, $V_{SS} = AV_{SS} = 0\ V$, $\phi = 2$ MHz to maximum operating frequency, Ta = –20 to 75°C

	Condition B2			Condition B1			Condition A				
	10 MHz			10 MHz			16 MHz				
Item	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions
Resolution	8	8	8	8	8	8	8	8	8	Bits	
Conversion time (setting time)	—	—	10.0	—	—	10.0	—	—	10.0	µs	30 pF load capacitance
Absolute accuracy	—	±2.0	±3.0	—	±1.0	±1.5	—	±1.0	±1.5	LSB	2 MΩ load resistance
	—	—	±2.0	—	—	±1.0	—	—	±1.0	LSB	4 MΩ load resistance

20.3 MCU Operational Timing

This section provides the following timing charts:

20.3.1 Bus Timing

(1) Basic Bus Cycle (without Wait States) in Expanded Modes

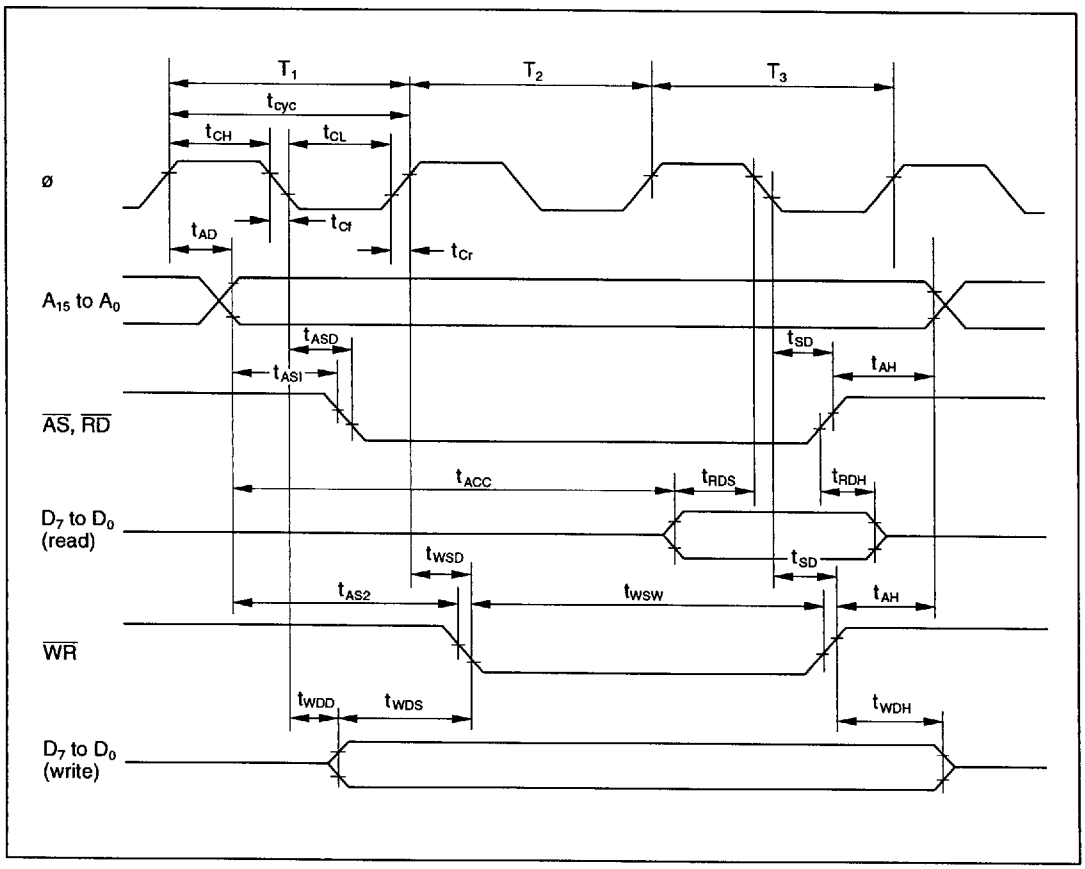


Figure 20-4 Basic Bus Cycle (without Wait States) in Expanded Modes

(2) Basic Bus Cycle (with 1 Wait State) in Expanded Modes

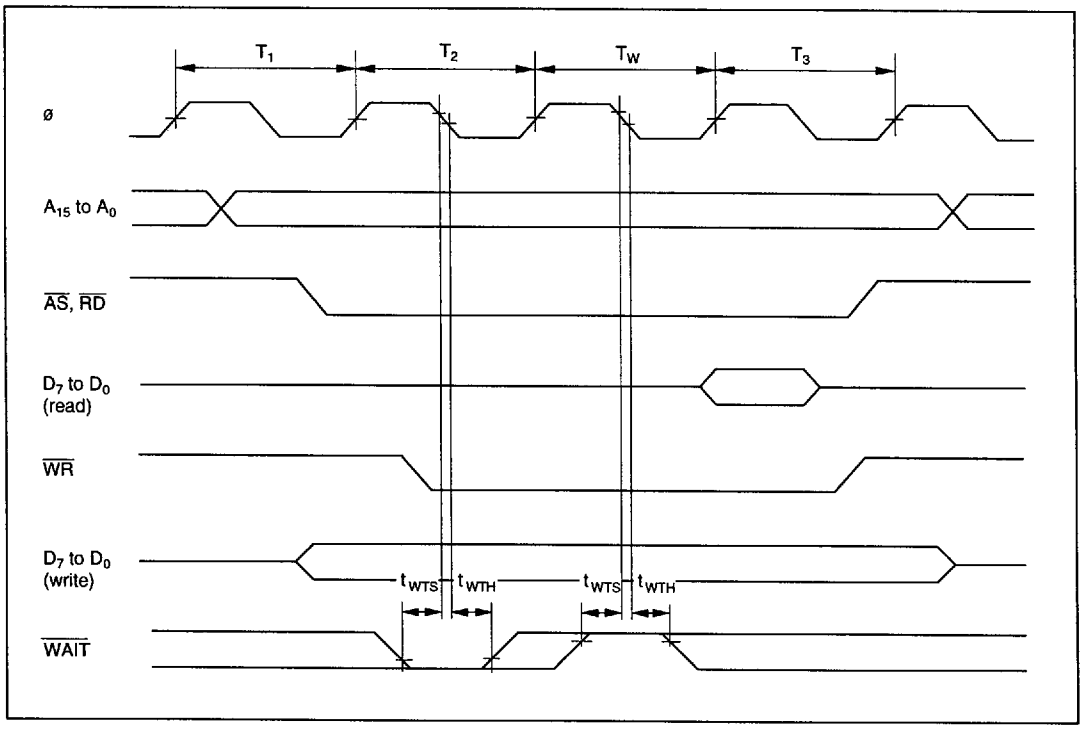


Figure 20-5 Basic Bus Cycle (with 1 Wait State) in Expanded Modes

20.3.2 Control Signal Timing

(1) Reset Input Timing

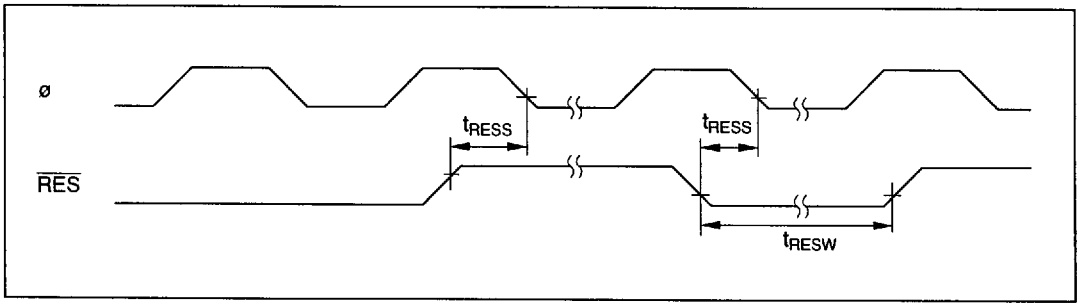


Figure 20-6 Reset Input Timing

(2) Interrupt Input Timing

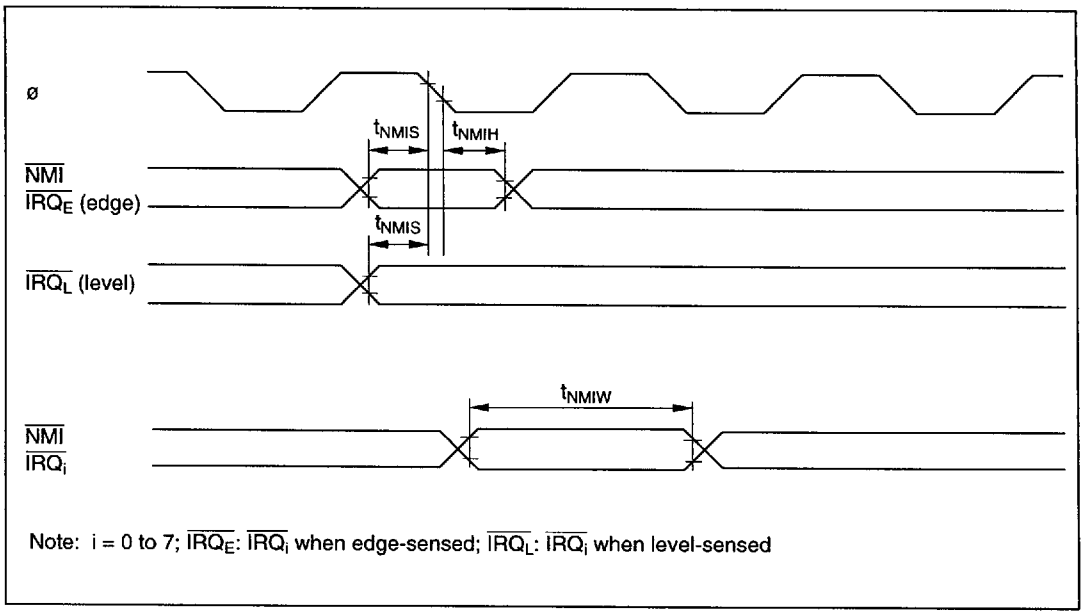


Figure 20-7 Interrupt Input Timing

(3) Clock Settling Timing

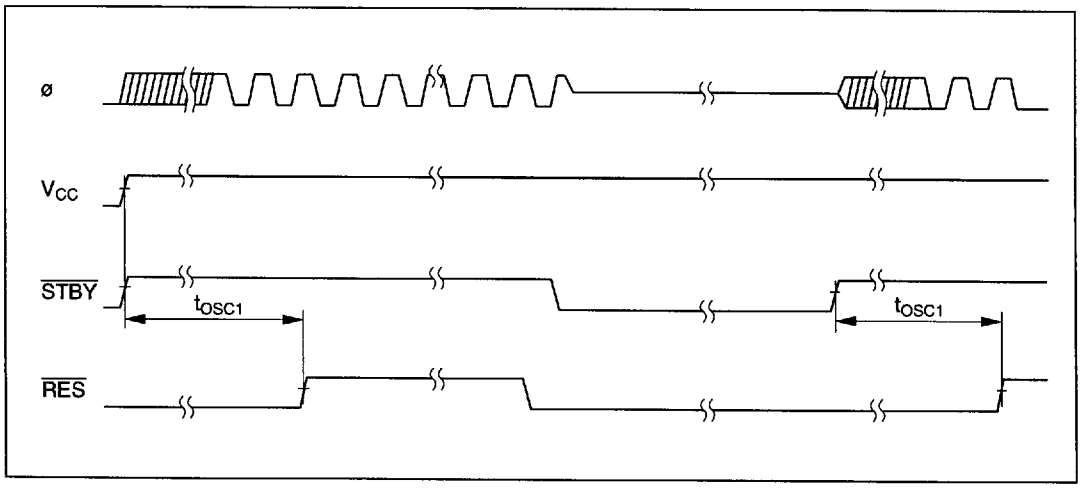


Figure 20-8 Clock Settling Timing

(4) Clock Settling Timing for Recovery from Software Standby Mode

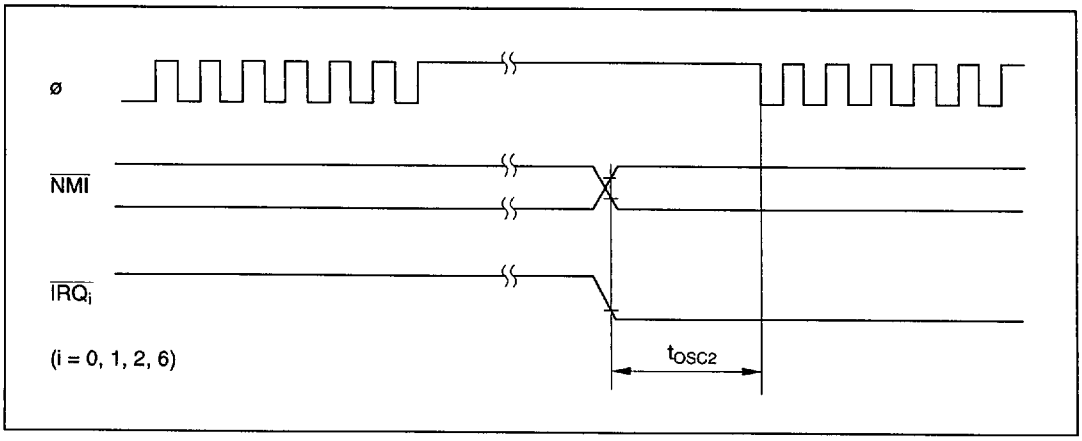


Figure 20-9 Clock Settling Timing for Recovery from Software Standby Mode

20.3.3 16-Bit Free-Running Timer Timing

(1) Free-Running Timer Input/Output Timing

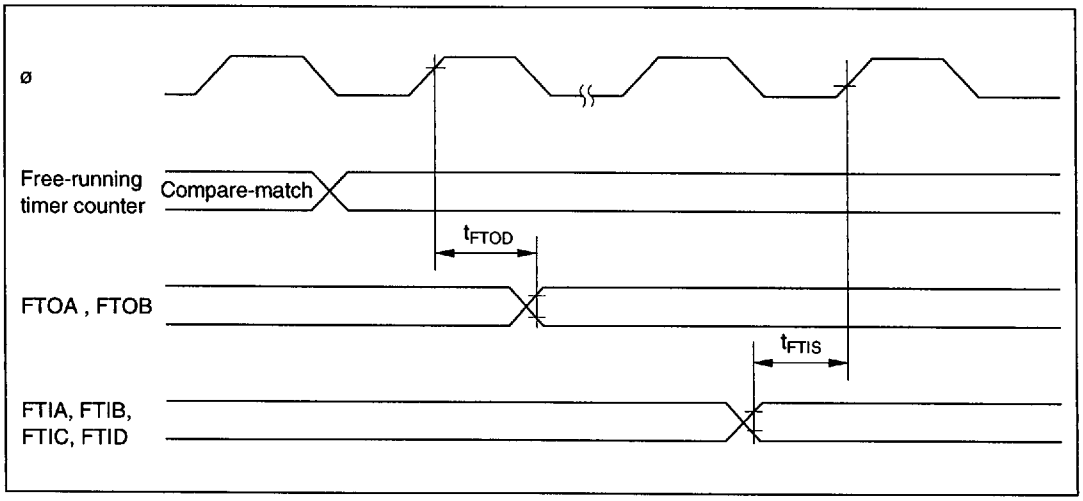


Figure 20-10 Free-Running Timer Input/Output Timing

(2) External Clock Input Timing for Free-Running Timer

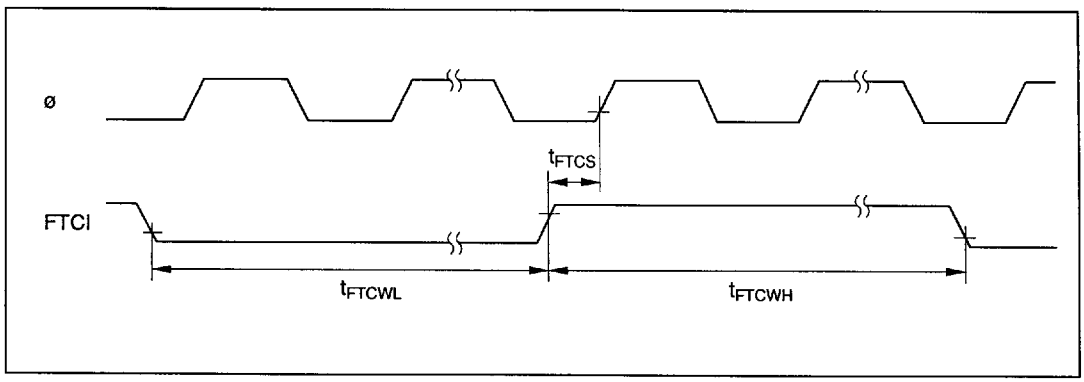


Figure 20-11 External Clock Input Timing for Free-Running Timer

20.3.4 8-Bit Timer Timing

(1) 8-Bit Timer Output Timing

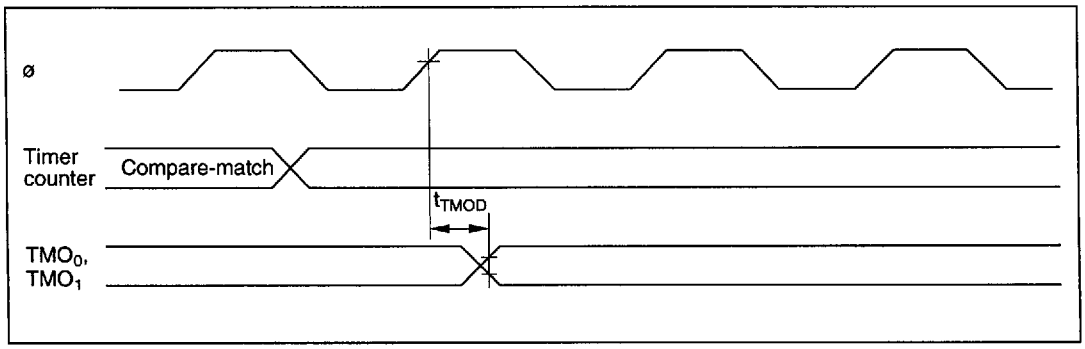


Figure 20-12 8-Bit Timer Output Timing

(2) 8-Bit Timer Clock Input Timing

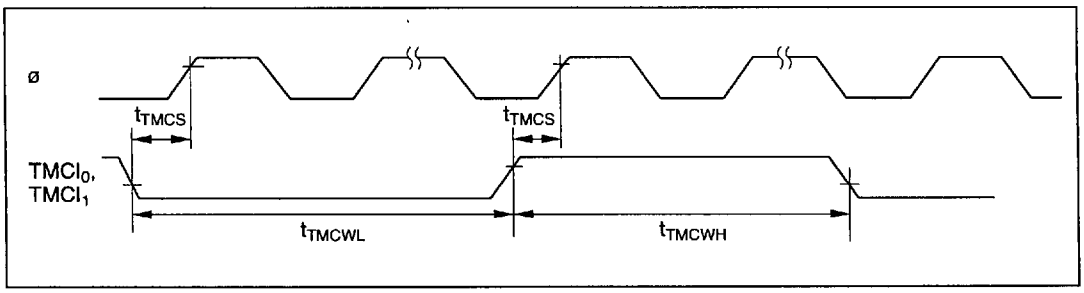


Figure 20-13 8-Bit Timer Clock Input Timing

(3) 8-Bit Timer Reset Input Timing

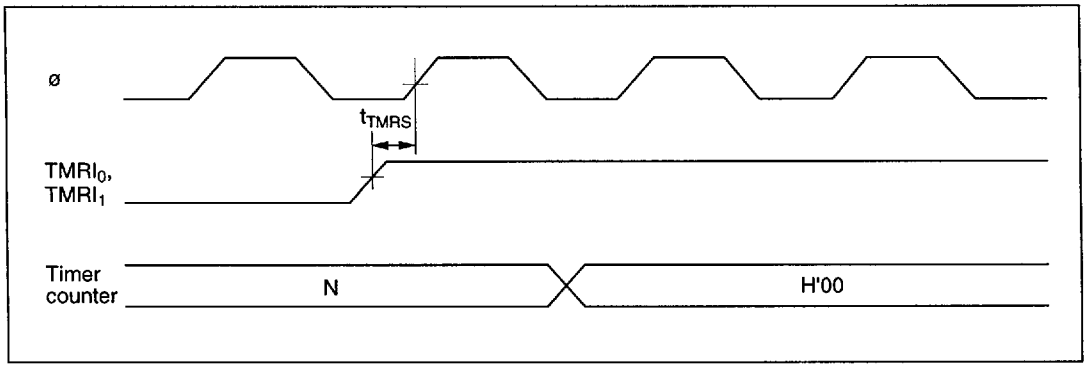


Figure 20-14 8-Bit Timer Reset Input Timing

20.3.5 Pulse Width Modulation Timer Timing

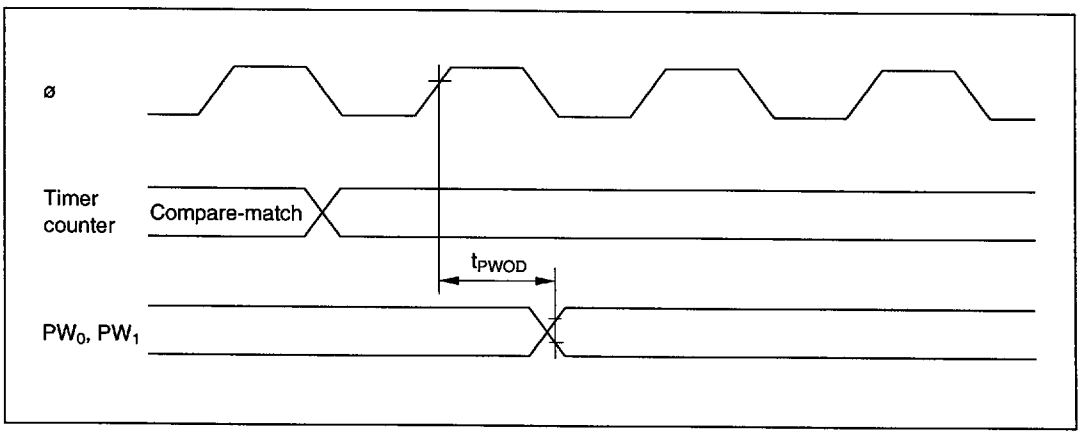


Figure 20-15 PWM Timer Output Timing

20.3.6 Serial Communication Interface Timing

(1) SCI Input/Output Timing

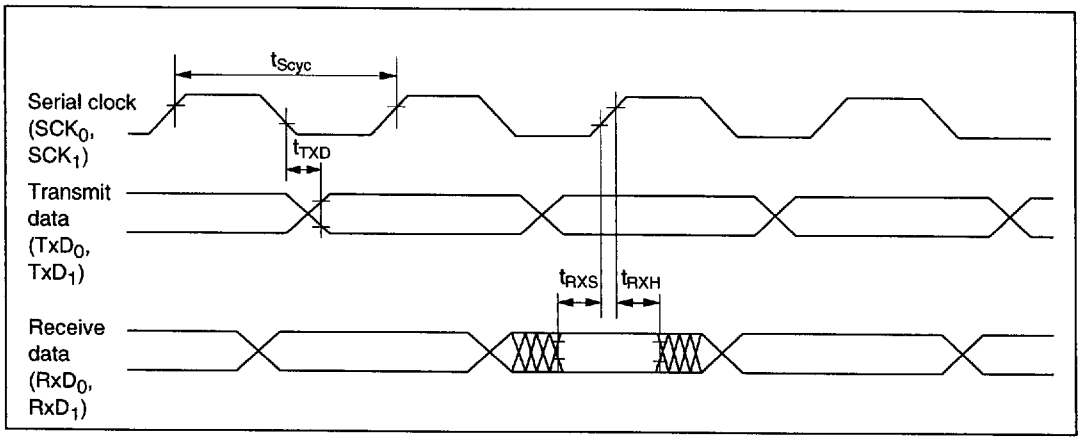


Figure 20-16 SCI Input/Output Timing (Synchronous Mode)

(2) SCI Input Clock Timing

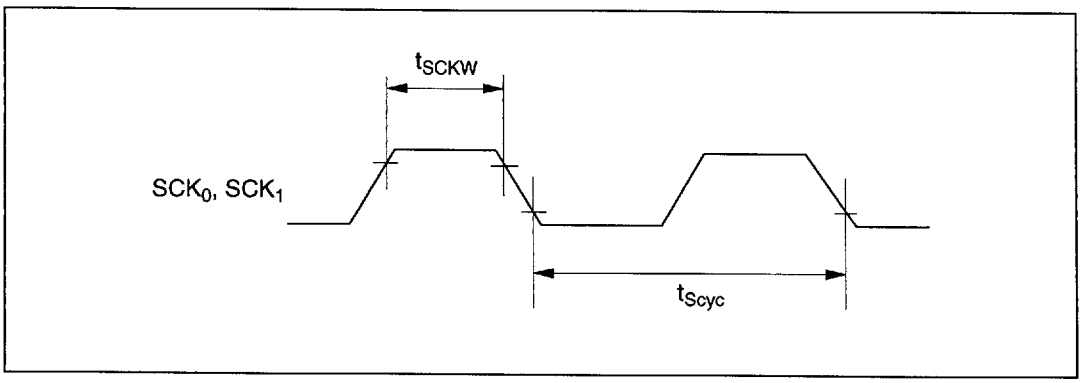


Figure 20-17 SCI Input Clock Timing

20.3.7 I/O Port Timing

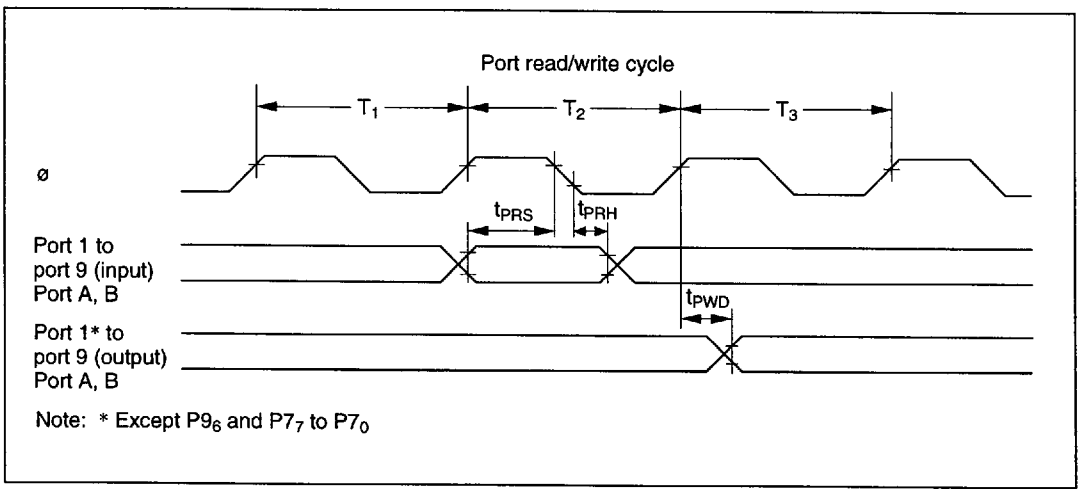
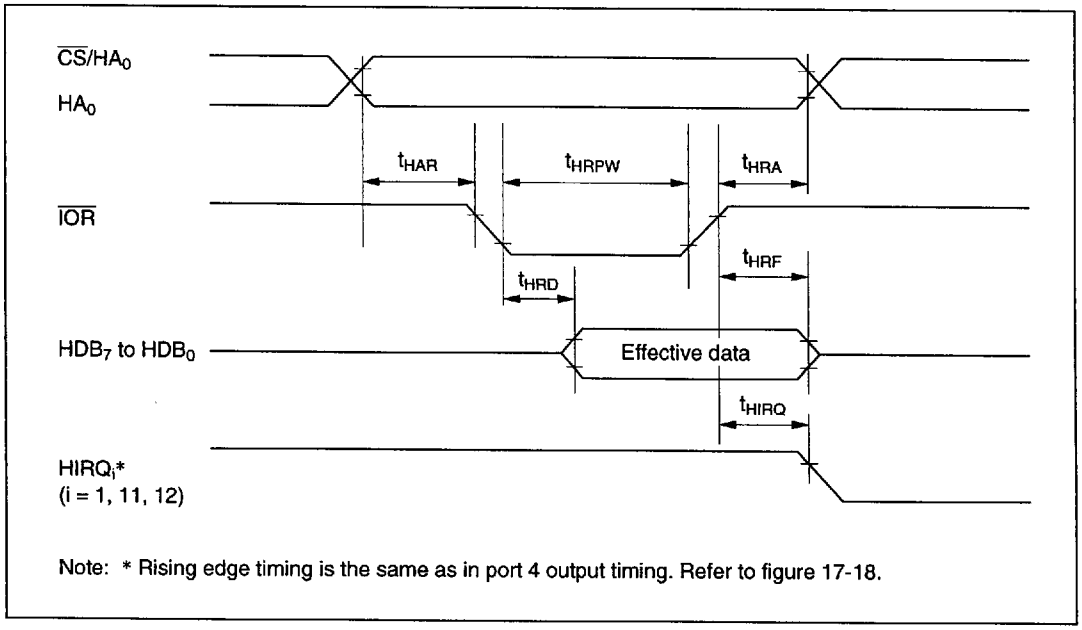


Figure 20-18 I/O Port Input/Output Timing

20.3.8 Host Interface Timing

(1) Host Interface Read Timing



Note: * Rising edge timing is the same as in port 4 output timing. Refer to figure 17-18.

Figure 20-19 Host Interface Read Timing

(2) Host Interface Write Timing

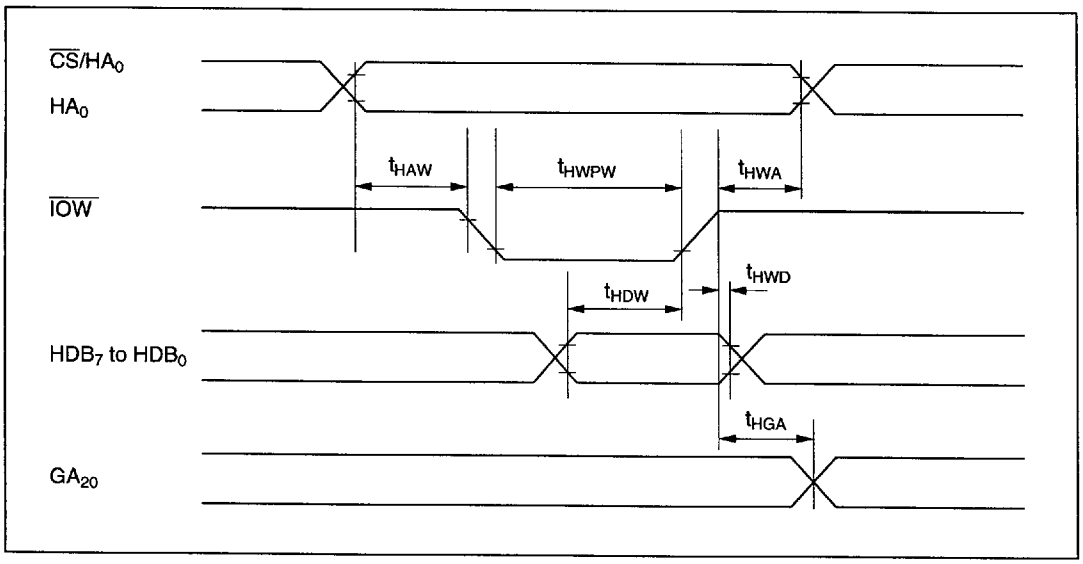


Figure 20-20 Host Interface Write Timing

20.3.9 I²C Bus Timing

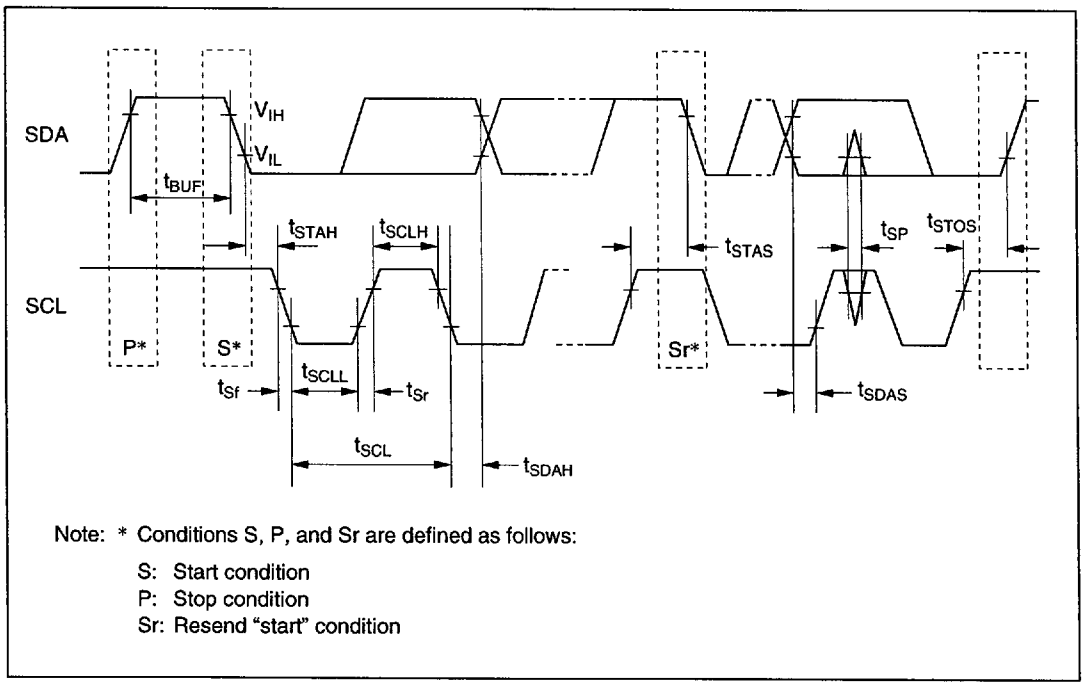


Figure 20-21 I²C Bus Interface I/O Timing

20.3.10 Reset Output Timing

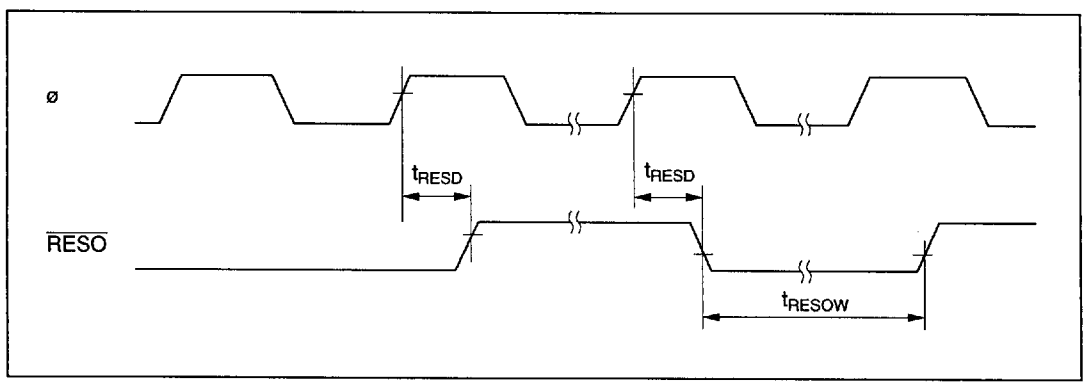


Figure 20-22 Reset Output Timing