T-49-17-34

FireFox 386SX
Chipset Specifications

Process technology used	1.0μ CMOS
CPUs supported	Intel 80386SX Am386DX Cyrix 486SLC
CPU speed supported	16/20/25/33/40 MHz
Coprocessor supported in 386 system (No external PALS required)	Intel 80387/ Cyrix/IIT/ULSI/ WEITEK/3167
AT clock generation	Asynchronous
Programmable AT bus clock	Yes
Hardware/Software turbo switching	Yes
Page Mode DRAM control	Yes
DRAM type supported	256K/1M/4M
Max physical memory	16 MB
Mixing DRAMS	Yes
Hidden refresh	Yes
Shadow RAM range maximum size/block size	256 KB/64KB
Support Local Bus	Yes
PQFP package	160
Programmable wait states	Yes
On chip cache controller	Yes
Support 8kx8 and 8kx9 Tag RAM	Yes
Cache update scheme	Write back
Cache organization	Direct mapped
Data cache size	16/32/64/128KB
Non-cacheable support	Yes
Each non-cacheable region size	512KB-32MB
Zero wait state cache read hit	Yes
Zero wait state cache write hit	Yes
External TTL component	12
SRAM speed required @ 40MHz	80ns
SRAM speed required @ 33MHz	80ns
SRAM speed required @ 25MHz	80ns
Fast gate A20	Yes
Fast reset	Yes
22cm x 22cm half baby AT board	Yes

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