FAIRCHILD SEMICONDUCTOR®

January 2007

FDMC3300NZA

Monolithic Common Drain N-Channel 2.5V Specified PowerTrench® MOSFET
20V, 8A, 26mΩ

Features

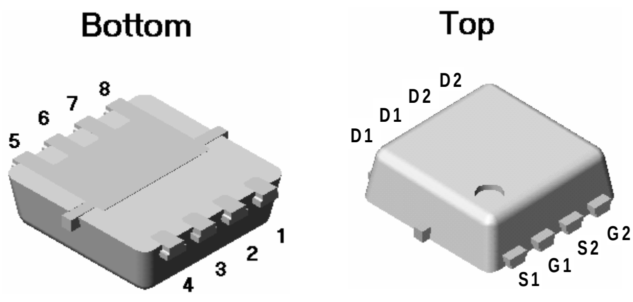
- Max $r_{DS(on)}$ = 26mΩ at V_{GS} = 4.5V, I_D = 8.0A
- Max $r_{DS(on)}$ = 34mΩ at V_{GS} = 2.5V, I_D = 7.0A
- >2000V ESD protection
- Low Profile - 1mm maximum - in the new package MLP 3.3x3.3 mm
- RoHS Compliant

General Description

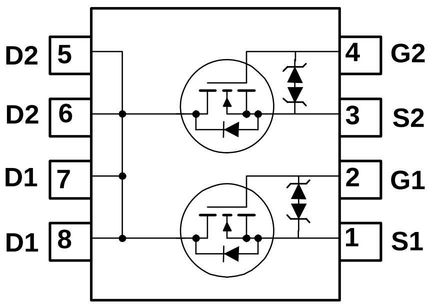
This dual N-Channel MOSFET has been designed using Fairchild Semiconductor's advanced PowerTrench® process to optimize the $r_{DS(on)}$ @ V_{GS} = 2.5V on special MLP lead frame with all the drains on one side of the package.

Application

- Li-Ion Battery Pack



Power 33



MOSFET Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		Rating	Units
V_{DS}	Drain to Source Voltage		20	V
V_{GS}	Gate to Source Voltage		±12	V
I_D	Drain Current -Continuous	(Note 1a)	8	A
	-Pulsed		40	
P_D	Power Dissipation (Steady State)	(Note 1a)	2.1	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range		-55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	60	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	135	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
3300A	FDMC3300NZA	Power 33	7”	8mm	3000 units

Electrical Characteristics T_J = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units

Off Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250µA, V_{GS} = 0V	20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250µA, referenced to 25°C		12		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 16V, V_{GS} = 0V			1	µA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±12V, V_{DS}= 0V			±10	µA

On Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250µA	0.6		1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250µA, referenced to 25°C		-3.1		mV/°C
$r_{DS(on)}$	Drain to Source On Resistance	V_{GS} = 4.5V, I_D = 8.0A		20	26	mΩ
		V_{GS} = 2.5V, I_D = 7.0A		25	34	
		V_{GS} = 4.5V, I_D = 8.0A, T_J = 150°C		26	35	
g_{FS}	Forward Transconductance	V_{DS} = 5V, I_D = 8.0A		29		S

Dynamic Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
C_{iss}	Input Capacitance	V_{DS} = 10V, V_{GS} = 0V, f = 1MHZ		610	815	pF
C_{oss}	Output Capacitance			165	220	pF
C_{rss}	Reverse Transfer Capacitance			115	175	pF
R_g	Gate Resistance	f = 1MHz		1.7		Ω

Switching Characteristics

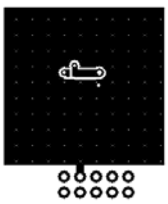
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 10V, I_D = 1.0A V_{GS} = 4.5V, R_{GEN} = 6.0Ω		8	16	ns
t_r	Rise Time			8	16	ns
$t_{d(off)}$	Turn-Off Delay Time			19	34	ns
t_f	Fall Time			9	18	ns
$Q_{g(TOT)}$	Total Gate Charge at 4.5V	V_{GS} = 0V to 4.5V; V_{DD} = 10V, I_D = 8.0A		8	12	nC
Q_{gs}	Gate to Source Gate Charge			1		nC
Q_{gd}	Gate to Drain “Miller” Charge			2		nC

Drain-Source Diode Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0V, I_S = 2.0A (Note 2)		0.7	1.2	V
t_{rr}	Reverse Recovery Time	I_F = 8.0A, di/dt = 100A/µs			21	ns
Q_{rr}	Reverse Recovery Charge				6	nC

Notes:

1: $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.
(a)$R_{\theta JA}$ = 60°C/W when mounted on a 1 in^2 pad of 2 oz copper, 1.5’x1.5’x0.062’ thick PCB.
(b)$R_{\theta JA}$ = 135°C/W when mounted on a minimum pad of 2 oz copper.



a. 60°C/W when mounted on a 1 in^2 pad of 2 oz copper

b. 135°C/W when mounted on a minimum pad of 2 oz copper

2: Pulse Test: Pulse Width < 300µs, Duty cycle < 2.0%.

Typical Characteristics T_J = 25°C unless otherwise noted

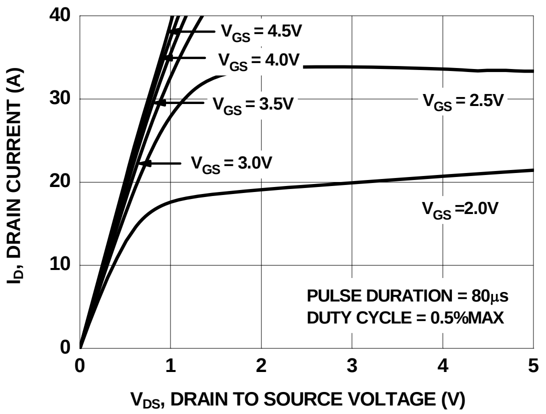


Figure 1. On Region Characteristics

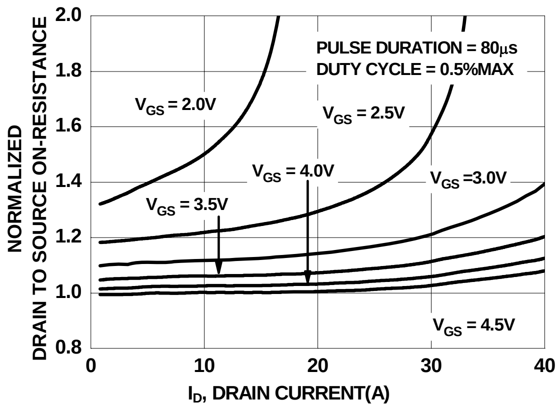


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

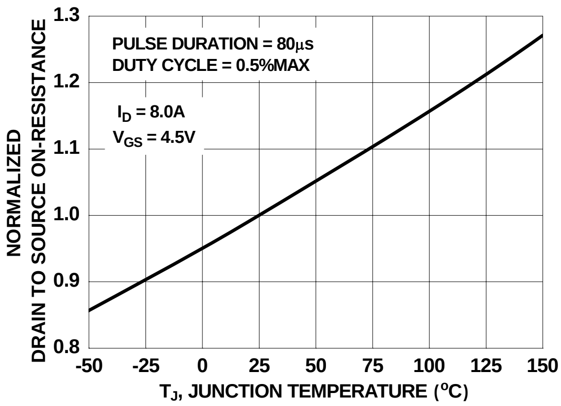


Figure 3. Normalized On Resistance vs Junction Temperature

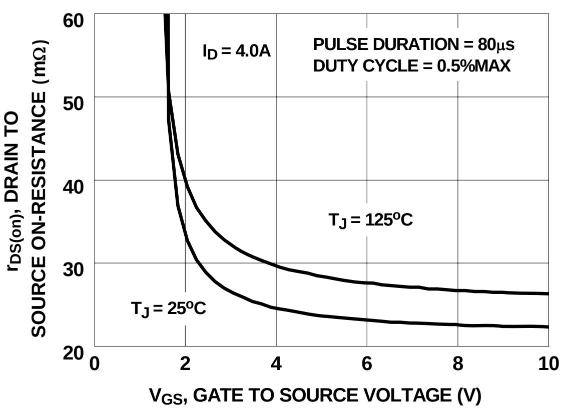


Figure 4. On-Resistance vs Gate to Source Voltage

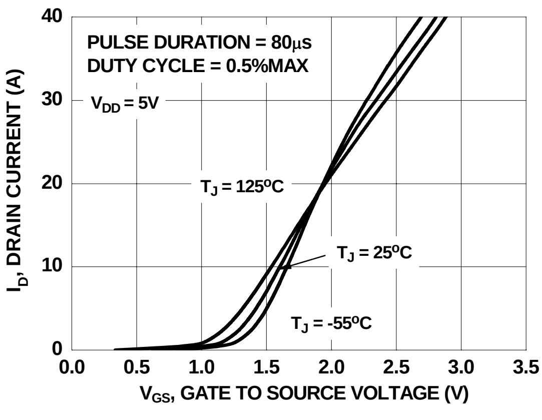


Figure 5. Transfer Characteristics

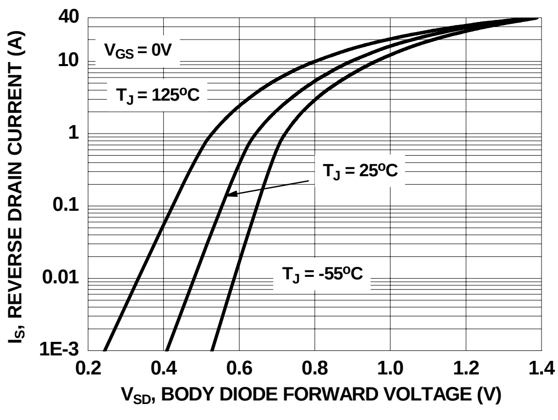


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics T_J = 25°C unless otherwise noted

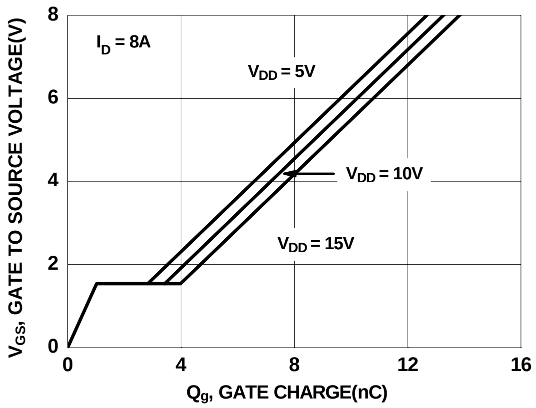


Figure 7. Gate Charge Characteristics

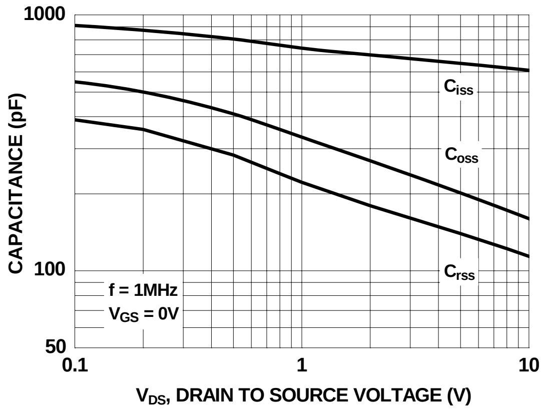


Figure 8. Capacitance vs Drain to Source Voltage

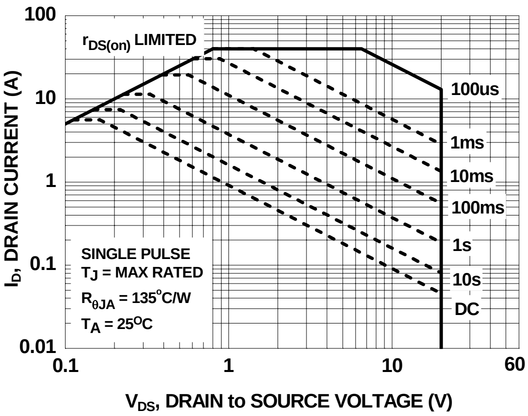


Figure 9. Forward Bias Safe Operating Area

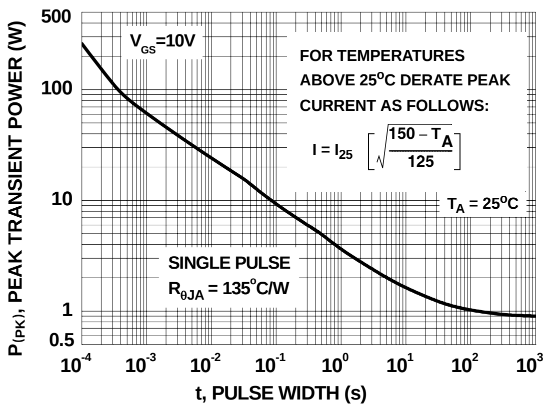


Figure 10. Single Pulse Maximum Power Dissipation

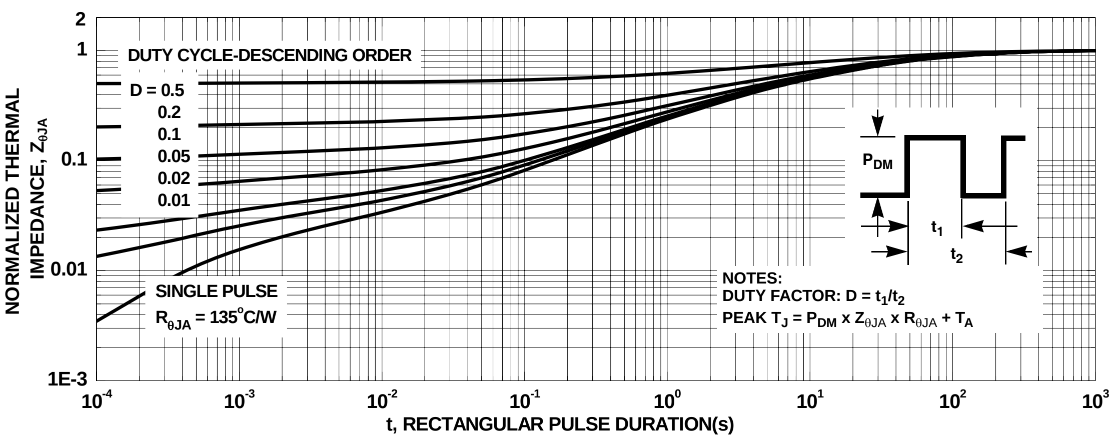
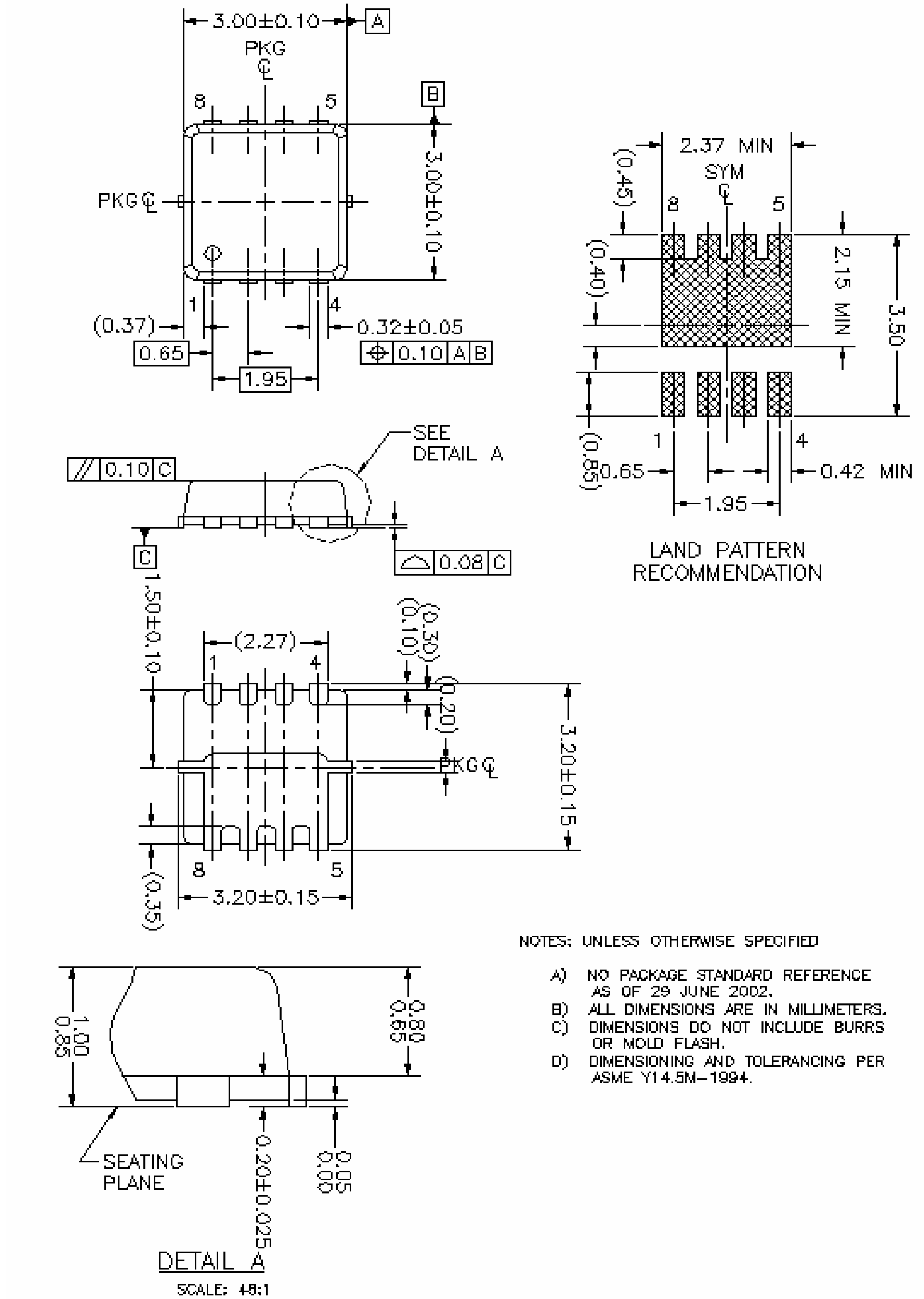


Figure 11. Transient Thermal Response Curve



NOTES: UNLESS OTHERWISE SPECIFIED

A) NO PACKAGE STANDARD REFERENCE AS OF 29 JUNE 2002.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH.
D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.

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