



## DM76S64/DM86S64 Bipolar Character Generator

### General Description

The DM76S64/DM86S64 is a 64-character bipolar character generator with serial output designed primarily for the CRT display marketplace, and packaged in a standard 16-pin DIP. The DM76S64/DM86S64 incorporates several CRT system level functions, as well as a 7 x 9 or 5 x 7 row scan character font. The DM76S64/DM86S64 performs the system functions of parallel to serial shifting, character address latching, character spacing and character line spacing. These system functions have required extra packages in the past.

Shifted characters can be generated by the on-chip subtractor.

The clear input and the load enable input are active low. Load enable is synchronous with the dot clock. Both the line clock and the dot clock are positive edge-triggered. When the address latch control signal is high,

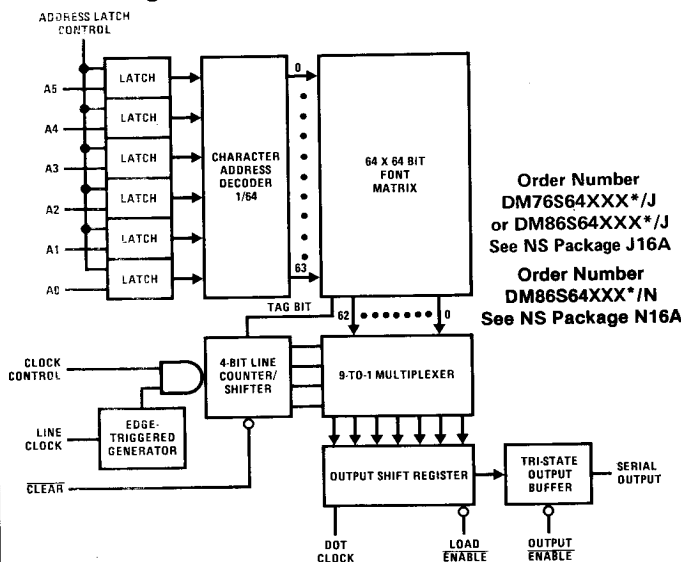
the character addresses "fall through" the latch. And when the address latch control signal goes low, the character addresses are latched.

### Features

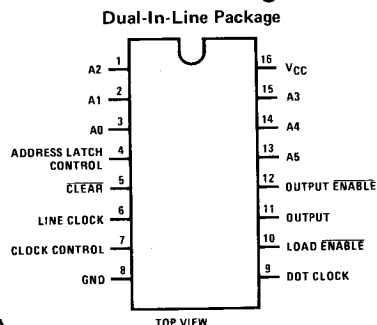
- 64-character—row scan
- 5 x 7 or 7 x 9 font
- Custom fonts available with shift options
- Serial output
- 16-pin package
- 35 MHz typ clock rate
- On-chip input latches
- On-chip shift register
- On-chip dot blanking
- On-chip row blanking
- TRI-STATE® output

|                       | 7 x 9 | 5 x 7 | FONT                       | PACKAGE |
|-----------------------|-------|-------|----------------------------|---------|
| DM76S64BWF/DM86S64BWF | X     |       | Upper Case Block Letters   | N, J    |
| DM76S64CAE/DM86S64CAE | X     |       | Shifted Lower Case Block   | N, J    |
| DM76S64CAB/DM86S64CAB |       | X     | Upper Case Block Letters   | N, J    |
| DM76S64CAH/DM86S64CAH |       | X     | Shifted Lower Case Block   | N, J    |
| DM76S64CTA/DM86S64CTA | X     |       | ASCII Character Set        | N, J    |
| DM76S64CTB/DM86S64CTB | X     |       | ASCII Numerals and Control | N, J    |

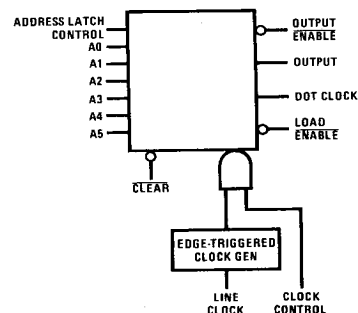
### Block Diagram



### Connection Diagram



### Logic Symbol



\* alpha pattern designators

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**Absolute Maximum Ratings** (Note 1)

|                                          |                 |
|------------------------------------------|-----------------|
| Supply Voltage                           | -0.5V to +7V    |
| Input Voltage                            | -1.5V to +5.5V  |
| Output Voltage                           | -0.5V to +5.5V  |
| Storage Temperature                      | -65°C to +150°C |
| Lead Temperature (Soldering, 10 seconds) | 300°C           |

**Operating Conditions**

|                               | MIN  | MAX  | UNITS |
|-------------------------------|------|------|-------|
| Supply Voltage ( $V_{CC}$ )   |      |      |       |
| DM76S64                       | 4.5  | 5.5  | V     |
| DM86S64                       | 4.75 | 5.25 | V     |
| Ambient Temperature ( $T_A$ ) |      |      |       |
| DM76S64                       | -55  | +125 | °C    |
| DM86S64                       | 0    | +70  | °C    |
| Logical "0" Voltage           | 0    | 0.8  | V     |
| Logical "1" Voltage           | 2.0  | 5.5  | V     |

**DC Electrical Characteristics** (Note 2)

| SYM      | PARAMETER                | CONDITIONS                                                               | MIN | TYP  | MAX  | UNITS   |
|----------|--------------------------|--------------------------------------------------------------------------|-----|------|------|---------|
| $I_{IL}$ | Input Load Current       | $V_{CC} = \text{Max}$ , $V_{IN} = 0.45V$                                 |     |      | -800 | $\mu A$ |
| $I_{IH}$ | Input Leakage Current    | $V_{CC} = \text{Max}$ , $V_{IN} = 2.4V$                                  |     |      | 40   | $\mu A$ |
| $I_I$    | Input Leakage Current    | $V_{CC} = \text{Max}$ , $V_{IN} = 5.5V$                                  |     |      | 1    | mA      |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC} = \text{Min}$ , $I_{OL} = 16 \text{ mA}$                         |     | 0.35 | 0.45 | V       |
| $V_{IL}$ | Low Level Input Voltage  | $V_{CC} = \text{Min}$                                                    |     |      | 0.80 | V       |
| $V_{IH}$ | High Level Input Voltage | $V_{CC} = \text{Min}$                                                    | 2.0 |      |      | V       |
| $V_C$    | Input Clamp Voltage      | $V_{CC} = \text{Min}$ , $I_{IN} = -12 \text{ mA}$                        |     | -0.8 | -1.5 | V       |
| $C_{IN}$ | Input Capacitance        | $V_{CC} = 5V$ , $V_{IN} = 2V$ , $T_A = 25^\circ C$ ,<br>1 MHz            |     | 4.0  |      | pF      |
| $C_O$    | Output Capacitance       | $V_{CC} = 5V$ , $V_O = 2V$ , $T_A = 25^\circ C$ ,<br>1 MHz, Output "OFF" |     | 6.0  |      | pF      |
| $I_{CC}$ | Power Supply Current     | $V_{CC} = \text{Max}$ , All Inputs Grounded,<br>Output Open              |     | 80   | 140  | mA      |

**TRI-STATE PARAMETERS**

|          |                              |                                                                          |     |     |          |         |
|----------|------------------------------|--------------------------------------------------------------------------|-----|-----|----------|---------|
| $I_{SC}$ | Output Short-Circuit Current | $V_O = 0V$ , $V_{CC} = \text{Max}$                                       | -15 |     | -70      | mA      |
| $I_{HZ}$ | Output Leakage               | $V_{CC} = \text{Max}$ , $V_O = 0.45 \text{ to } 2.4V$ ,<br>Chip Disabled |     |     | $\pm 40$ | $\mu A$ |
| $V_{OH}$ | Output Voltage High          | $I_{OH} = -2 \text{ mA}$                                                 | 2.4 | 3.2 |          | V       |

**AC Electrical Characteristics** (Note 2)

| SYM      | PARAMETER                  | CONDITIONS | DM76S64 |     |     | DM86S64 |     |     | UNITS |
|----------|----------------------------|------------|---------|-----|-----|---------|-----|-----|-------|
|          |                            |            | MIN     | TYP | MAX | MIN     | TYP | MAX |       |
| $T_{DO}$ | Access Time                |            |         |     |     |         |     |     | ns    |
| $T_{EA}$ | Dot Clock to Output        |            |         | 25  | 50  |         | 25  | 40  | ns    |
| $T_{ER}$ | Output Enable              |            |         | 10  | 35  |         | 10  | 30  | ns    |
|          | Output Disable             |            |         | 13  | 35  |         | 13  | 30  | ns    |
|          | Set-Up Time                |            |         |     |     |         |     |     | ns    |
| $TS1$    | Load to Dot Clock          |            | 25      | 7   |     | 20      | 7   |     | ns    |
| $TS2$    | Address to Load            | See        | 335     | 54  |     | 280     | 54  |     | ns    |
| $TS3$    | Clear to Load              | Switching  | 335     | 14  |     | 280     | 14  |     | ns    |
| $TS4$    | Control to Line Clock      | Time       | 50      | -10 |     | 40      | -10 |     | ns    |
| $TS5$    | Line Clock to Load         | Waveforms  | 1140    | 156 |     | 950     | 156 |     | ns    |
| $TS6$    | Address to Address Latch   |            | 50      | 6   |     | 40      | 6   |     | ns    |
|          | Hold Time                  |            |         |     |     |         |     |     | ns    |
| $TH1$    | Load from Dot Clock        |            | 5       | -6  |     | 0       | -6  |     | ns    |
| $TH2$    | Address from Load          |            | 0       | -14 |     | 0       | -14 |     | ns    |
| $TH3$    | Control from Line Clock    |            | 120     | 23  |     | 100     | 23  |     | ns    |
| $TH4$    | Address from Address Latch |            | 50      | 3   |     | 40      | 3   |     | ns    |

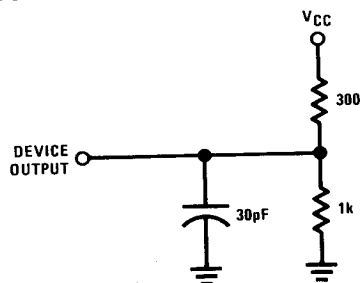
## AC Electrical Characteristics (Continued) (Note 2)

| SYM              | PARAMETER       | CONDITIONS | DM76S64 |     |     | DM86S64 |     |     | UNITS |
|------------------|-----------------|------------|---------|-----|-----|---------|-----|-----|-------|
|                  |                 |            | MIN     | TYP | MAX | MIN     | TYP | MAX |       |
|                  | Pulse Width     |            |         |     |     |         |     |     |       |
| TW1              | Line Clock      |            | 50      | 12  |     | 40      | 12  |     | ns    |
| TW2              | Clear           |            | 50      | 6   |     | 40      | 6   |     | ns    |
| TW3              | Dot Clock       |            | 25      | 12  |     | 20      | 12  |     | ns    |
| TW4              | Load            |            | 40      | 8   |     | 30      | 8   |     | ns    |
| TW5              | Address Latch   |            | 50      | 22  |     | 40      | 22  |     | ns    |
| f <sub>MAX</sub> | Clock Frequency |            | 18      | 35  |     | 22      | 35  |     | MHz   |

**Note 1:** Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

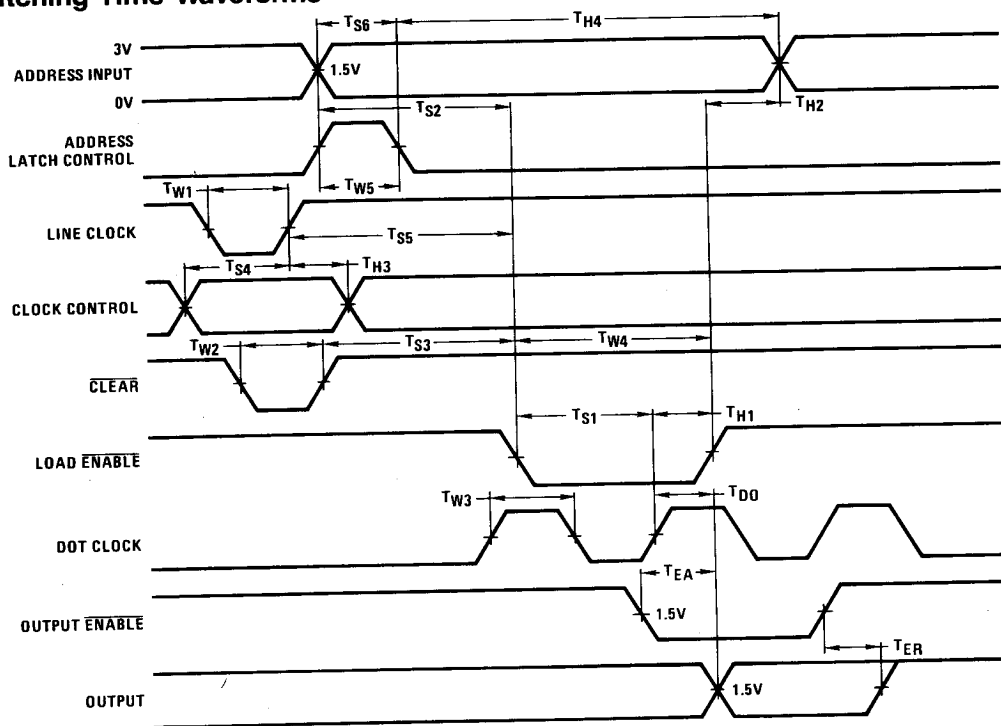
**Note 2:** These limits apply over the entire operating range unless stated otherwise. All typical values are for  $V_{CC} = 5V$  and  $T_A = 25^\circ C$ .

## Standard Test Load



- Input waveforms are supplied by a pulse generator having the following characteristics: PRR = 1 MHz,  $Z_{OUT} = 50 \Omega$ ,  $t_r < 5$  ns and  $t_f < 5$  ns (between 1.0V and 2.0V).
- $T_{DO}$  is measured with output enable at a steady low level.

## Switching Time Waveforms



## Truth Tables

### A) ADDRESS LATCH

| ADDRESS LATCH CONTROL | FUNCTION PERFORMED |
|-----------------------|--------------------|
| 0                     | Latched            |
| 1                     | Fall Through       |

### B) OUTPUT

| OUTPUT ENABLE | STATE OF THE OUTPUT |
|---------------|---------------------|
| 1             | Output Hi-Z         |
| 0             | Data Out            |

### C) 4-BIT LINE COUNTER

| CLOCK CONTROL | LINE CLOCK                                                                         | CLEAR | LINE COUNTER                        |
|---------------|------------------------------------------------------------------------------------|-------|-------------------------------------|
| H             |   | H     | Increment line counter              |
| X             | X                                                                                  | L     | Asynchronous clear resets counter   |
| L             | X                                                                                  | H     | Clock inhibited                     |
| H             |  | H     | No change on high-to-low clock edge |

X = Don't care

## Definitions

**A0–A5:** Character address. A 6-bit code which selects 1 of the 64 characters in the font.

**Clear:** Active low clear for mod 16 row counter, (can be used to truncate mod 16 counter).

**Line Clock:** Clock that advances the line counter. Advances counter on the low-to-high transition.

**Clock Control:** Enables line clock when high and disables line clock when low.

**Load Enable:** Active low load command which routes data from the character ROM to the "D" inputs of the 7-bit shift register.

**Dot Clock:** A low-to-high transition of the dot clock loads the shift register if load enable is low or shifts data if load enable is high.

**Output Enable:** An active low output enable. When high the output is in the Hi-Z state.

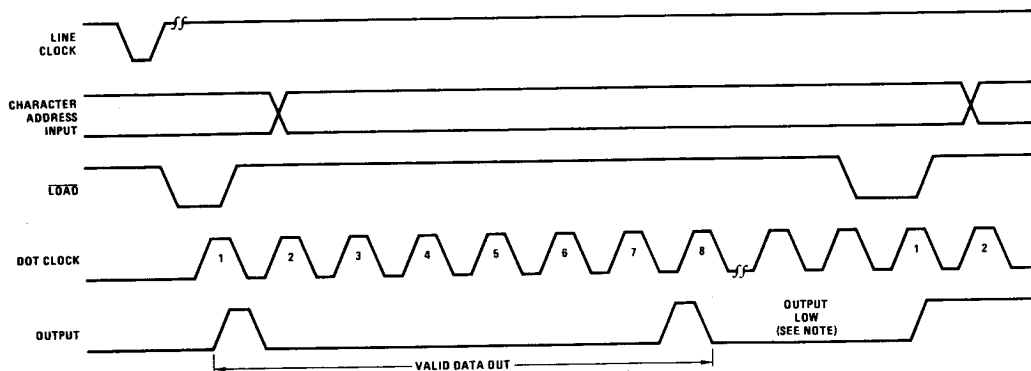
**Output:** A TTL TRI-STATE output buffer.

## Functional Description

To select a character, a 6-bit binary word must be present at the address inputs A0–A5 when the address latch control is high. This address can be latched by bringing the address latch control signal low after a 40 ns set-up time. When the clear input receives a low pulse, the counter is reset to zero. The shift register can be loaded ( $T_{S2}$  ns) after the character is addressed. Data, representing 1 horizontal line of the addressed character, is available at the output when the load enable input is brought low. As shown in Figure 1, valid data arrives serially at the output. Dot clock pulses beyond that required to shift out 1 line of the

character will add lows to the end of character. This provides a horizontal spacing between characters.

Figure 2 shows how the counter sequences through the rows of addressed lines with the application of clock pulses at the line clock input. Any additional line clocks beyond that required to display the character will put a vertical space between characters. This spacing can be truncated by bringing the clear input low. Detailed system application information is contained in application note AN-167 available from National.



Note. Output goes and stays low following the leading edge of the eighth Dot-Clock pulse until Load enable is enabled again and new parallel data is loaded into the shift register.

FIGURE 1. Character Cycle

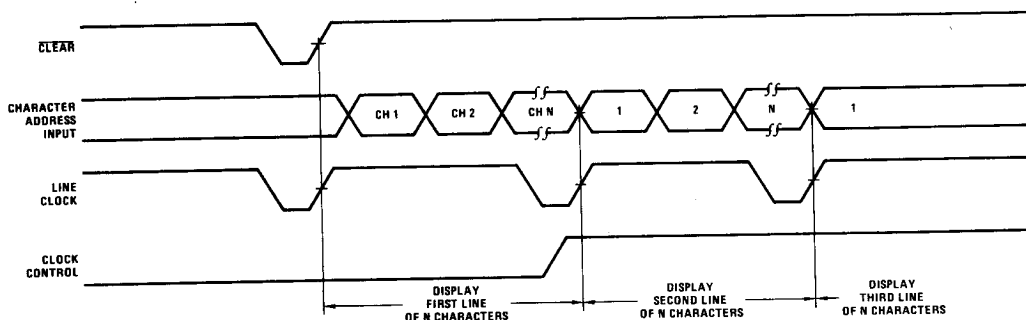


FIGURE 2. Line Cycle

## Functional Description (Continued)

A two character display example is shown in *Figure 3* and a typical system timing waveform is shown in *Figure 4*.

A chip select input is provided for expansion of the character font. The various standard fonts are shown in *Figures 5, 6, 7, 8, 9 and 10*. Descending characters in the 5 x 7 fonts are shifted by virtue of their placement in the matrix. Descending characters in the 7 x 9 fonts are shifted (by the on-chip line shifter/counter) the number of lines indicated by the number in the upper left hand corner of the character drawings in the figures.

**Character Cycle** — ROM data corresponding to 1 line of characters is loaded into the shift register TS2 after the ROM is addressed. When load enable goes low, ROM data is allowed to be present at the D input of

the shift register via the MUX. The first bit of the ROM data is transferred to the output at the next low-to-high transition of the dot clock. After load enable goes back high, the second to seventh clock pulses shift out the rest of the selected row of the addressed character. Additional clock pulses will shift out low data used for spacing.

**Line Cycle** — The line counter is a mod 16 counter. A low-to-high transition of the line clock advances the line counter to the next count. If, for any reason, the counts need to be truncated, a low signal at the  $\overline{\text{clear}}$  input resets the counter to zero. The clock control may be used as a line clock disable. A high signal at the line clock control terminal enables the counter and a low signal disables the line clock.

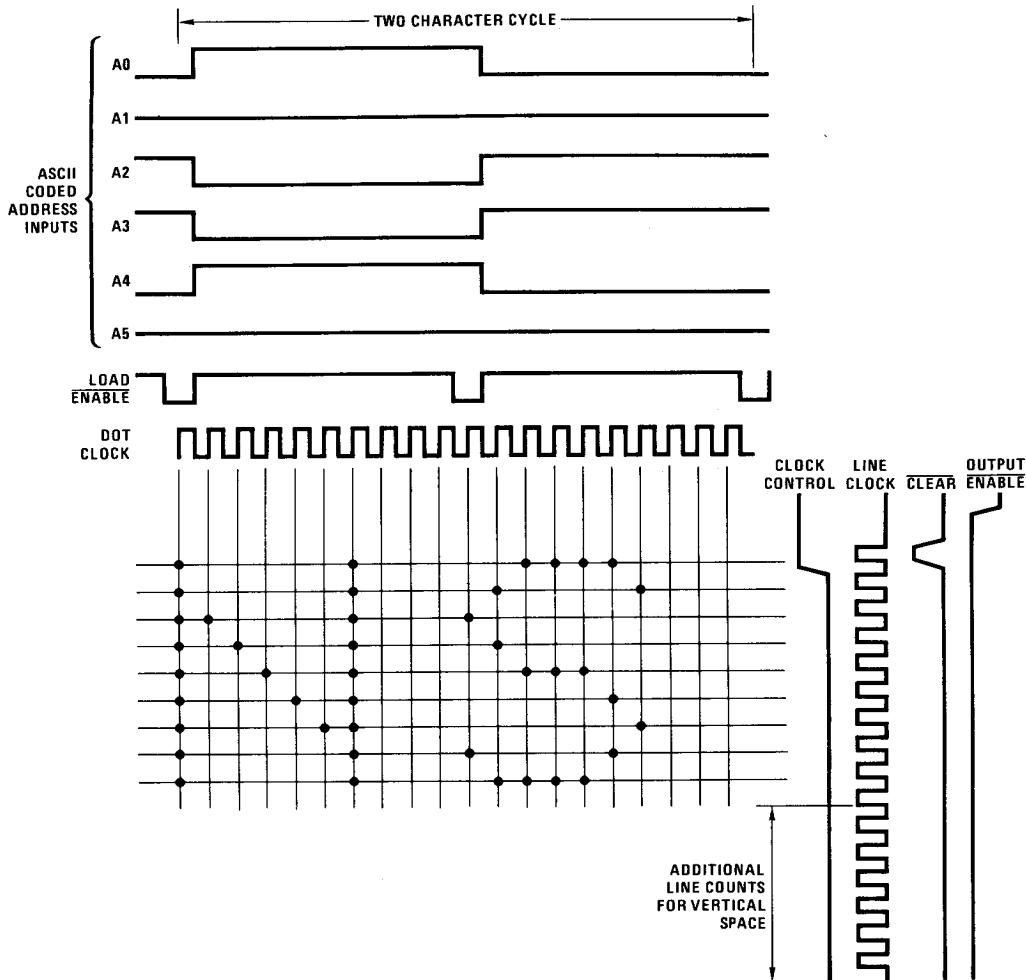
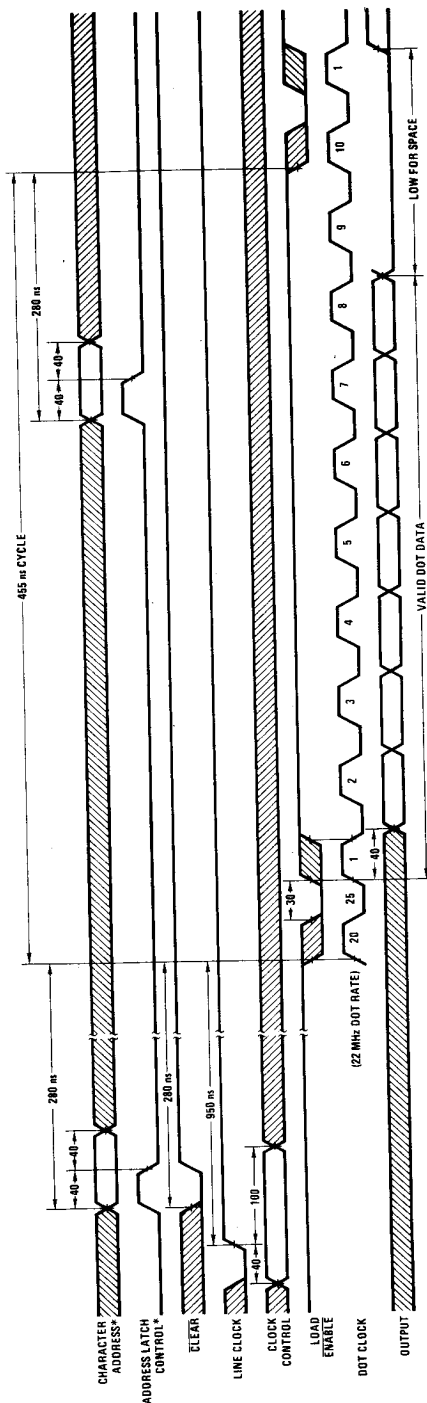


FIGURE 3. Example of Two Characters Display Timing

## Functional Description (Continued)



\*Shown here for operation with dynamic memory. For static memory operation the address latch control would be tied high and the character addresses would be stable between each address change occurring 280 ns before the high-to-low transition of Load enable.

FIGURE 4. Typical System Timing Waveform

# Functional Description (Continued)

| A0-A3<br>A4-A6 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
|----------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0              |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 1              |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 2              |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 3              |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

FIGURE 7. DM76S64CAB/DM86S64CAB

| A0-A3<br>A4-A6 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
|----------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0              |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 1              |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 2              |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 3              |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

FIGURE 8. DM76S64CAH/DM86S64CAH



# Functional Description (Continued)

DM76S64/DM86S64

| A0-A3<br>A4-A6 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
|----------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0              |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 1              |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 2              |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 3              |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

FIGURE 5. DM76S64BWF/DM86S64BWF

| A0-A3<br>A4-A6 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
|----------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0              |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 1              |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 2              |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 3              |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

FIGURE 6. DM76S64CAE/DM86S64CAE

| A0-A3<br>A4-A5 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
|----------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
|                |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 0              |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 1              |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 2              |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 3              |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

FIGURE 9. DM76S64CTA/DM86S64CTA

## Functional Description (Continued)

| A0-A3<br>A4-A5 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
|----------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
|                |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 0              |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 1              |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 2              |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 3              |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

FIGURE 10. DM76S64CTB/DM86S64CTB