CY2SSTU877

1.8V, 500-MHz, 10-Output JEDEC-Compliant Zero Delay Buffer

Features

- **Operating frequency: 125 MHz to 500 MHz**
- **Supports DDRII SDRAM**
- **Ten differential outputs from one differential input**
- **Spread-Spectrum-compatible**
- **Low jitter (cycle-to-cycle): < 40 ps**
- **Very low skew: < 40 ps**
- **Power management control input**
- **1.8V operation**
- **Fully JEDEC-jompliant**
- **52-ball BGA and a 40-pin MLF (QFN)**

Functional Description

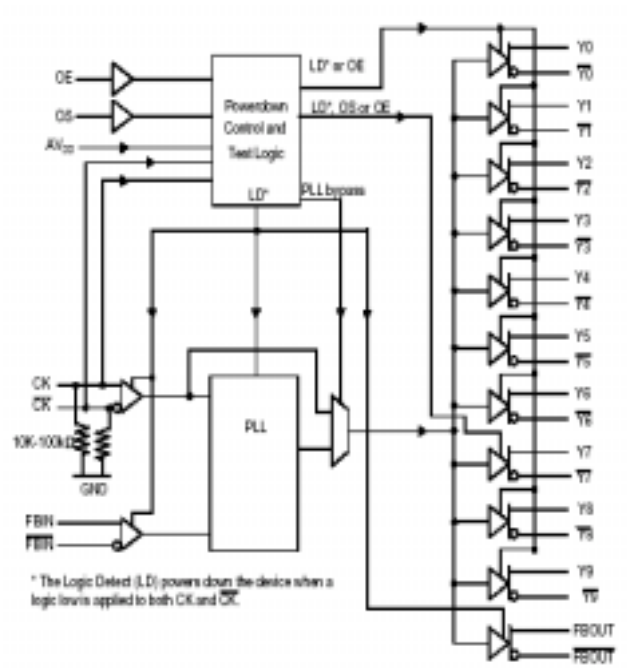
The CY2SSTU877 is a high-performance, low-skew, low-jitter zero delay buffer designed to distribute differential clocks in high-speed applications. The CY2SSTU877 generates ten differential pair clock outputs from one differential pair clock input. In addition, the CY2SSTU877 features differential feedback clock outputs and inputs. This allows the CY2SSTU877 to be used as a zero-delay buffer. When used as a zero-delay buffer in nested clock trees, the CY2SSTU877 locks onto the input reference and translates with near zero delay to low-skew outputs.

This phase-locked loop (PLL) clock buffer is designed for a VDD of 1.8V, an AVDD of 1.8 V and differential data input and output levels. Package options include a plastic 526-ball VFBGA and a 40-pin MLF(QFN). The device is a zero delay buffer that distributes a differential clock input pair (CK, CK#) to ten differential pair of clock outputs (Y[0:9], Y#[0:9]) and one differential pair feedback clock outputs (FBOUT, FBOUT#). The input clocks (CK, CK#), the feedback clocks (FBIN, FBIN#), the LVCMOS (OE, OS), and the analog power input (AVDD) control the clock outputs.

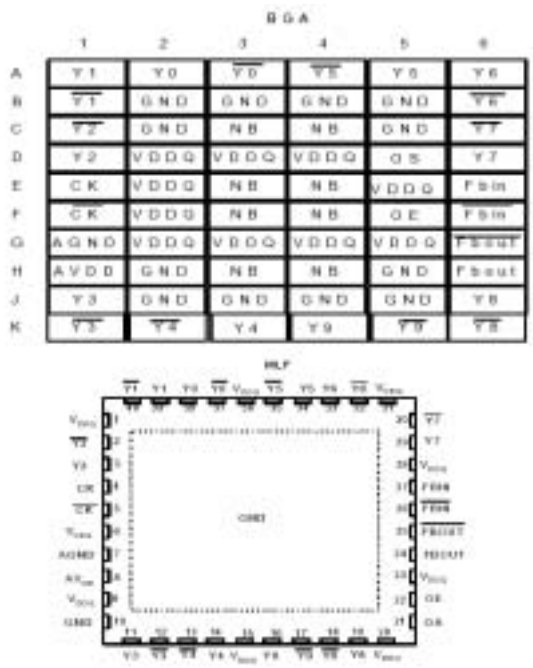
The PLL in the CY2SSTU877 clock driver uses the input clocks (CK, CK#) and the feedback clocks (FBIN, FBIN#) to provide high-performance, low-skew, low-jitter output differential clocks (Y[0:9], Y#[0:9]). The CY2SSTU877 is also able to track Spread Spectrum Clocking (SSC) for reduced EMI.

When AVDD is grounded, the PLL is turned off and bypassed for test purposes. When both clock signals (CK, CK#) are logic low, the device will enter a low power mode. An input logic detection circuit on the differential inputs, independent from the input buffers, will detect the logic low level and perform a low power state where all outputs, the feedback and the PLL are OFF. When the inputs transition from both being logic low to being differential signals, the PLL will be turned back on, the inputs and outputs will be enabled and the PLL will obtain phase lock between the feedback clock pair (FBIN, FBIN#) and the input clock pair (CK, CK#) within the specified stabilization time tL.

Block Diagram



Pin Configuration



All product and company names mentioned in this document are the trademarks of their respective holders.

Document History Page

Document Title:CY2SSTU877 1.8V, 500-MHz, 10-Output JEDEC-Compliant Zero Delay Buffer Document Number: 38-07575				
Rev.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	129198	08/22/03	RGL	New Data Sheet