

CD54/74HC02 CD54/74HCT02

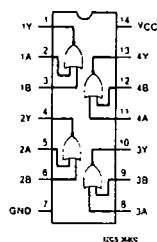
File Number 1647

T-43-21-00

High-Speed CMOS Logic

HARRIS SEMICONDUCTOR

27E D 4302271 0017459 7 HAS



FUNCTIONAL DIAGRAM and
TERMINAL ASSIGNMENT

Quad 2-Input NOR Gate

Type Features:

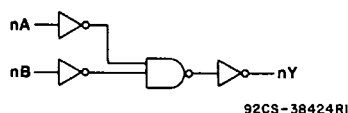
- Buffered Inputs
- Typical Propagation Delay = 7ns
@ $V_{CC} = 5V$, $C_L = 15pF$, $T_A = 25^\circ C$

The RCA-CD54/74HC02 and CD54/74HCT02 logic gates utilize silicon-gate CMOS technology to achieve operating speeds similar to LSTTL gates with the low power consumption of standard CMOS integrated circuits. All devices have the ability to drive 10 LSTTL loads. The CD54/74HCT logic family is functionally as well as pin compatible with the standard 54LS/74LS logic family.

The CD54HC02 and CD54HCT02 are supplied in 14-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC02 and CD74HCT02 are supplied in 14-lead dual-in-line plastic packages (E suffix) and in 14-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- Fanout (Over Temperature Range):
Standard Outputs - 10 LSTTL Loads
Bus Driver Outputs - 15 LSTTL Loads
- Wide Operating Temperature Range:
CD74HC/HCT: -40 to $+85^\circ C$
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- Alternate Source is Philips/Signetics
- CD54HC/CD74HC Types:
2 to 6 V Operation
High Noise Immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$
of V_{CC} , @ $V_{CC} = 5V$
- CD54HCT/CD74HCT Types:
4.5 to 5.5 V Operation
Direct LSTTL Input Logic Compatibility
 $V_{IL} = 0.8V$ Max., $V_{IH} = 2V$ Min.
CMOS Input Compatibility
 $I_i \leq 1 \mu A$ @ V_{OL} , V_{OH}



LOGIC DIAGRAM

TRUTH TABLE		
nA	nB	nY
L	L	H
L	H	L
H	L	L
H	H	L

CD54/74HC02

CD54/74HCT02

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE, (V_{CC})	
(Voltages referenced to ground)	-0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_i < -0.5$ V OR $V_i > V_{CC} + 0.5$ V)	± 20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC} + 0.5$ V)	± 20 mA
DC DRAIN CURRENT, PER OUTPUT (I_o) (FOR -0.5 V $< V_o < V_{CC} + 0.5$ V)	± 25 mA
DC V_{CC} OR GROUND CURRENT (I_{CC})	± 50 mA
POWER DISSIPATION PER PACKAGE (P_D)	
For $T_A = -40$ to $+60^\circ$ C (PACKAGE TYPE E)	500 mW
For $T_A = +60$ to $+85^\circ$ C (PACKAGE TYPE E)	Derate Linearly at 8 mW/ $^\circ$ C to 300 mW
For $T_A = -55$ to $+100^\circ$ C (PACKAGE TYPE F, H)	500 mW
For $T_A = +100$ to $+125^\circ$ C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/ $^\circ$ C to 300 mW
For $T_A = -40$ to $+70^\circ$ C (PACKAGE TYPE M)	400 mW
For $T_A = +70$ to $+125^\circ$ C (PACKAGE TYPE M)	Derate Linearly at 6 mW/ $^\circ$ C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE F, H	-55 to $+125^\circ$ C
PACKAGE TYPE E, M	-40 to $+85^\circ$ C
STORAGE TEMPERATURE (T_{stg})	-65 to $+150^\circ$ C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance $1/16 \pm 1/32$ in. (1.59 ± 0.79 mm) from case for 10 s max.	$+265^\circ$ C
Unit inserted into a PC Board (min. thickness $1/16$ in., 1.59 mm)	
with solder contacting lead tips only	$+300^\circ$ C

RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range) V_{CC} .*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_i , V_o	0	V_{CC}	V
Operating Temperature T_A :			
CD74 Types	-40	$+85$	$^\circ$ C
CD54 Types	-55	$+125$	$^\circ$ C
Input Rise and Fall Times t_r , t_f			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

*Unless otherwise specified, all voltages are referenced to Ground.

CD54/74HC02 CD54/74HCT02

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC02/CD54HC02											CD74HCT02/CD54HCT02											UNITS
	TEST CONDITIONS			74HC/54HC SERIES			74HC SERIES		54HC SERIES		TEST CONDITIONS		74HCT/54HCT SERIES			74HCT SERIES		54HCT SERIES					
	V _i V	I _o mA	V _{cc} V	+25°C			-40/ +85°C		-55/ +125°C		V _i V	V _{cc} V	+25°C			-40/ +85°C		-55/ +125°C					
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max				
High-Level Input Voltage V _{ih}			2	1.5	—	—	1.5	—	1.5	—	—	4.5	2	—	—	2	—	2	—	V			
			4.5	3.15	—	—	3.15	—	3.15	—		5.5											
			6	4.2	—	—	4.2	—	4.2	—													
Low-Level Input Voltage V _{il}			2	—	—	0.5	—	0.5	—	0.5	—	4.5			0.8	—	0.8	—	0.8	V			
			4.5	—	—	1.35	—	1.35	—	1.35	—	5.5											
			6	—	—	1.8	—	1.8	—	1.8	—												
High-Level Output Voltage V _{oh}	V _{ih} or CMOS Loads	-0.02	2	1.9	—	—	1.9	—	1.9	—	V _{ih} or V _{ih}	4.5	4.4	—	—	4.4	—	4.4	—	V			
			4.5	4.4	—	—	4.4	—	4.4	—		5.5											
			6	5.9	—	—	5.9	—	5.9	—													
TTL Loads	V _{ih} or V _{oh}	-4 -5.2	4.5	3.98	—	—	3.84	—	3.7	—	V _{ih} or V _{oh}	4.5	3.98	—	—	3.84	—	3.7	—	V			
Low-Level Output Voltage V _{ol}	V _{il} or CMOS Loads	0.02	2	—	—	0.1	—	0.1	—	0.1	V _{il} or V _{ol}	4.5	—	—	0.1	—	0.1	—	0.1	V			
			4.5	—	—	0.1	—	0.1	—	0.1		5.5											
			6	—	—	0.1	—	0.1	—	0.1													
TTL Loads	V _{il} or V _{oh}	4 5.2	4.5	—	—	0.26	—	0.33	—	0.4	V _{il} or V _{ih}	4.5	—	—	0.26	—	0.33	—	0.4	V			
Input Leakage Current I _i	V _{cc} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V _{cc} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA			
Quiescent Device Current I _{cc}	V _{cc} or Gnd	0	6	—	—	2	—	20	—	40	V _{cc} or Gnd	5.5	—	—	2	—	20	—	40	μA			
Additional Quiescent Device Current per input pin. 1 unit load ΔI _{cc}											V _{cc} -2.1 5.5	4.5 to 5.5	— 100	360	— 450	— 490			μA				

*For dual-supply systems theoretical worst case ($V_i = 2.4$ V, $V_{cc} = 5.5$ V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
All	1.5

*Unit Load is ΔI_{cc} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.

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CD54/74HC02

CD54/74HCT02

SWITCHING CHARACTERISTICS ($V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, Input t_r , $t_f = 6\text{ ns}$)

CHARACTERISTIC	C_L (pF)	SYMBOL	TYPICAL		UNITS
			HC	HCT	
Propagation Delay, Data Input to Output Y (Fig. 1)	15	t_{PLH} t_{PHL}	7	8	ns
Power Dissipation Capacitance*	—	C_{PD}	26	26	pF

* C_{PD} is used to determine the dynamic power consumption, per gate.

$PD = V_{CC}^2 f_i (C_{PD} + C_L)$

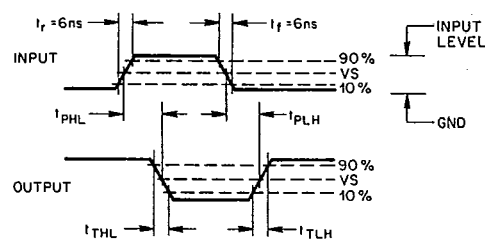
f_i = input frequency

C_L = output load capacitance

V_{CC} = supply voltage

SWITCHING CHARACTERISTICS ($C_L = 50\text{ pF}$, Input t_r , $t_f = 6\text{ ns}$)

CHARACTERISTIC	SYMBOL	V _{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay, Input to Output (Fig. 1)	t _{PLH}	2		90		—		115		—		135		—	ns
	t _{PHL}	4.5		18		21		23		26		27		32	
		6		15		—		20		—		23		—	
Transition Times (Fig. 1)	t _{TLH}	2		75		—		95		—		110		—	ns
	t _{THL}	4.5		15		15		19		19		22		22	
		6		13		—		16		—		19		—	
Input Capacitance	C _I	—		10		10		10		10		10		10	pF



92CS-3799IR1

	54/74HC	54/74HCT
Input Level	V_{CC}	3V
Switching Voltage, V_S	50% V_{CC}	1.3 V

Fig. 1 - Transition times and propagation delay times.