High Reliability Serial EEPROMs

WL-CSP EEPROM family
SPI BUS

BU9832GUL-W

No.10001EAT16

●Description

BU9832GUL-W is a serial EEPROM of SPI BUS interface method.

●Features

1) High speed clock action up to 5MHz (Max.)
2) Wait function by $\overline{\text{HOLD}}$ terminal.
3) Part or whole of memory arrays settable as read only memory area by program.
4) 1.8 ~ 5.5V single power source action most suitable for battery use.
5) Page write mode useful for initial value write at factory shipment.
6) For SPI bus interface (CPOL, CPHA) = (0, 0), (1, 1)
7) Auto erase and auto end function at data rewrite.
8) Low current consumption
   At write action (5V) : 1.5mA (Typ.)
   At read action (5V) : 1.0mA (Typ.)
   At standby action (5V) : 0.1μA (Typ.)
9) Address auto increment function at read action
10) Write mistake prevention function
   Write prohibition at power on.
   Write prohibition by command code (WRDI).
   Write prohibition by $\overline{\text{WP}}$ pin.
   Write prohibition block setting by status registers (BP1, BP0)
   Write mistake prevention function at low voltage.
11) Data at shipment Memory array: FFh, status register WPEN, BP1, BP0 : 0
12) Data kept for 40 years.
13) Data rewrite up to 1,000,000times.

●Page write

Product number	Number of pages
BU9832GUL-W	32 Byte

●BU9832GUL-W

Type	Capacity	Bit format	Power source voltage	Package
BU9832GUL-W	8Kbit	1K×8	1.8~5.5V	VCSP50L2

●Absolute maximum ratings (Ta=25℃)

Parameter	Symbol	Ratings	Unit
Impressed voltage	Vcc	-0.3~+6.5	V
Permissible dissipation	Pd	220(VCSP50L2) *1	mW
Storage Temperature range	Tstg	-65~+125	℃
Operating Temperature range	Topr	-40~+85	℃
Terminal voltage	—	-0.3~Vcc+0.3	V

*1 When using at Ta=25℃ or higher, 220mW to be reduced per 1℃

● **Recommended action conditions**

Parameter	Symbol	Ratings	Unit
Power source voltage	Vcc	1.8~5.5	V
Input voltage	Vin	0~Vcc	

● **Memory cell characteristics** (Ta=25℃, Vcc=1.8~5.5V)

Parameter	Limits			Unit
	Min.	Typ.	Max	
Number of data rewrite times *1	1,000,000	–	–	Times
Data hold years *1	40	–	–	Years

*1 : Not 100% TESTED

● **Input / output capacity** (Ta=25℃, frequency=5MHz)

Parameter	Symbol	Limits		Unit	Conditions
		Min.	Max		
Input capacity *1	C_{IN}	–	8	pF	V_{IN}=GND
Output capacity *1	C_{OUT}	–	8	pF	V_{OUT}=GND

*1 : Not 100% TESTED

●**Electrical characteristics** (Unless otherwise specified, Ta=-40~+85℃, Vcc=1.8~5.5V)

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
“H” input voltage 1	VIH1	0.7xVcc	–	Vcc+0.3	V	1.8≦Vcc≦5.5V
“L” input voltage 1	VIL1	-0.3	–	0.3xVcc	V	1.8≦Vcc≦5.5V
“L” output voltage 1	VOL1	0	–	0.4	V	IOL=2.1mA(Vcc=2.5V~5.5V)
“L” output voltage 2	VOL2	0	–	0.2	V	IOL=150μA(Vcc=1.8V~2.5V)
“H” output voltage 1	VOH1	Vcc-0.5	–	Vcc	V	IOH=-0.4mA(Vcc=2.5V~5.5V)
“H” output voltage 2	VOH2	Vcc-0.2	–	Vcc	V	IOH=-100μA(Vcc=1.8V~2.5V)
Input leak current	ILI	-1	–	1	μA	VIN=0~Vcc
Output leak current	ILO	-1	–	1	μA	VOUT=0~Vcc, $\overline{CS}$ =Vcc
Current consumption at write action	ICC1	–	–	1.0	mA	Vcc=1.8V,fSCK=2MHz, tE/W=5ms Byte write, Page write, Write status register
	ICC2	–	–	2.0	mA	Vcc=2.5V,fSCK=5MHz, tE/W=5ms Byte write, Page write, Write status register
	ICC3	–	–	3.0	mA	Vcc=5.5V,fSCK=5MHz, tE/W=5ms Byte write, Page write, Write status register
Current consumption at read action	ICC4	–	–	1.5	mA	Vcc=2.5V,fSCK=5MHz Read, Read status register
	ICC5	–	–	2.0	mA	Vcc=5.5V,fSCK=5MHzN Read, Read status register
Standby current	ISB	–	–	2	μA	Vcc=5.5V SCK=SI=Vcc or=GND,SO=OPEN

○This product is not designed for protection against radioactive rays.

●Operating timing characteristics

(Ta=-40~+85℃, unless otherwise specified, load capacity C_{L1}=100pF)

Parameter	Symbol	1.8≤Vcc<2.5V			2.5≤Vcc<5.5V			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
SCK frequency	fSCK	–	–	2	–	–	5	MHz
SCK high time	tSCKWH	200	–	–	85	–	–	ns
SCK low time	tSCKWL	200	–	–	85	–	–	ns
$\overline{CS}$ high time	tCS	200	–	–	85	–	–	ns
$\overline{CS}$ setup time	tCSS	200	–	–	90	–	–	ns
$\overline{CS}$ hold time	tCSH	200	–	–	85	–	–	ns
SCK setup time	tSCKS	200	–	–	90	–	–	ns
SCK hold time	tSCKH	200	–	–	90	–	–	ns
SI setup time	tDIS	40	–	–	20	–	–	ns
SI hold time	tDIH	50	–	–	40	–	–	ns
Data output delay time1	tPD1	–	–	150	–	–	70	ns
Data output delay time2 (C_{L2}=30pF)	tPD2	–	–	145	–	–	55	ns
Output hold time	tOH	0	–	–	0	–	–	ns
Output disable time	tOZ	–	–	250	–	–	100	ns
$\overline{HOLD}$ setting setup time	tHFS	120	–	–	60	–	–	ns
$\overline{HOLD}$ setting hold time	tHFH	90	–	–	40	–	–	ns
$\overline{HOLD}$ release setup time	tHRS	120	–	–	60	–	–	ns
$\overline{HOLD}$ release hold time	tHRH	140	–	–	70	–	–	ns
Time from $\overline{HOLD}$ to output High-Z	tHOZ	–	–	250	–	–	100	ns
Time from $\overline{HOLD}$ To output change	tHPD	–	–	150	–	–	70	ns
SCK rise time *1	tRC	–	–	1	–	–	1	μs
SCK fall time *1	tFC	–	–	1	–	–	1	μs
Output rise time *1	tRO	–	–	100	–	–	50	ns
Output fall time *1	tFO	–	–	100	–	–	50	ns
Write time	tE/W	–	–	5	–	–	5	ms

*1 NOT 100% TESTED

●AC measurement conditions

Parameter	Symbol	Limits			Unit
		Min.	Typ.	Max.	
Load capacity 1	C_{L1}	–	–	100	pF
Load capacity 2	C_{L2}	–	–	30	pF
Input rise time	–	–	–	50	ns
Input fall time	–	–	–	50	ns
Input voltage	–	0.2Vcc/0.8Vcc			V
Input / Output judgment voltage	–	0.3Vcc/0.7Vcc			V

●Sync data input / output timing

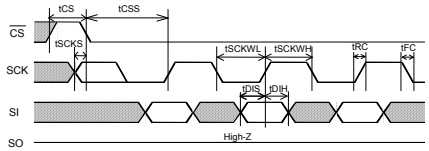


Fig.1 Input timing

SI is taken into IC inside in sync with data rise edge of SCK.
IInput address and data from the most significant bit MSB.

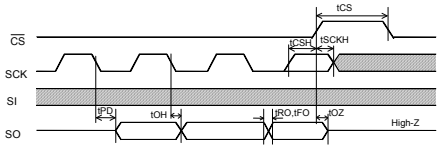


Fig.2 Input / Output timing

SO is output in sync with data fall edge of SCK. Data is output from the most significant bit MSB.

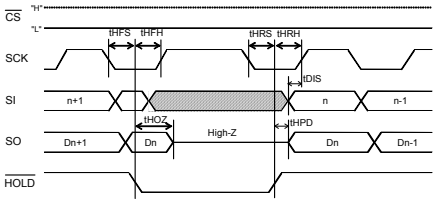


Fig.3 HOLD timing

●Block diagram

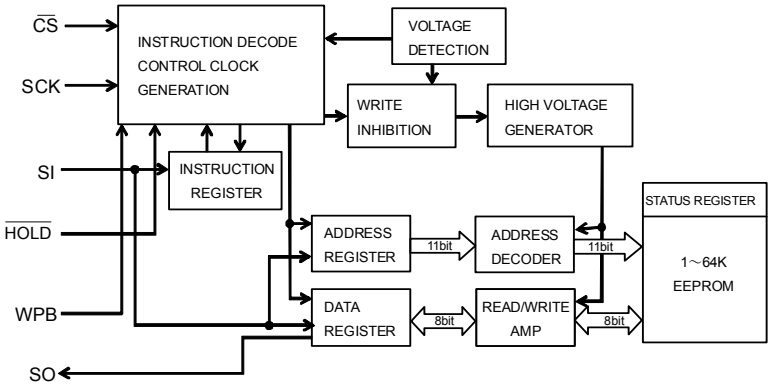


Fig.4 Block diagram

●Pin assignment and description

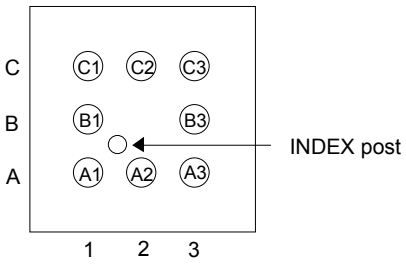


Fig.5 Pin assignment diagram

Land No.	Terminal name	Input/ Output	Function
A1	WPB	Input	Write protect input Write status register command is prohibited.
A2	GND	–	All input / output reference voltage, 0V
A3	SI	Input	Start bit, ope code, address, and serial data input
B1	SO	Output	Serial data output
B3	SCK	Input	Serial clock input
C1	$\overline{CS}$	Input	Chip select input
C2	Vcc	–	Power source to be connected
C3	$\overline{HOLD}$	Input	Hold input Command communication may be suspended temporarily (HOLD status)

●Characteristic data (The following characteristic data are Typ. Values.)

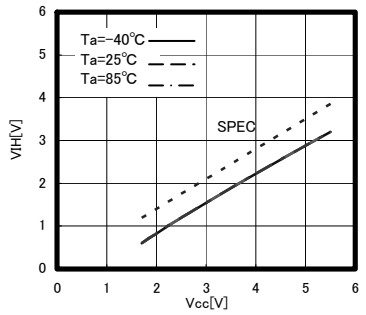


Fig.6 "H" input voltege VIH($\overline{CS}$,SCK,SI,$\overline{HOLD}$,$\overline{WP}$)

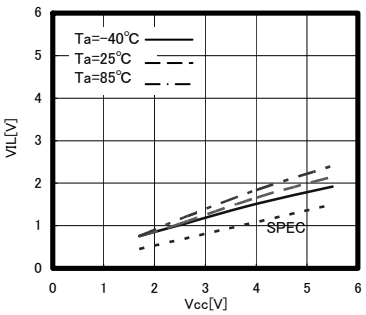


Fig.7 "L" input voltage VIL($\overline{CS}$,SCK,SI,$\overline{HOLD}$,$\overline{WP}$)

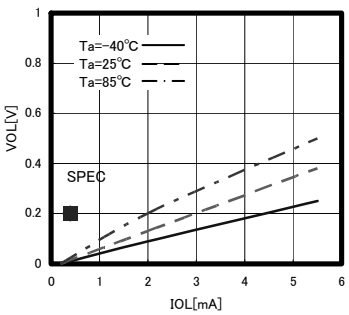


Fig.8 "L" output voltage VOL-IOL (Vcc=1.8V)

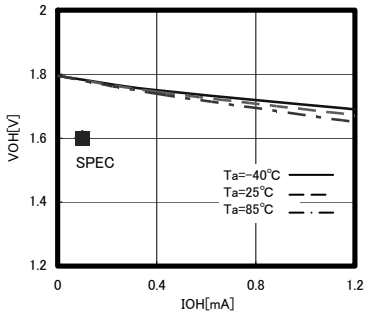


Fig.9 "H" output voltage VOH-IOH (Vcc=1.8V)

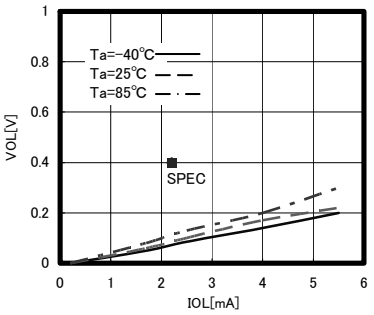


Fig.10 "L" output voltage VOL-IOL (Vcc=2.5V)

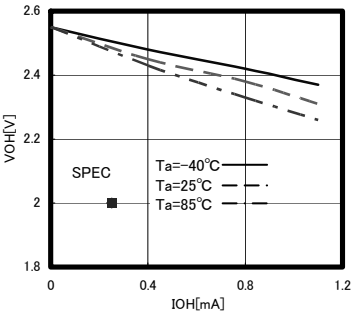


Fig.11 "H" output voltage VOH-IOH (Vcc=2.5V)

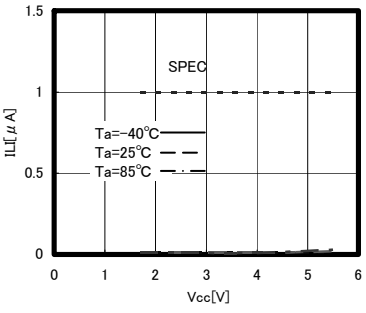


Fig.12 Input leak current ILI($\overline{CS}$,SCK,SI,$\overline{HOLD}$,$\overline{WP}$)

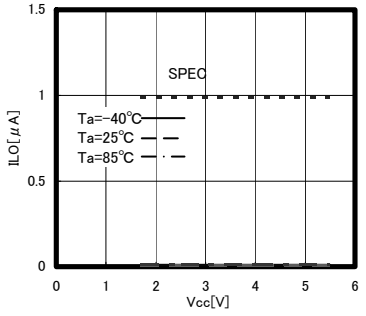


Fig.13 Output leak current ILO(SO)

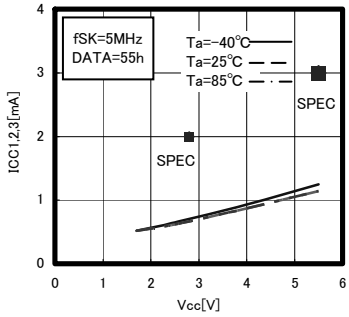


Fig.14 Current consumption at WRITE operation ICC1,2,3 (WRITE,PAGE WRITE,WRSR,fSCK=5MHz)

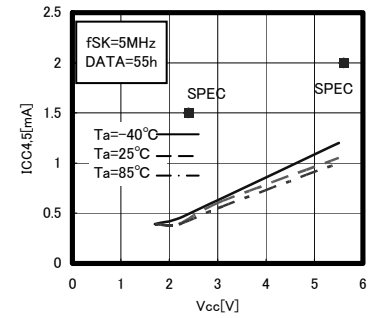


Fig.15 Consumption current at READ operation ICC4,5(READ,WRSR,fSK=5MHz)

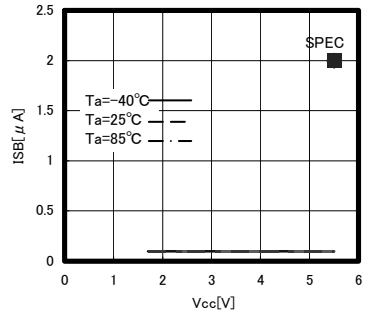


Fig.16 Consumption current at standby operation ISB

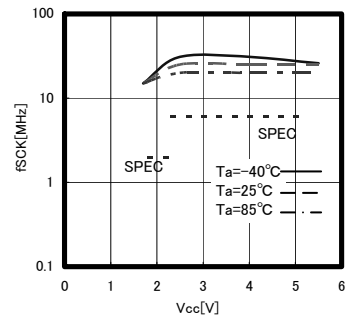


Fig.17 SCK frequency fSCK

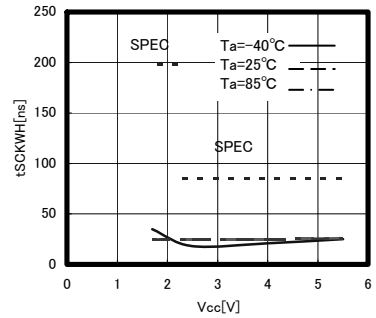


Fig.18 tSCK high time tSCKWH

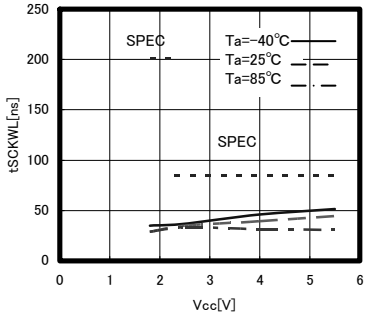


Fig.19 tSCK low time tSCKWL

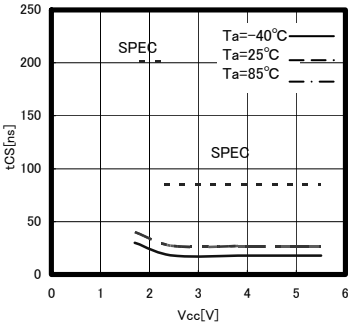


Fig.20 $\overline{CS}$ high time tCS

●Characteristic data (The following characteristic data are Typ. Values.)

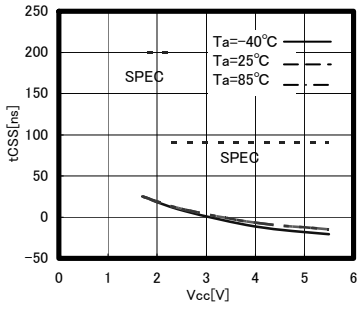


Fig.21 $\overline{CS}$ setup time tCSS

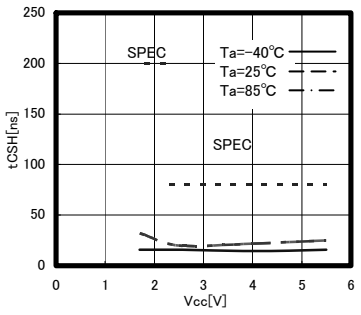


Fig.22 $\overline{CS}$ hold time tCSH

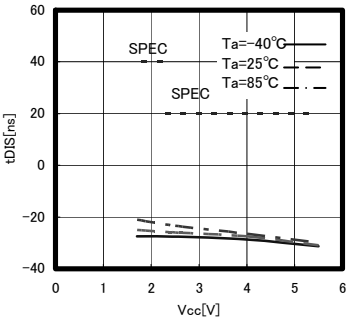


Fig.23 SI setup time tDIS

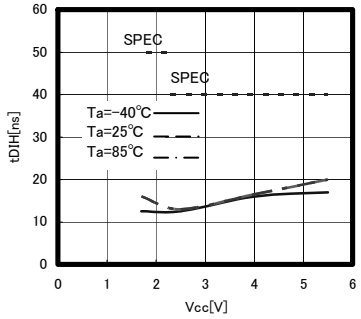


Fig.24 SI hold time tDIH

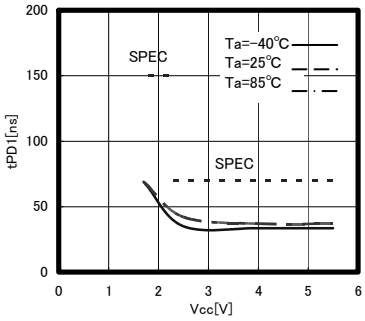


Fig.25 Data output delay time tPD1(CL=100pF)

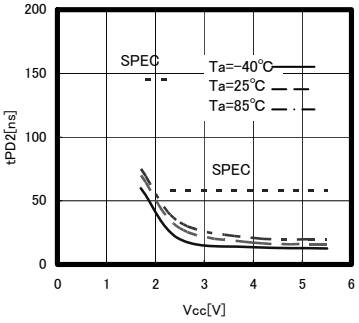


Fig.26 Data output delay time tPD2(CL=30pF)

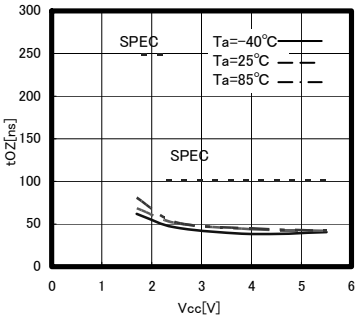


Fig.27 Output disable time tOZ

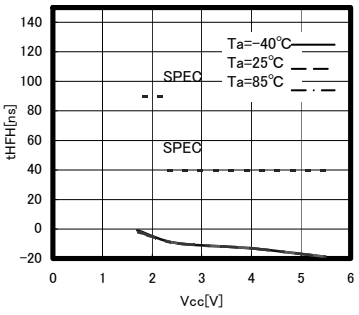


Fig.28 $\overline{HOLD}$ setting hold time tHFH

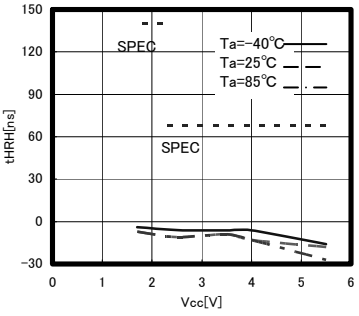


Fig.29 $\overline{HOLD}$ release hold time tHRH

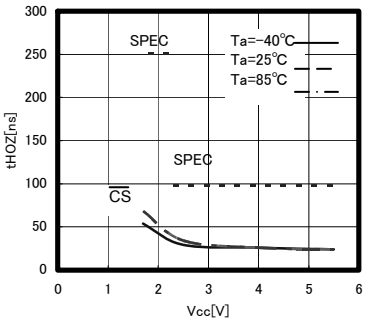


Fig.30 Time From $\overline{HOLD}$ to output High-Z tHOZ

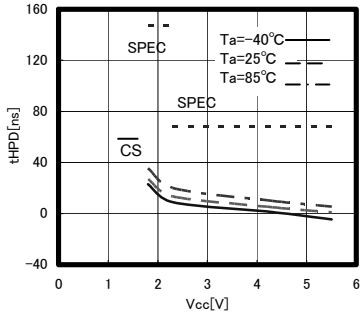


Fig.31 Time from $\overline{HOLD}$ to output change tHPD

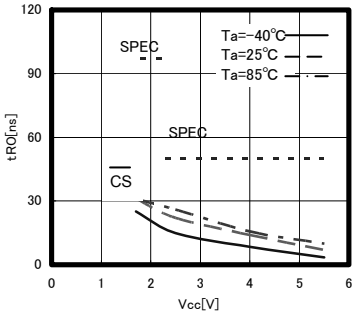


Fig.32 Output rise time tRO

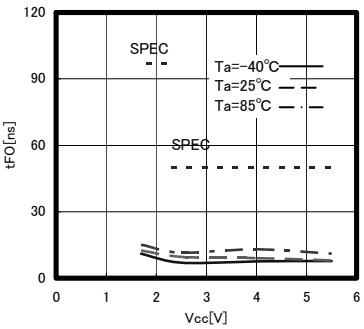


Fig.33 Output fall time tFO

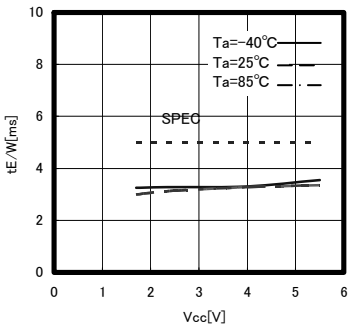


Fig.34 Write cycle time tE/W

●Features

○Status registers

This IC has status registers. The status registers are of 8 bits and express the following parameters.
BP0 and BP1 can be set by write status register command. These 2 bits are memorized into the EEPROM, therefore are valid even when power source is turned off.
Rewrite characteristics and data hold time are same as characteristics of the EEPROM.
WEN can be set by write enable command and write disable command. WEN becomes write disable status when power source is turned off. $\overline{R}$/B is for write confirmation, therefore cannot be set externally.
The value of status register can be read by read status command.

●Status registers

Product number	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
BU9832GUL-W	WPEN	0	0	0	BP1	BP0	WEN	$\overline{R}$/B

bit	Memory location	Function	Contents
WPEN	EEPROM	$\overline{WP}$ pin enable / disable designation bit WPEN=0=invalid WPEN=1=valid	This enables / disables the functions of $\overline{WP}$ pin.
BP1 BP0	EEPROM	EEPROM write disable block designation bit	This designates the write disable area of EEPROM. Write designation areas of product numbers are shown below.
WEN	Register	Write and write status register write enable / disable status confirmation bit WEN=0=prohibited WEN=1=permitted	
$\overline{R}$/B	Register	Write cycle status (READY / BUSY) status confirmation bit $\overline{R}$/B =0=READY $\overline{R}$/B =1=BUSY	

●Write disable block setting

BP1	BP0	Write disable block
0	0	None
0	1	300h-3FFh
1	0	200h-3FFh
1	1	000h-3FFh

○ $\overline{WP}$ pin

By setting $\overline{WP}$ =LOW, write command is prohibited. As for BU9832GUL-W when WPEN bit is set “1”, the $\overline{WP}$ pin functions become valid. And the write command to be disabled at this moment is WRSR.
However, when write cycle is in execution, no interruption can be made.

Product number	WRSR	WRITE
BU9832GUL-W	Prohibition possible but WPEN bit “1”	Prohibition impossible

○ $\overline{HOLD}$ pin

By $\overline{HOLD}$ pin, data transfer can be interrupted. When SCK=”1”, by making $\overline{HOLD}$ from “1” into”0”, data transfer to EEPROM is interrupted. When SCK = “0”, by making $\overline{HOLD}$ from “0” into “1”, data transfer is restarted.

●Command mode

Command		Contents	Ope code	
WREN	Write enable	Write enable command	0000	0110
WRDI	Write disable	Write disable command	0000	0100
READ	Read	Read command	0000	0011
WRITE	Write	Write command	0000	0010
RDSR	Read status register	Status register read command	0000	0101
WRSR	Write status register	Status register write command	0000	0001

●Timing chart

1. Write enable (WREN) / disable (WRDI) cycle

・WREN (WRITE ENABLE): Write enable

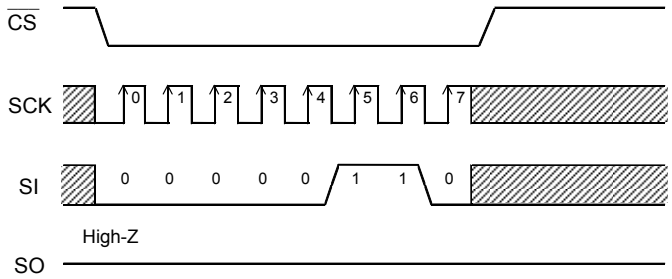


Fig.35 Write enable command

・WRDI (WRITE DISABLE): Write disable

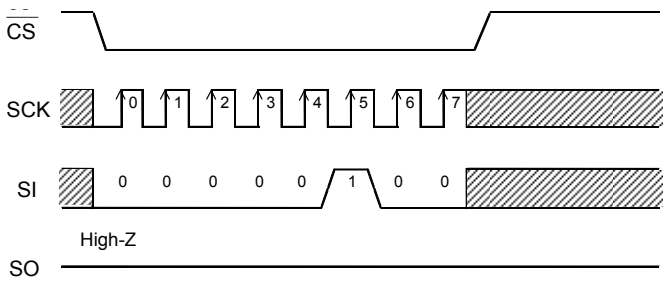


Fig.36 Write disable

○This IC has write enable status and write disable status. It is set to write enable status by write enable command, and it is set to write disable status by write disable command. As for these commands, set $\overline{CS}$ LOW, and then input the respective ope codes. The respective commands accept command at the 7-th clock rise. Even with input over 7 clocks, command becomes valid.

When to carry out write and write status register command, it is necessary to set write enable status by the write enable command. If write or write status register command is input in the write disable status, commands are cancelled. And even in the write enable status, once write and write status register command is executed once, it gets in the write disable status. After power on, this IC is in write disable status.

2. Read command (READ)

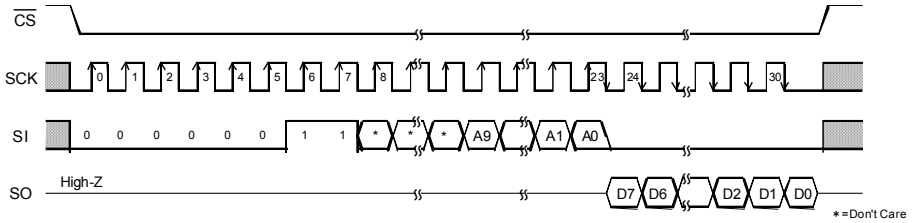


Fig.37 Read command

By read command, data of EEPROM can be read. As for this command, set $\overline{CS}$ LOW, then input address after read ope code. EEPROM starts data output of the designated address. Data output is started from SCK fall of 15 clock, and from D7 to D0 sequentially. This IC has increment read function. After output of data for 1 byte (8bits), by continuing input of SCK, data of the next address can be read. Increment read can read all the addresses of EEPROM. After reading data of the most significant address, by continuing increment read, data of the most insignificant address is read.

3. Write command (WRITE)

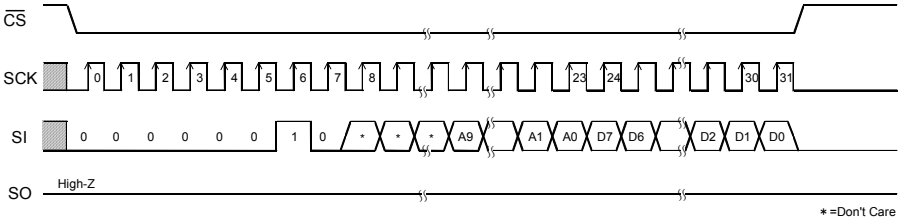


Fig.38 Write command

By write command, data of EEPROM can be written. As for this command, set $\overline{CS}$ LOW, then input address and data after write ope code. Then, by making $\overline{CS}$ HIGH, the EEPROM starts writing. The write time of EEPROM requires time of tE/W (Max 5ms). During tE/W, other than status read command is not accepted. Start $\overline{CS}$ after taking the last data (D0), and before the next SCK clock starts. At other timing, write command is not executed, and this write command is cancelled. This IC has page write function, and after input of data for 1 byte (8 bits), by continuing data input without starting $\overline{CS}$, data up to 16 bytes can be written for one tE/W. In page write, the insignificant 4 bit of the designated address is incremented internally at every time when data of 1 byte is input and data is written to respective addresses. When data of the maximum bytes or higher is input, address rolls over, and previously input data is overwritten.

4. Status register write / read command

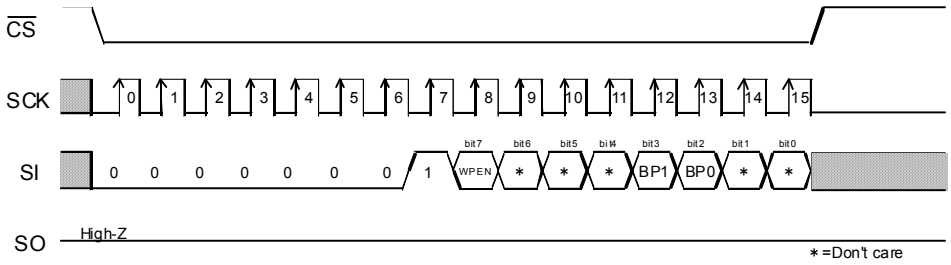


Fig.39 Status register write command

Write status register command can write status register data. The data can be written by this command are 2 bits*1, that is, BP1 (bit3) and BP0 (bit2) among 8 bits of status register. By BP1 and BP0, write disable block of EEPROM can be set. As for this command, set $\overline{CS}$ LOW, and input ope code of write status register, and input data. Then, by making $\overline{CS}$ HIGH, EEPROM starts writing. Write time requires time of tE/W as same as write. As for $\overline{CS}$ rise, start $\overline{CS}$ after taking the last data bit (bit0), and before the next SCK clock starts. At other timing, command is cancelled. Write disable block is determined by BP1 and BP0, and the block can be selected from 1/4 of memory array, 1/2, and entire memory array. (Refer to the write disable block setting table.) To the write disabled block, write cannot be made, and only read can be made.

*1 3bits including 1WPEN (bit7)

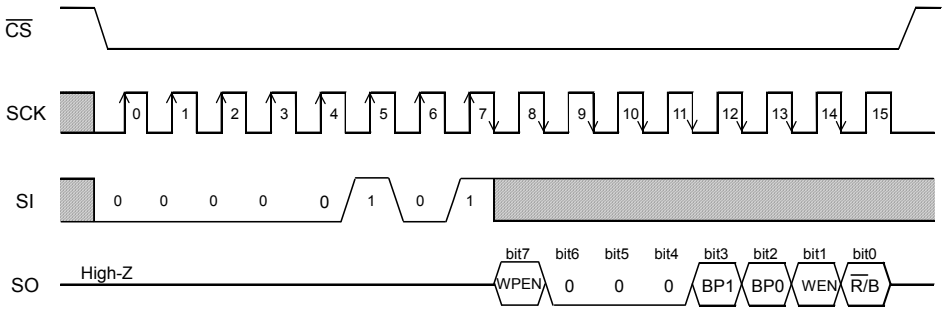


Fig.40 Status register read command

●At standby

○Current at standby

Set $\overline{CS}$ "H", and be sure to set SCK, SI, $\overline{WP}$, $\overline{HOLD}$ input "L" or "H". Do not input intermediate electric potantial.

○Timing

As shown in Fig.41, at standby, when SCK is "H", even if $\overline{CS}$ is fallen, SI status is not read at fall edge. SI status is read at SCK rise edge after fall of $\overline{CS}$. At standby and at power ON/OFF, set $\overline{CS}$ "H" status.

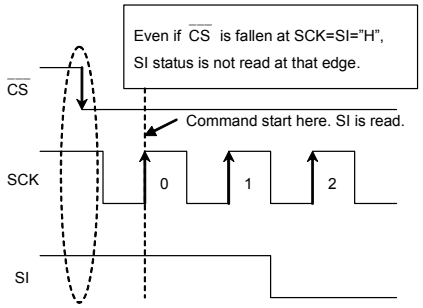


Fig.41 Operating timing

● $\overline{WP}$ cancel valid area

$\overline{WP}$ is normally fixed to "H" or "L" for use, but when $\overline{WP}$ is controlled so as to cancel write status register command and write command, pay attention to the following $\overline{WP}$ valid timing.

While write or write status register command is executed, by setting $\overline{WP}$ = "L" in cancel valid area, command can be cancelled. The area from command ope code before $\overline{CS}$ rise at internal automatic write start becomes the cancel valid area. However, once write is started, any input cannot be cancelled. $\overline{WP}$ input becomes Don't Care, and cancellation becomes invalid.

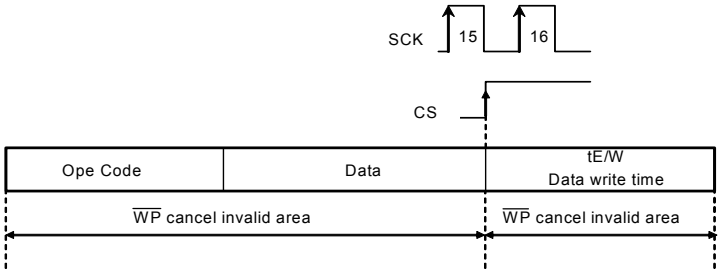


Fig.42 $\overline{WP}$ valid timing (WRSR)

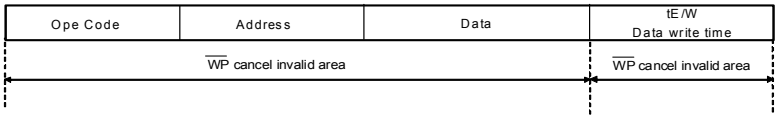


Fig.43 $\overline{WP}$ valid timing (WRITE)

● $\overline{HOLD}$ pin

By $\overline{HOLD}$ pin, command communication can be stopped temporarily (HOLD status). The $\overline{HOLD}$ pin carries out command communications normally when it is HIGH. To get in HOLD status, at command communication, when SCK=LOW, set the $\overline{HOLD}$ pin LOW. At HOLD status, SCK and SI become Don't Care, and SO becomes high impedance (High-Z). To release the HOLD status, set the $\overline{HOLD}$ pin HIGH when SCK=LOW. After that, communication can be restarted from the point before the HOLD status. For example, when HOLD status is made after A5 address input at read, after release of HOLD status, by starting A4 address input, read can be restarted. When in HOLD status, leave $\overline{CS}$ LOW. When it is set $\overline{CS}$ =HIGH in HOLD status, the IC is reset, therefore communication after that cannot be restarted.

●Method to cancel each command

○READ

・Method to cancel : cancel by $\overline{CS}$ = “H”

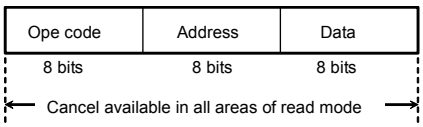


Fig.44 READ cancel valid timing

○RDSR

・Method to cancel : cancel by $\overline{CS}$ = “H”

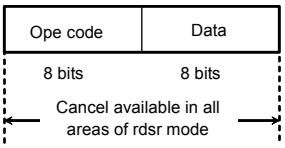


Fig.45 RDSR cancel valid timing

○WRITE, PAGE WRITE

a: Ope code, address input area.
Cancellation is available by $\overline{CS}$ ="H"
b: Data input area (D7~D1 input area)
Cancellation is available by $\overline{CS}$ ="H"
c: Data input area (D0 area)
When $\overline{CS}$ is started, write starts.
After $\overline{CS}$ rise, cancellation cannot be made by any means.
d: tE/W area.
Cancellation is available by $\overline{CS}$ = “H”. However, when write starts ($\overline{CS}$ is started) in the area c, cancellation cannot be made by any means. And by inputting on SCK clock, cancellation cannot be made. In page write mode, there is write enable area at every 8 clocks.

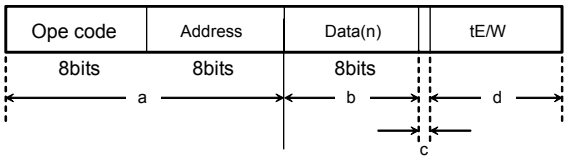
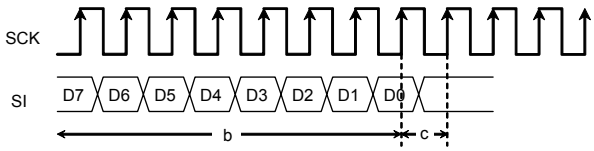


Fig.46 WRITE cancel valid timing



Note 1) If Vcc is made OFF during write execution, designated address data is not guaranteed, therefore write it once again.
Note 2) If $\overline{CS}$ is started at the same timing as that of the SCK rise, write execution / cancel becomes unstable,therefore, it is necessary to fall in SCK = “L” area. As for SCK rise, assure timing of tCSS / tCSH or higher.

○WRSR

a: From ope code to 15 rise.
Cancel by $\overline{CS}$ ="H".
b: From 15 clock rise to 16 clock rise (write enable area).
When $\overline{CS}$ is started, write starts.
After $\overline{CS}$ rise, cancellation cannot be made by any means.
c: After 16 clock rise.
Cancel by $\overline{CS}$ ="H". However, when write starts ($\overline{CS}$ is started) in the area b, cancellation cannot be made by any means.
And, by inputting on SCK clock, cancellation cannot be made.

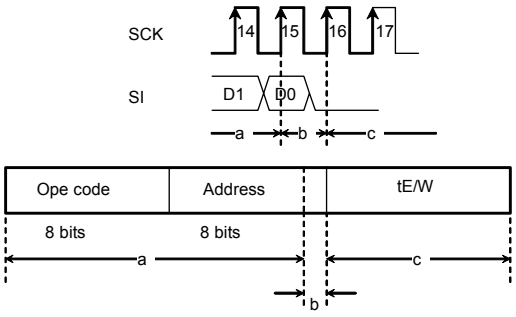


Fig.47 WRSR cancel valid timing

Note 1) If Vcc is made OFF during write execution, designated address data is not guaranteed, therefore write it once again
Note 2) If $\overline{CS}$ is started at the same timing as that of the SCK rise, write execution / cancel becomes unstable, therefore, it is necessary to fall in SCK = “L” area. As for SCK rise, assure timing of tCSS / tCSH or higher.

○WREN/WRDI

a: From ope code to clock rise, cancel by $\overline{CS}$ = “H”.
b: Cancellation is not available when $\overline{CS}$ is started after 7 clock.

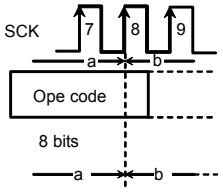


Fig.48 WREN/WRDI cancel valid timing

●High speed operation

In order to realize stable high speed operations, pay attention to the following input / output pin conditions.

○Input pin pull up, pull down resistance

When to attach pull up, pull down resistance to EEPROM input pin, select an appropriate value for the microcontroller V_{OL}, I_{OL} from V_{IL} characteristics of this IC.

○Pull up resistance

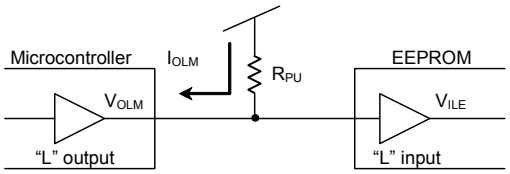


Fig.49 Pull up resistance

$$R_{PU} \geq \frac{V_{CC}-V_{OLM}}{I_{OLM}} \quad \cdots ①$$

$$V_{OLM} \leq V_{ILE} \quad \cdots ②$$

Example) When Vcc=5V, V_{ILM}=1.5V, V_{OLM}=0.4V, I_{OLM}=2mA, from the equation ①,

$$R_{PU} \geq \frac{5-0.4}{2\times10^{-3}}$$

$$\therefore R_{PU} \geq 2.3[k\Omega]$$

With the value of R_{PU} to satisfy the above equation, V_{OLM} becomes 0.4V or higher, and with V_{ILE} (=1.5V), the equation ② is also satisfied.

- V_{ILM} :EEPROM V_{IH} specifications
- V_{OLM} :Microcontroller V_{OL} specifications
- I_{OLM} :Microcontroller I_{OL} specifications

And, in order to prevent malfunction, mistake write at power ON/OFF, be sure to make $\overline{CS}$ pull up.

○Pull down resistance

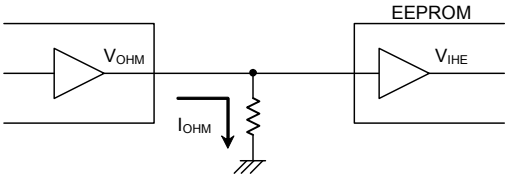


Fig.50 Pull down resistance

$$R_{PD} \geq \frac{V_{OHM}}{I_{OHM}} \quad \cdots ③$$

$$V_{OHM} \geq V_{IHE} \quad \cdots ④$$

Example) When V_{CC}=5V, V_{OHM}=V_{CC}-0.5V, I_{OHM}=0.4mA, V_{IHM}=V_{CC}×0.7V, from the equation③,

$$R_{PD} \geq \frac{5-0.5}{0.4\times10^{-3}}$$

$$\therefore R_{PU} \geq 11.3[k\Omega]$$

Further, by amplitude VIHE, VILE of signal input to EEPROM, operation speed changes. By inputting signal of amplitude of V_{CC} / GND level to input, more stable high speed operations can be realized. On the contrary, when amplitude of 0.8V_{CC} / 0.2Vcc is input, operation speed becomes slow. ※1

In order to realize more stable high speed operation, it is recommended to make the values of R_{PU}, R_{PD} as large as possible, and make the amplitude of signal input to EEPROM close to the amplitude of V_{CC} / GND level.

(※1 At this moment, operating timing guaranteed value is guaranteed.)

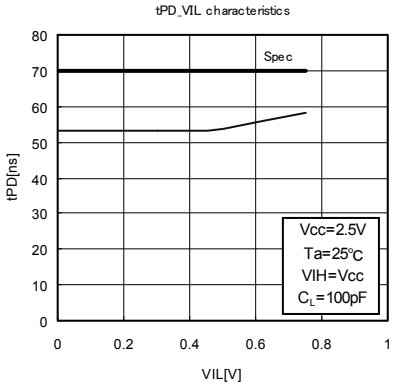


Fig.51 V_{IL} dependency of data output delay time

○SO load capacity condition

Load capacity of SO output pin affects upon delay characteristic of SO output. (Data output delay time, time from $\overline{\text{HOLD}}$ to High-Z) In order to make output delay characteristic into higher speed, make SO load capacity small. In concrete, “Do not connect many devices to SO bus”, “Make the wire between the controller and EEPROM short”, and so forth.

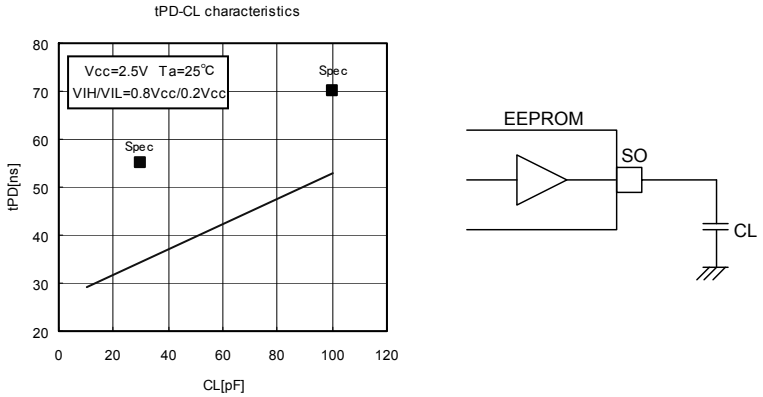


Fig.52 SO load dependency of data output delay time

○Other cautions

Make the wire length from the microcontroller to EEPROM input signal same length, in order to prevent setup / hold violation to EEPROM, owing to difference of wire length of each input.

●Equivalent circuit

○Output circuit

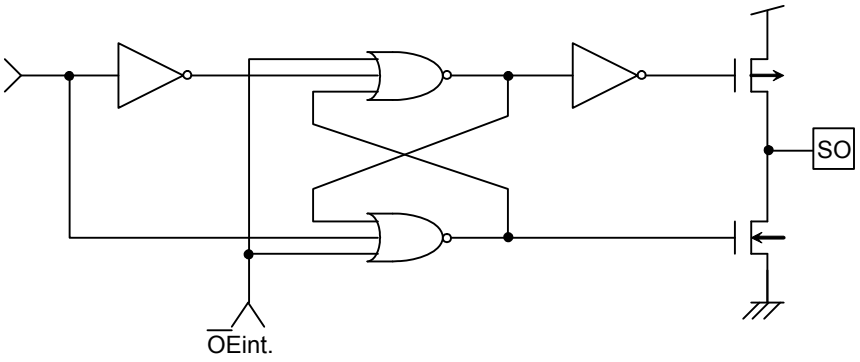


Fig.53 SO output equivalent circuit

○Input circuit

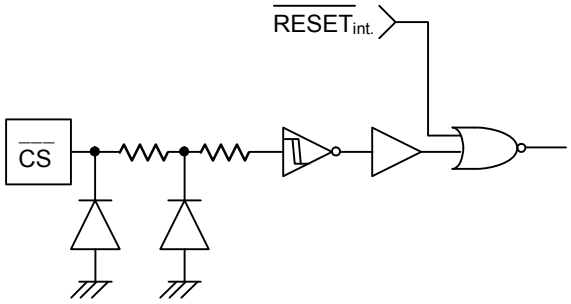


Fig.54 $\overline{CS}$ input equivalent circuit

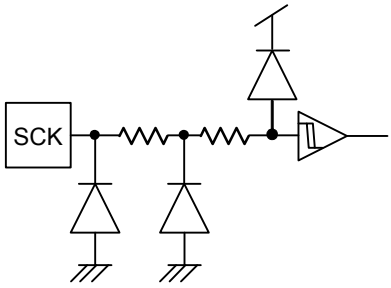


Fig.55 SCK input equivalent circuit

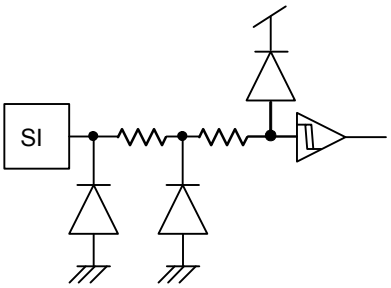


Fig.56 SI input equivalent circuit

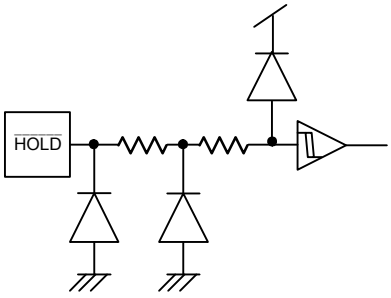


Fig.57 $\overline{HOLD}$ input equivalent circuit

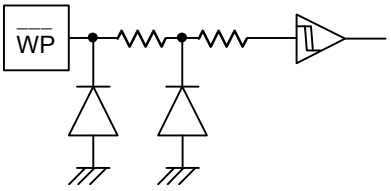


Fig.58 $\overline{WP}$ input equivalent circuit

●Notes on power ON/OFF

○At power ON/OFF, set $\overline{CS}$ "H" (=Vcc).

When $\overline{CS}$ is "L", this IC gets in input accept status (active). If power is turned on in this status, noises and the likes may cause malfunction, mistake write or so. To prevent these, at power ON, set $\overline{CS}$ "H". (When $\overline{CS}$ is in "H" status, all inputs are canceled.)

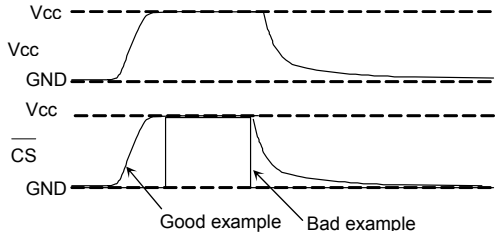


Fig.59 CS timing at power ON/OFF

(Good example) $\overline{CS}$ terminal is pulled up to Vcc.
At power OFF, take 10ms or higher before supply. If power is turned on without observing this condition, the IC internal circuit may not be reset, which please note.

(Bad example) $\overline{CS}$ terminal is "L" at power ON/OFF.
In this case, $\overline{CS}$ always becomes "L" (active status), and EEPROM may have malfunction, mistake write owing to noises and the likes.
Even when $\overline{CS}$ input is High-Z, the status becomes like this case, which please note.

○P.O.R. circuit

This IC has a P.O.R. (Power On Reset) circuit as mistake write countermeasure. After P.O.R. action, it gets in write disable status. The P.O.R. circuit is valid only when power is ON, and does not work when power is OFF. When power is ON, if the recommended conditions of the following tR, tOFF, and Vbot are not satisfied, it may become write enable status owing to noises and the likes.

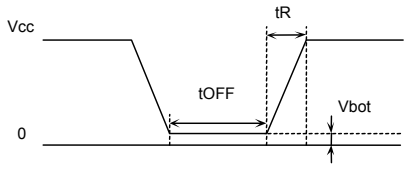


Fig.60 Rise waveform

Recommended conditions of t_R, t_{OFF}, Vbot

t_R	t_{OFF}	Vbot
10ms or below	10ms or higher	0.3V or below
100ms or below	10ms or higher	0.2V or below

●Noise countermeasures

○Vcc noise (bypass capacitor)

When noise or surge gets in the power source line, malfunction may occur, therefore, for removing these, it is recommended to attach a bypass capacitor (0.1μF) between IC Vcc and GND. At that moment, attach it as close to IC as possible. And, it is also recommended to attach a bypass capacitor between board Vcc and GND.

○SCK noise

When the rise time (tR) of SCK is long, and a certain degree or more of noise exists, malfunction may occur owing to clock bit displacement. To avoid this, a Schmitt trigger circuit is built in SCK input. The hysterisis width of this circuit is set about 0.2V, if noises exist at SCK input, set the noise amplitude 0.2Vp-p or below. And it is recommended to set the rise time (tR) of SCK 100ns or below. In the case when the rise time is 100ns or higher, take sufficient noise countermeasures. Make the clock rise, fall time as small as possible.

○ $\overline{WP}$ noise

During execution of write status register command, if there exist noises on $\overline{WP}$ pin, mistake in recognition may occur and forcible cancellation may result, which please note. To avoid this, a Schmitt trigger circuit is built in $\overline{WP}$ input. In the same manner, a Schmitt trigger circuit is built in SI input, SI input and $\overline{HOLD}$ input too.

●Notes for use

(1) Described numeric values and data are design representative values, and the values are not guaranteed.

(2) We believe that application circuit examples are recommendable, however, in actual use, confirm characteristics further sufficiently. In the case of use by changing the fixed number of external parts, make your decision with sufficient margin in consideration of static characteristics and transition characteristics and fluctuations of external parts and our LSI.

(3) Absolute maximum ratings
If the absolute maximum ratings such as impressed voltage and operating temperature range and so forth are exceeded, LSI may be destructed. Do not impress voltage and temperature exceeding the absolute maximum ratings. In the case of fear exceeding the absolute maximum ratings, take physical safety countermeasures such as fuses, and see to it that conditions exceeding the absolute maximum ratings should not be impressed to LSI.

(4) GND electric potential
Set the voltage of GND terminal lowest at any action condition. Make sure that each terminal voltage is higher than that of GND terminal.

(5) Heat design
In consideration of permissible dissipation in actual use condition, carry out heat design with sufficient margin.

(6) Terminal to terminal short circuit and wrong packaging
When to package LSI onto a board, pay sufficient attention to LSI direction and displacement. Wrong packaging may destruct LSI. And in the case of short circuit between LSI terminals and terminals and power source, terminal and GND owing to foreign matter, LSI may be destructed.

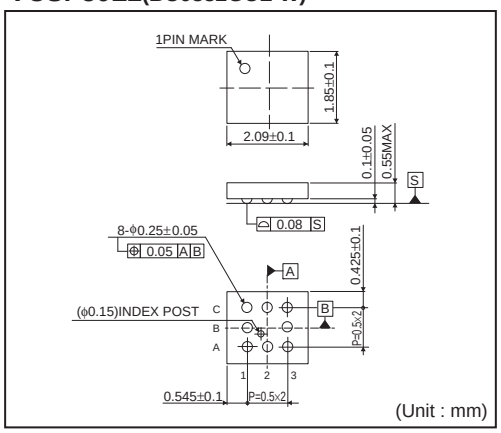
(7) Use in a strong electromagnetic field may cause malfunction, therefore, evaluate design sufficiently.

●Ordering part number

B	U	9	8	3	2	G	U	L	-	W	E	2

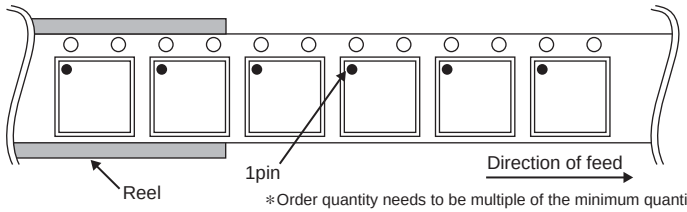
Part No.	Part No.	Package GUL : VCSP50L2	W-CELL	Packaging and forming specification E2: Embossed tape and reel

VCSP50L2(BU9832GUL-W)



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

Notes

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