AMD

AMD-750™

Chipset

Overview

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AMD-750™ Chipset

The AMD Athlon™ processor powers the next generation of computing platforms, delivering the ultimate performance for cutting-edge applications and an unprecedented computing experience.

The AMD-750™ chipset is a highly integrated system logic solution that delivers enhanced performance for the AMD Athlon processor and other AMD Athlon frontside bus-compatible processors. The AMD-750 chipset consists of the AMD-751™ system controller in a 492-pin plastic ball-grid array (PBGA) package and the AMD-756™ peripheral bus controller.

The AMD-751 system controller features the AMD Athlon frontside bus, system memory controller, accelerated graphics port (AGP) controller, and peripheral component interconnect (PCI) bus controller.

The AMD-756 peripheral bus controller features three primary blocks (PCI-to-ISA bridge, USB controller interface, EIDE UDMA-33 and -66 controller), each with independent access to the PCI bus, a complete set of PCI interface signals and state machines, and capable of working independently with separate devices.

Figure 1 on page 2 shows the block diagram of the AMD-750 chipset system.

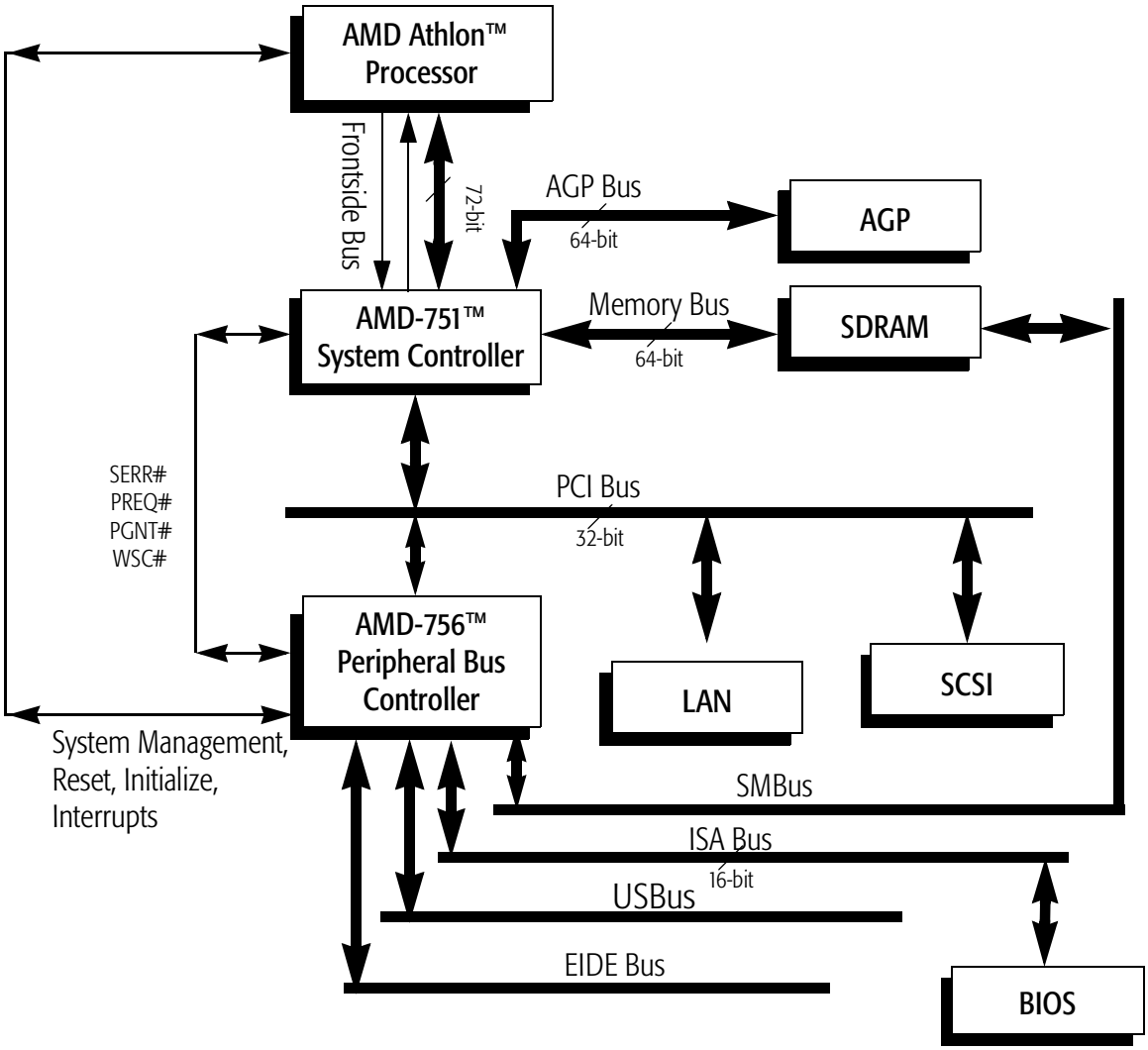

Figure 1. AMD-750™ Chipset System Block Diagram

AMD-751™ System Controller

Key features of the AMD-751 system controller are provided in this section. For more information, see the *AMD-751™ System Controller Data Sheet*, order# 21910.

The AMD-751 system controller is designed with the following features:

- The AMD Athlon frontside bus supports three 200-MHz high-speed channels
- The 33-MHz 32-bit PCI 2.2-compliant bus interface supports up to six masters
- The 66-MHz AGP 2.0-compliant interface supports 2x data transfer mode
- High-speed memory—The AMD-751 system controller is designed to support 100-MHz PC-100 revision 1.0 SDRAM DIMMs

AMD Athlon™ System Bus

The AMD Athlon frontside bus has the following features:

- High-performance point-to-point system bus topology
- Source synchronous clocking for high-speed transfers
- HSTL-like low-voltage swing transceiver logic signal levels
- Three 200-MHz independent high-speed channels:
  - 13-pin processor request channel
  - 13-pin system probe channel
  - 72-pin data transfer channel (8-bit ECC)
- 1.6 Gbytes per second peak-data-transfer rates at 200 MHz
- Large 64-byte (cache line) data burst transfers
- Data Buffers:
  - Memory write FIFO (MWF)
  - Memory read FIFO (MRF)
  - PCI/APCI (AGP-PCI) write buffer
  - PCI/APCI read buffer

- Transaction Queues:
  - Command queue (CQ)
  - Memory write queue (MWQ)
  - Memory read queue (MRQ)
  - Probe (snoop) queue (PQ)

Integrated Memory Controller

The integrated memory controller has the following features:

- Memory Request Organizer (MRO)—Serves as a data crossbar, determines request dependencies, and optimizes scheduling of memory requests
- The AMD-751 system controller supports the following concurrences:
  - Processor-to-main-memory with PCI-to-main-memory
  - Processor-to-main-memory with AGP-to-main-memory
  - Processor-to-PCI with PCI-to-main-memory or AGP-to-main-memory
- Memory error correcting code (ECC) support
- Supports the following DRAM:
  - Up to three non-buffered PC-100 revision 1.0 SDRAM DIMMs using 16-Mbit, 64-Mbit, and 128-Mbit technology
  - 64-bit data width, plus 8-bit ECC paths
  - Flexible row and column addressing
- Supports up to 768 Mbytes of memory
- Four open pages within one CS (device selected by chip select) for one quadword
- Default two-page leapfrog policy for eight quadword requests
- BIOS-configurable memory-timing parameters and configuration parameters
- 3.3-V memory interface operation with no external buffers
- Four cache lines (32 quadwords) of processor-to-DRAM posted write buffers with full read-around capability
- Concurrent DRAM writeback and read-around-write
- Burst read and write transactions

- Decoupled and burst DRAM refresh with staggered CS timing
- Provides the following refresh options:
  - Programmable refresh rate
  - CAS-before-RAS
  - Populated banks only
  - Chipset powerdown via SDRAM automatic refresh command
  - Automatic refresh of idle slots—improves bus availability for memory access by the processor or system

PCI Bus Controller

The PCI bus controller has the following features:

- Compliance with *PCI Local Bus Specification, Revision 2.2*
- Supports six PCI masters
- 32-bit interface, compatible with 3.3-V and 5-V PCI I/O
- Synchronous PCI bus operation up to 33 MHz
- PCI-initiator peer concurrence
- Automatic processor-to-PCI burst cycle detection
- Four-entry, 64-bit PCI master (processor or AGP) write FIFO
- Extensive utilization of FIFOs
- Zero wait-state PCI initiator and target burst transfers
- PCI-to-DRAM data streaming up to 132 Mbytes per second
- Enhanced PCI command optimization, such as memory read line (MRL), memory read multiple (MRM), and memory-write-and-invalidate (MWI)
- Timer-enforced fair arbitration between PCI initiators
- Supports advanced concurrency
- Supports retry disconnect for improved bus utilization
- PCI read buffer keeps track of each master
- PCI target request queue

AGP Features

The AGP features include the following:

- Bus Features
  - Compliance with AGP 1.0 specification
  - Synchronous 66-MHz 1x and 2x data-transfer modes
  - Multiplexed and demultiplexed transfers
  - Up to four pipelined grants
  - Support of sideband address (SBA) bus
- Request Queue Features
  - Separate read-request and write-request queues
  - Reordering of high-priority requests over low-priority requests in queue
  - Concurrent issuing of requests from both the write queue and read queue
  - Selects next request to optimize bus utilization
- Transaction Queues
  - Memory-to-AGP and processor-to-AGP transaction queues
- FIFO Features
  - 16-entry (64-bit) AGP-to-memory write FIFO
  - 64-entry (64-bit) memory-to-AGP read FIFO
- Secondary PCI Bus Features
  - Pipelined burst reads and writes
  - Extensive utilization of FIFOs
- GART (graphics address remapping table) Features
  - Conventional (two-level) GART scheme
  - Eight-entry, fully-associative GART table cache (GTC)
  - Three fully-associative GART directory caches (GDC)
    - One 4-entry for PCI
    - One 8-entry for the processor
    - One 16-entry for AGP

Power Management

The power management features include the following:

- Support for both ACPI and Microsoft® PC 98 power management
- AMD-751 system controller supports the following power states:
  - Processor Halt/Stop-Grant/Sleep states
  - Power-On-Suspend

AMD-756™ Peripheral Bus Controller

Key features of the AMD-756 controller are listed in this section. For more information, see the *AMD-756™ Peripheral Bus Controller Data Sheet*, order# 22548.

The AMD-756 contains the following functional units:

- Integrated ISA bus controller
- Enhanced master-mode PCI IDE controller with ultra DMA-33/66 support
- USB controller
- Keyboard/mouse controller
- Real-time clock

PCI-to-ISA Bridge

The AMD-756 controller includes a PC97-compliant PCI-to-ISA bridge with the following features:

- PCI 2.2-compliant interface
- Eight-level doubleword buffer between PCI and ISA buses
- Dual cascaded AT-8259-compatible interrupt controllers
- Dual AT-8237-compatible DMA controllers
- Type F DMA transfer support
- Support for ISA legacy distributed DMA across the PCI bus
- AT-8254-compatible programmable interval timer
- Integrated real-time clock w/extended 256-byte CMOS RAM
- Programmable ISA bus clock
- Fast reset and gate A20 operation
- Edge-triggered or level-sensitive interrupts
- Flash, 2-Mbyte EPROM, BIOS support
- Integrated keyboard controller with PS/2 mouse support

Enhanced IDE Controllers

The AMD-756 controller includes enhanced master mode PCI and IDE controllers with the following features:

- Ultra DMA-33/66 support for a primary and secondary dual-drive port
- Transfer rates up to 33 Mbytes per second supporting PIO modes 1–4, multi-word DMA mode-2 drivers, and up to 66 Mbytes per second supporting the ultra DMA-66 interface
- Sixteen-level doubleword prefetch and write buffers
- Commands can be interleaved between the two channels
- Bus master programming interface for compliance with SFF-8038i 1.0 and Microsoft Windows® 95
- Full-featured scatter-gather capability
- Support for ATAPI-compliant devices
- Support for PCI-native and ATA-compatibility modes
- Complete bus mastering software driver support

Universal Serial Bus Controller

The AMD-756 controller includes a universal serial bus (USB) controller with the following features:

- USB 1.0 and OHCI compliant
- Sixteen-level doubleword FIFO for burst PCI bus access
- Root hub and four ports
- Integrated physical-layer transceivers with over-current detection status on USB inputs
- Legacy keyboard and PS/2 mouse support

Plug-n-Play Support

The AMD-756 controller supports plug-n-play with the following features:

- PCI interrupts steerable to any of three interrupt channels
- Microsoft Windows 98 and plug-n-play BIOS compliant
- Serial IRQ compliant

Power Management

The AMD-756 controller includes the following sophisticated power management features:

- Supports advanced configuration and power interface power management (ACPI 1.0 compliant)
- Supports legacy power management (APM 1.2 compliant)
- Supports soft-off and power-on suspend with hardware automatic wakeup
- Two general-purpose timers, one system-inactivity timer, and a 24-bit or 32-bit APCI-compliant timer
- Dedicated external modem-ring input pin for system wakeup
- Normal, doze, sleep, suspend, and conserve modes
- Eighteen multiplexed general-purpose I/O pins
- SMBus implementation for JEDEC-compatible DIMM identification and on-board device power/thermal control
- Primary and secondary interrupt differentiation for individual channels
- Clock throttling control
- Multiple internal and external SMI# sources for flexible power management