EG&G RETICON

M Series Multiplexers

T-41-55

The EG&G Reticon M Series parallel-in-serial-out multiplexer is a general purpose digital scanner for hybrid imager applications, especially applicable for infrared arrays made with compound semiconductor materials (InSb, etc.). These devices are available in die form and dual-inline packages for evaluation and/or nonhybrid applications (see Figure 1). A simplified block diagram of the multiplexer is shown in Figure 2.

The M Series is available in four lengths (32, 64, 128, or 256 multiplexing switches) on 4-mil center-to-center spacing. Each switch has an input connection bonding pad on-chip, with a 70 µm x 200 µm area for wire bonds or flip-chip bonds (see Figures 3 and 4).

Mirror-image configuration is provided for interdigitated image applications (see Typical Application). The M Series is fabricated in standard Reticon PMOS silicon gate technology. Very small photodiodes are connected to the multiplex switches for use in testing.

Key Features

- 32, 64, 128 or 256 elements (RL0032M, RL0064M, RL0128M, and RL0256M respectively)
- 100 µm spacing
- On-chip bonding pad suitable for wire bonds or flip-chip bonds
- Photodiode with each bonding pad for optical testing
- Standard and mirror images available for interdigitated linear array
- Low power requirements
- Diode reset feature
- Dummy video output for fixed pattern cancellation
- Low output video line capacitance

Operation

As shown in Figure 2, the shift register is clocked with a two-phase complementary clock (see clock specifications). A start pulse is required to initiate the scan (see start pulse specification). Upon entry of the start pulse, the dummy and the active video signals are sequentially interrogated through the multiplexer switches as the loaded bit is clocked down the shift register. An End-Of-Scan (EOS) signal occurs at the termination of each scan.

The off-chip sensors are bonded to the pads. There are two sets of switches, one an active and the other a dummy switch. The sources of the active switches are connected to the bonding pads, while the dummy switches are not connected to any pads. When the switches are simultaneously scanned by the shift register, both the signal charge and the dummy signal are read out through the active and dummy video lines, respectively. The dummy video line output signal is then subtracted from the active video line output signal in external circuitry, minimizing the fixed pattern noise generated by the multiplexing switches.

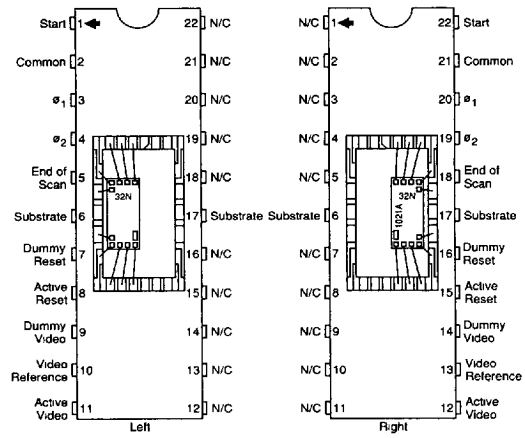

Figure 1. Pinout Configurations

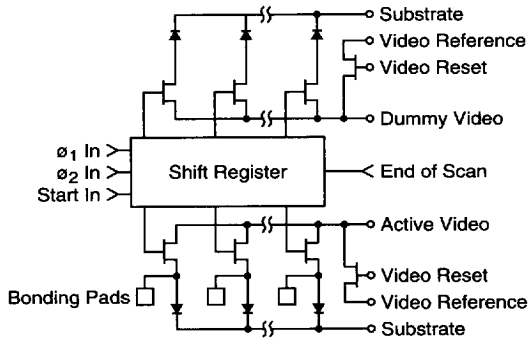

Figure 2. Simplified Block Diagram of the Multiplexer

Multiplex switch resistance as a function of clock voltage is provided in Table 1. The test setup used to obtain these resistance measurements is shown in Figure 9. I/O capacitance is given in Table 2.

Reset switches are provided on each video for use in signal processing (see Typical Application). The switch resistance values are given in Table 3. A reset switch resistance measurement set-up is shown in Figure 10.

General I/O timing relationships are shown in Figure 5. The detailed clock specifications and timing are covered under Clock, Start and EOS Specifications.

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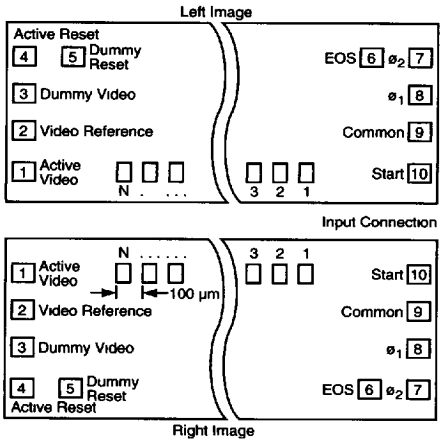


Figure 3. Left and Right Side Flip Chip Set (Shift Register Scanning from Right to Left)

The photodiode sites, indicated in Figure 2, are used for testing. They are each in parallel with a sensor bonding pad; together with the pad, each represents a capacitance of 0.3 pF.

Electrical Specifications

1. Shift Register Clocks ($ø_1$ and $ø_2$)

These clocks operate the shift register. For optimum multiplexer operation the clocks should cross at the midpoint. Figure 6 shows the typical midpoint crossing of 50%. The range of operation should be between 25% to 75%.

The clock rise (t_r) and fall (t_f) times should be between 5 ns and 100 ns. The clock amplitude operates within the range -9V to -16V and is typically at -15V with respect to the substrate. The clock frequency f($ø_1$) ranges from several kHz to 7 MHz.

2. Start Pulse ($ø_{ST}$)

The start pulse ($ø_{ST}$) loads the shift register with a voltage pulse to initiate the scanning process. It loads the register on each $ø_2$ low-to-high (negative-to-positive) transition as long as the start pulse is held low. Therefore, to ensure that only one bit is loaded, the start pulse should be low during only one $ø_2$ rising edge. Figure 5 illustrates the timing relationship with respect to $ø_2$. The rise (t_r) and fall (t_f) times should be between 5 ns and 100 ns. The clock amplitude of $ø_{ST}$ should be between -10V and -7V. The setup time (t_{set}) should be at least 30 ns, the hold time (t_{hold}) at least 30 ns, and t_{off} at least 50 ns.

Note: The shift register will load multiple bits if the start pulse is low for more than one $ø_2$ rising edge.

3. End of Scan (EOS)

The EOS pulse is generated at the output of the shift register to mark the termination of the scan. The last position is accessed with the $ø_1$ clock going negative. On the next $ø_2$ falling edge, the output pulse is applied to the gate of the EOS transistor. The drain of this transistor is brought out on the EOS pad, and the source is tied to the common. Therefore, tying a resistor >5KΩ from EOS to -5V (referenced to substrate) provides a load on which a positive-going pulse is observed upon the scan termination. See Figure 5 for EOS timing relationship referenced to $ø_2$. The internal delays (delay for Turn On [t_{dn}] and Turn Off [t_{df}]) are typically in range of 50 ns < t_{dn} < 100 ns and 10 ns < t_{df} < 100 ns. The internal switch resistance with -15V clocks is typically 8KΩ. EOS amplitude is determined by the value of the resistor tied from EOS to the minus supply. Typical resistance value of 10KΩ provides a positive-going 4V pulse.

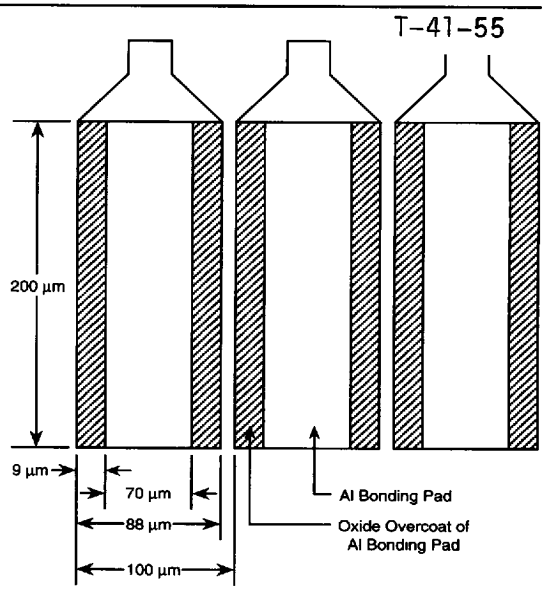


Figure 4. Switch Connection Bonding Pads

Typical Application

Figure 7 shows the interdigitated application of the mirrored devices where both left and right side devices are used with an array of sensor diodes. All three chips are bonded in a hybrid substrate, the pads bonded as shown. The clock inputs and video outputs are then bonded either to other dice on the substrate or to pin connections on a package to accommodate inputs and outputs for the clocks and the video. In this particular application photodiodes are accessed by using two devices, one for accessing the even numbered diodes and the other for the odd numbered diodes in the array. When the multiplexers are scanned, integrated-image charges will appear in sequence at the output, each one proportional to the light exposure at a given site.

Reset switches are provided for use in signal processing. They can be used to integrate signal charges on a capacitor (i.e., the video line capacitor or an external capacitor) then used to reset the capacitor after each multiplex site has been read out (see Figure 5 and Figure 8).

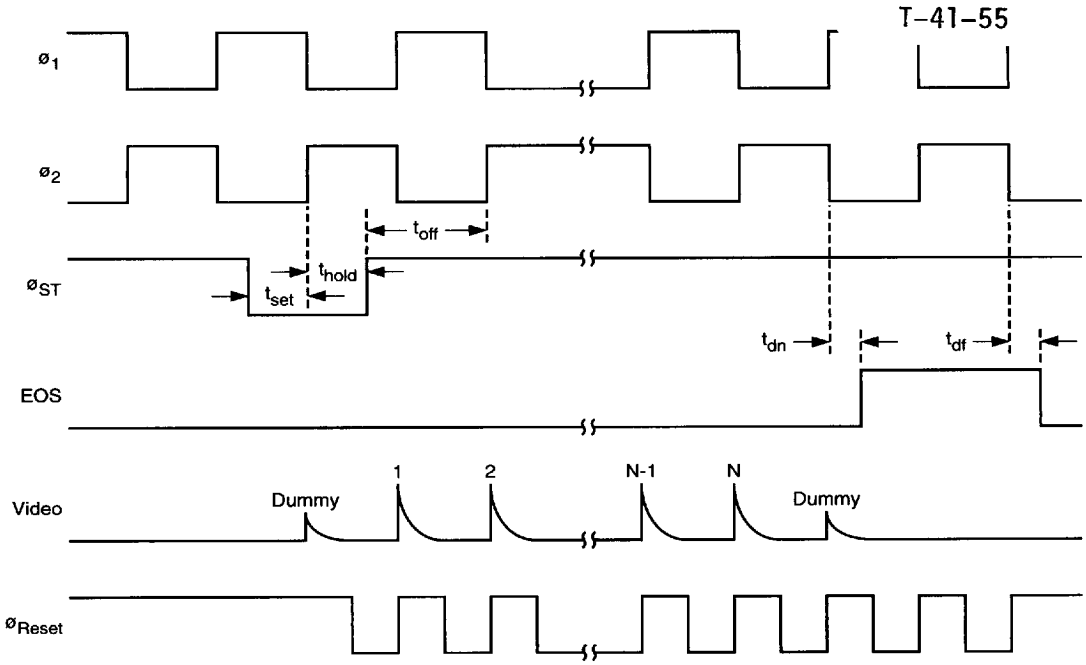


Figure 5. General Linear M Series Timing Diagram

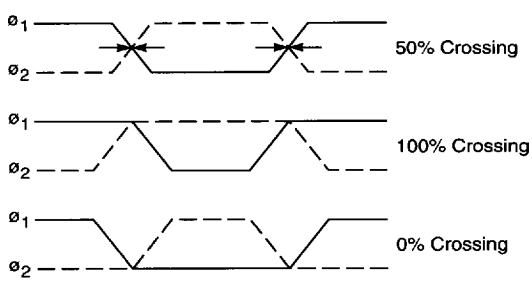


Figure 6. Definition of Clock Crossing

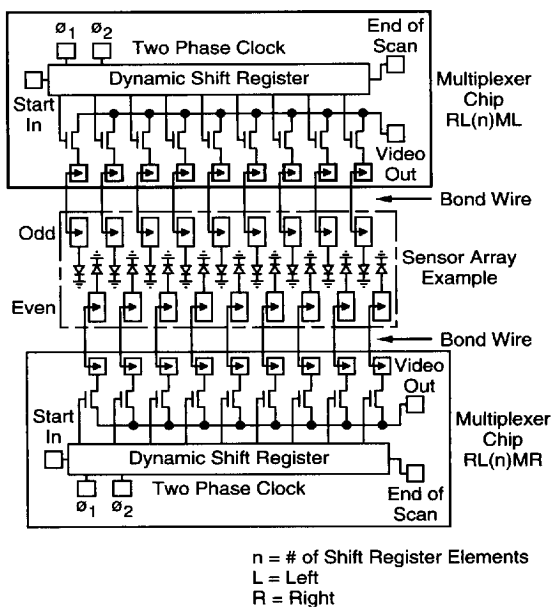
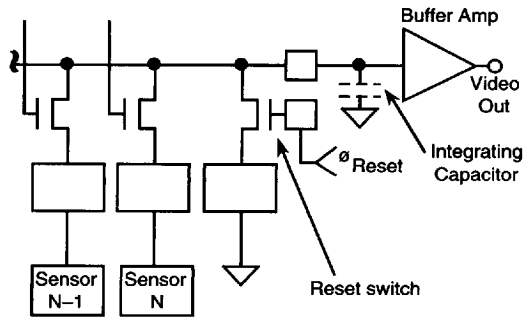
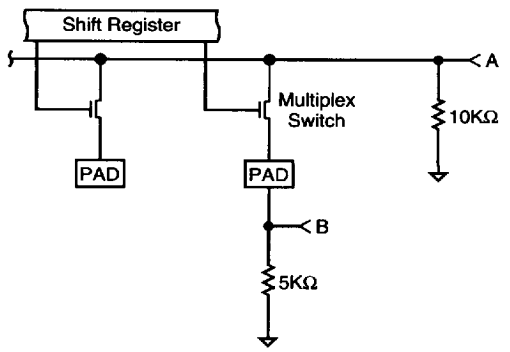


Figure 7. Interdigitated Photodiode Array



Note:
The reset switch can be continuously active, while the shift register remains inactive, thus discharging any extraneous charges accumulating on the video line.

Figure 8. Reset Switch



The resistances were measured using points A and B in the circuit as shown.

Figure 9. Multiplex Switch Resistance Test Set Up

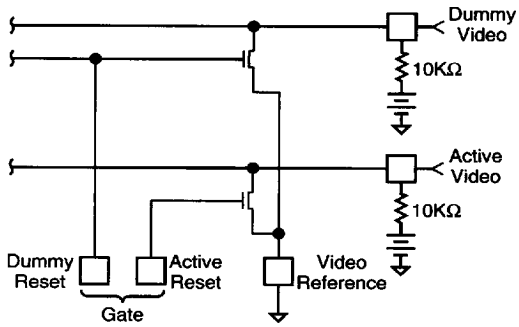


Figure 10. Reset Switch Resistance Measurement Set Up

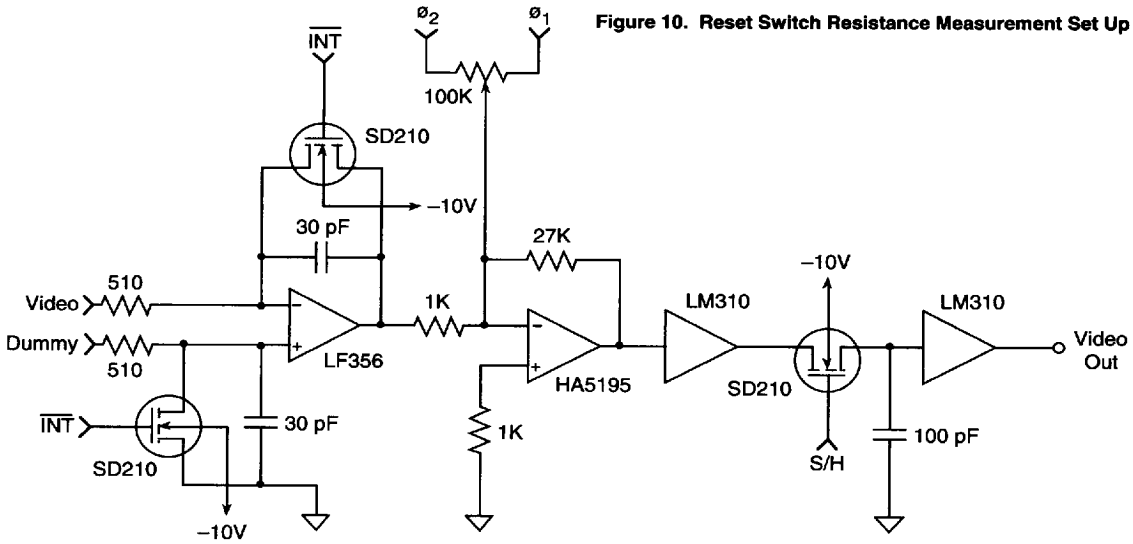


Figure 11. Test Circuit

Table 1. Multiplex Switch On-Resistance versus Clock Amplitude

Small sample variations are less than ±5% of the typical resistance.

Clock Amplitude	Typical Resistance
-15V	8.3 KΩ
-14V	10.5 KΩ
-13V	15.0 KΩ
-12V	26.7 KΩ
-11V	68.0 KΩ
-10V	235.0 KΩ

Table 2. I/O Capacitances [1, 2, 3]

	Device Type			
	256 Taps	128 Taps	64 Taps	32 Taps
$ø_{X1}$	81	41	22	13
$ø_{X2}$	81	41	22	13
$ø_{Start}$	4	3	4	3
EOS	20	11	7	5
Active video	15	8	5	4
Dummy video	15	8	5	4
Active reset	4.5	3.8	1.2	3
Dummy reset	4.5	3.8	1.2	3
Video reference	5	3.5	1.2	3.5

Notes:
1 Capacitance in picofarad (pF).
2 Measured with bias of -5V (with respect to substrate).
3 The readings are typical values.

Table 3. Reset Switch On-Resistance versus Reset Gate Voltage

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Reset Gate Voltage	Resistance of Reset Gate
-15V	3.3 KΩ
-14V	3.5 KΩ
-13V	3.7 KΩ
-12V	4.1 KΩ
-11V	4.7 KΩ
-10V	5.2 KΩ

Table 4. Electro-Optical Characteristics (25°C)

	Min	Typ	Max	Units
Center-to-center spacing landing pads		100		µm
Pad aperture width		175		µm
Pad capacitance		0.3		pF
Dark fixed pattern nonuniformity [1, 2, 5]			±3	$\%V_{SAT}$
Between adjacent elements [1, 2, 5]			2	$\%V_{SAT}$
Photo response nonuniformity [1, 3, 5]		±7	±10	%
Dark signal leakage [1, 4, 5]			4	$\%V_{SAT}$
End of scan resistance		5	10	KΩ
Saturation [1, 3, 5]	1.3	1.6	1.8	V

Notes:
1 All measurements taken with typical clock and power supply voltages, using test circuit in Figure 11.
2 Scan time = 1.3 ms
3 Using 2870°K light source with HA-11 filter
4 Measured at 40 ms scan time
5 This specification applies to the small photodiodes on the die used to test the multiplex switches.

Table 5. Electrical Characteristics (25°C)

	Min	Typ	Max	Units
Clock amplitude [1]	-9	-15	-16	V
Start amplitude [1]	-7		-10	V
Reset clock amplitude [1]	-7	-15	-16	V
Common voltage	+4.5	+5	+5.5	V
Substrate voltage	+4.5	+5	+5.5	V
Video reference [2]	-2	0	+1.0	V
Clock frequency			7	MHz

Notes:
1 Measured with respect to substrate. Substrate is normally run at +5V for compatibility with TTL clock circuits.
2 With +5V substrate and -15V clock with respect to substrate.

	A
RL0032M	1.080±.011
RL0064M	1.080±.011
RL0128M	1.080±.011
RL0256M	1.600±.016

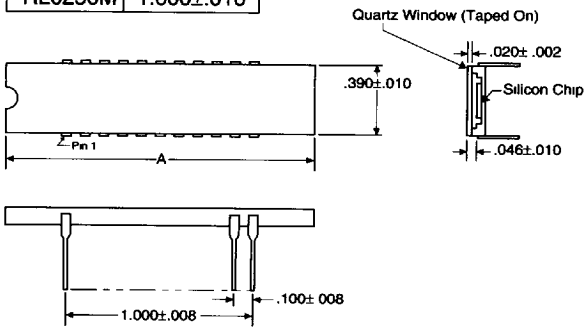

Figure 12. Package Dimensions

Ordering Information*

Mux Type	Package Order Number	Die Order Number
RL0032ML	RL0032MAU-011	RL0032MAD-001
RL0032MR	RL0032MAU-020	RL0032MAD-002
RL0064ML	RL0064MAU-011	RL0064MAD-001
RL0064MR	RL0064MAU-020	RL0064MAD-002
RL0128ML	RL0128MAU-011	RL0128MAD-001
RL0128MR	RL0128MAU-020	RL0128MAD-002
RL0256ML	RL0256MAU-011	RL0256MAD-001
RL0256MR	RL0256MAU-020	RL0256MAD-002

L denotes left element mux
R denotes right element mux
*Includes standard devices. For all options, consult your local sales office.