5 Electrical Characteristics

Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Voltage on any pin with respect to ground	V_S	– 0.4 to V_{DD} + 0.4	V
Ambient temperature under bias	T_A	0 to 70	°C
Storage temperature	T_{stg}	– 65 to 125	°C
Maximum voltage on V_{DD}	V_{DD}	6	V

Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Line Overload Protection

The maximum input current (under overvoltage conditions) is given as a function of the width of a rectangular input current pulse (**figure 54**).

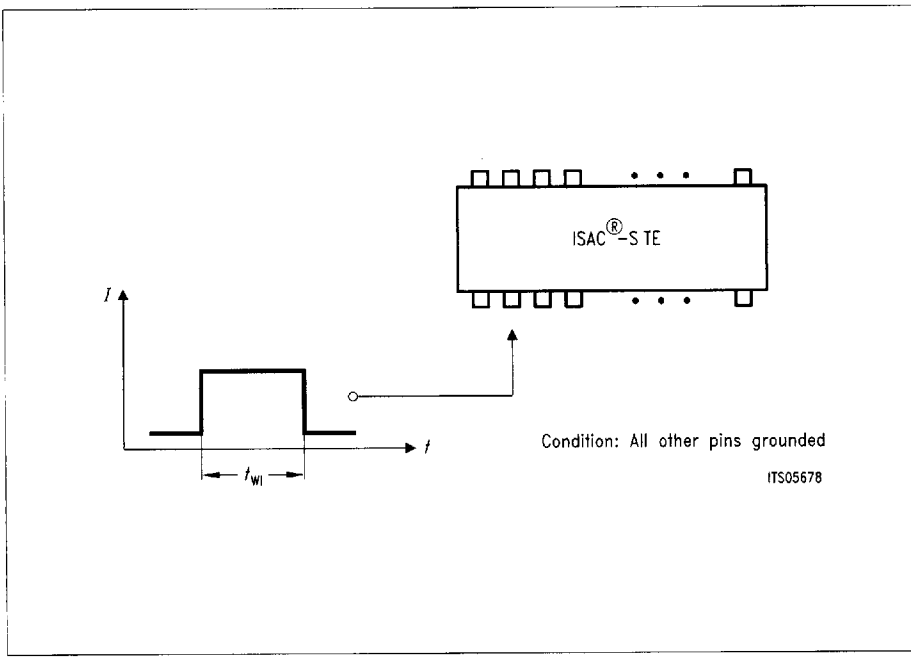


Figure 54
Test Condition for Maximum Input Current

Transmitter Input Current

The destruction limits for negative input signals are given in **figure 55**. $R_i \geq 2\ \Omega$.

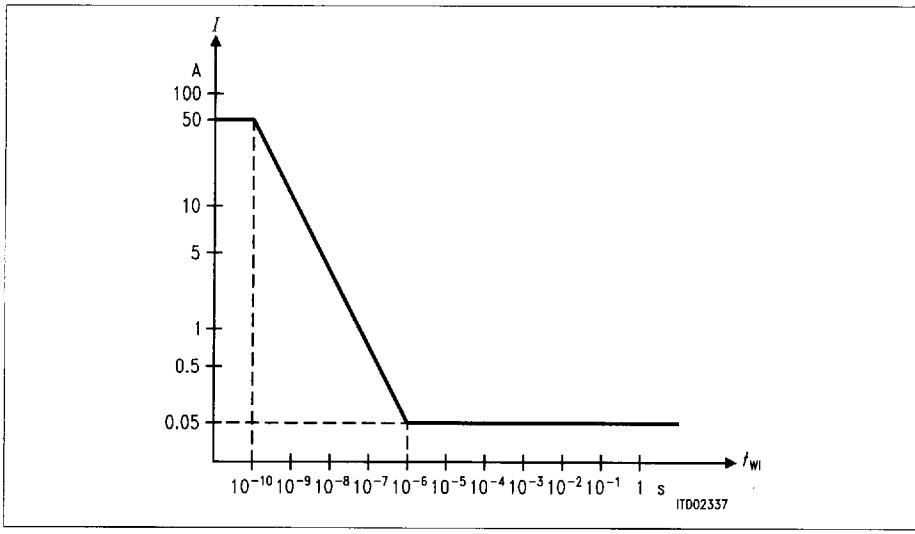


Figure 55

The destruction limits for positive input signals are given in **figure 56**. $R_i \geq 200\ \Omega$.

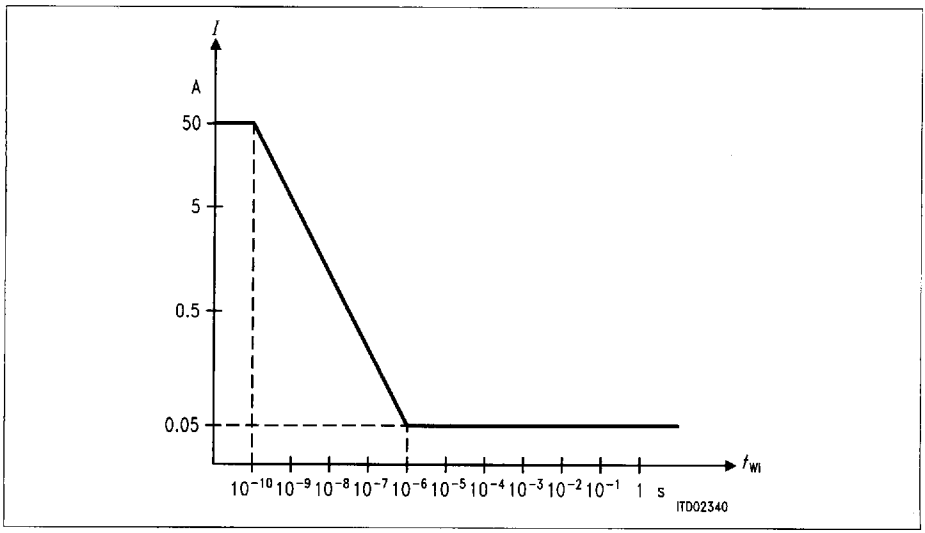
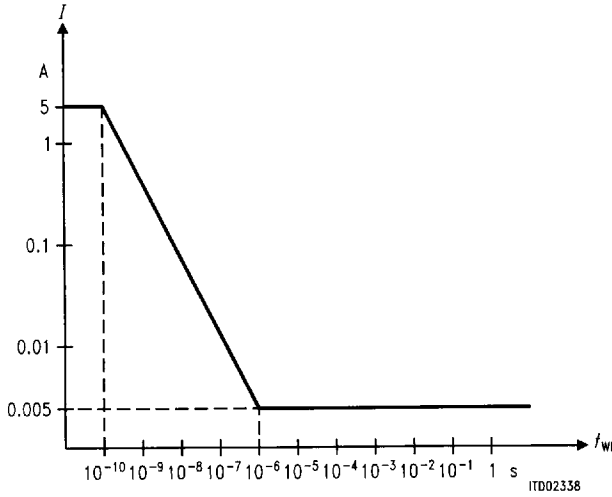


Figure 56

Receiver Input Current

The destruction limits are given in **figure 57**. $R_I \geq 300\ \Omega$.



DC Characteristics

T_A = 0 to 70 °C; V_{DD} = 5 V ± 5 %, V_{SSA} = 0 V, V_{SSD} = 0 V

Parameter		Symbol	Limit Values		Unit	Test Condition		Remarks
			min	max				
L-input voltage		V_{IL}	– 0.4	0.8	V			All pins except SX1,2, SR1,2
H-input voltage		V_{IH}	2.0	V_{DD} + 0.4	V			
L-output voltage L-output voltage (IDP0)		V_{OL} V_{OL1}		0.45 0.45	V V	I_{OL} = 2 mA I_{OL} = 7 mA		
H-output voltage H-output voltage		V_{OH} V_{OH}	2.4 V_{DD} – 0.5		V V	I_{OH} = – 400 µA I_{OH} = – 100 µA		
Power supply current	power down	I_{CC}		1.5	mA		V_{DD} = 5 V Inputs at V_{SS} / V_{DD} No output loads except SX1,2 (50 Ω load)	
	oper-ational (96 kHz)			17	mA	DCL = 1536 kHz		
	Emergency B1 = FF_H, B2 = FF_H, D = 1			7.7	mA	DCL = 1536 kHz		
	B1 = FF_H, B2 = FF_H, D = Flag			7.95	mA	DCL = 1536 kHz		
	B1 = 55_H, B2 = FF_H, D = Flag			8.75	mA	DCL = 1536 kHz		
	B1 = 00_H, B2 = FF_H, D = Flag			10	mA	DCL = 1536 kHz		
Input leakage current		I_{LI}		10	µA	0 V < V_{IN} < V_{DD} to 0 V		All pins except CP/BCL, X2, SX1,2, SR1,2, A0, A1, A3, A4
Output leakage current		I_{LO}		10	µA	0 V < V_{OUT} < V_{DD} to 0 V		

DC Characteristics

T_A = 0 to 70 °C; V_{DD} = 5 V ± 5 %, V_{SSA} = 0 V, V_{SSD} = 0 V (cont'd)

Parameter	Symbol	Limit Values		Unit	Test Condition	Remarks
		min	max			
Input leakage current internal pull-down	I_{LIPD}		120	µA	0 V < V_{IN} < V_{DD} to 0 V	A0, A1, A3, A4, CP/BCL, X2
Absolute value of output pulse amplitude (VSX2 – VSX1)	V_X	2.03 2.10	2.31 2.39	V V	R_L = 50 Ω[1)] R_L = 400 Ω[1)]	SX1,2
Transmitter output current	I_X	7.5	13.4	mA	R_L = 5.6 Ω[1)]	
Transmitter output impedance	R_X	10 0		kΩ Ω	Inactive or during binary one during binary zero R_L = 50 Ω	
Receiver output voltage	V_{SR1}	2.35	2.6	V	I_O < 5 µA	SR1,2
Receiver threshold voltage $V_{SR2} - V_{SR1}$	V_{TR}	225	375	mV	Dependent on peak level	

Note: [1)] Due to the transformer, the load resistance seen by the circuit is four times R_L.

Capacitances

T_A = 25 °C, V_{DD} = 5 V ± 5 %, V_{SSA} = 0 V, V_{SSD} = 0 V, f_c =1 MHz, unmeasuredpins grounded.

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Input capacitance I/O capacitance	C_{IN} $C_{I/O}$		7 7	pF pF	All pins except SR1,2
Output capacitance against V_{SSA}	C_{OUT}		10	pF	SX1,2
Input capacitance	C_{IN}		7	pF	SR1,2
Load capacitance	C_L		50	pF	XTAL1,2

Recommended Oscillator Circuits

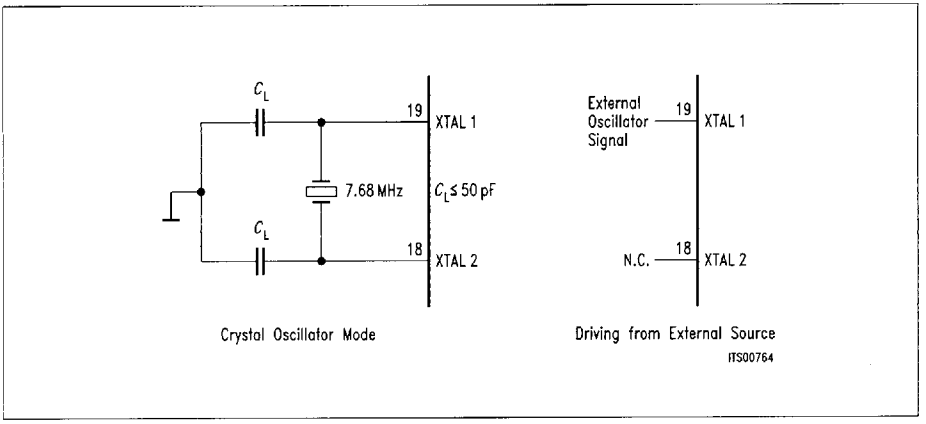


Figure 57
Oscillator Circuits

Crystal Specification

Parameter	Symbol	Limit Values	Unit
Frequency	f	7.680	MHz
Frequency calibration tolerance		max. 100	ppm
Load capacitance	C_L	max. 50	pF
Oscillator mode		fundamental	

Note: The load capacitance C_L depends on the recommendation of the crystal specification. Typical values for C_L are 22 ...33 pF.

XTAL1 Clock Characteristics (external oscillator input)

Parameter	Limit Values	
	min.	max.
Duty cycle	1:2	2:1

AC Characteristics

T_A = 0 to 70 °C, V_{DD} = 5 V ± 5%

Inputs are driven to 2.4 V for a logical "1" and to 0.4 V for a logical "0". Timing measurements are made at 2.0 V for a logical "1" and 0.8 V for a logical "0". The AC-testing input/output waveforms are shown in **figure 59.**

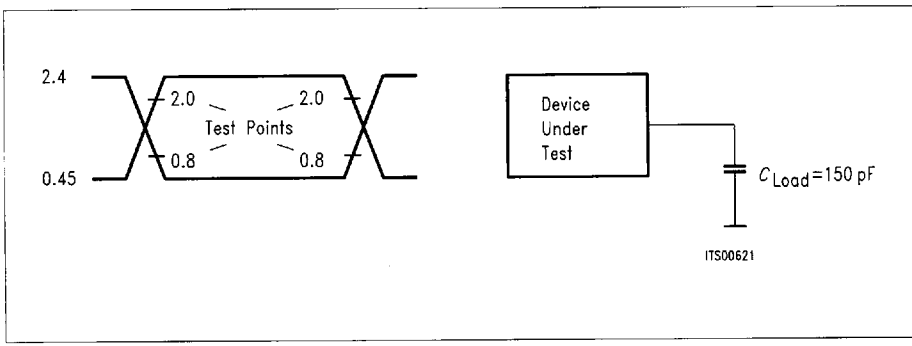


Figure 58
Input/Output Waveform for AC Tests

Microprocessor Interface Timing

Siemens/Intel Bus Mode

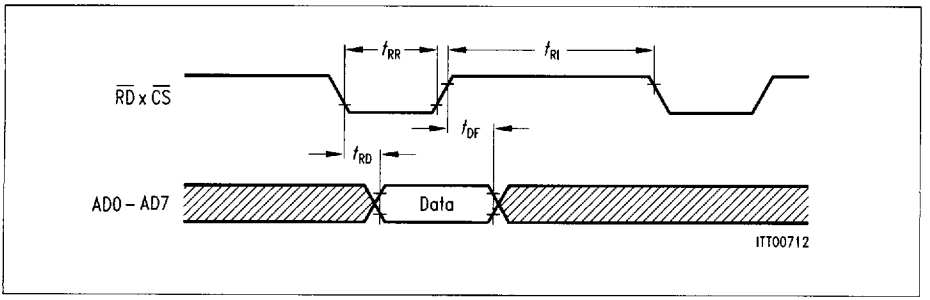


Figure 59
Microprocessor Read Cycle

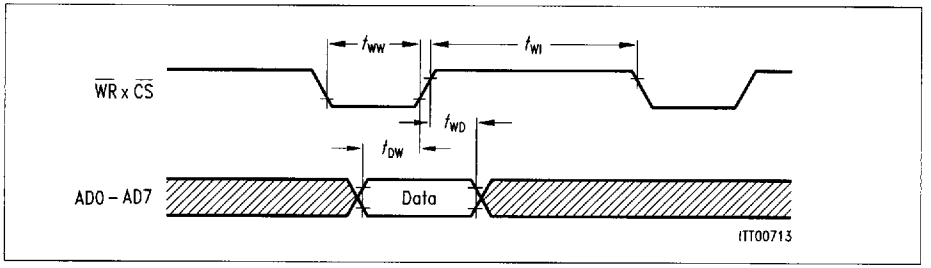


Figure 60
Microprocessor Write Cycle

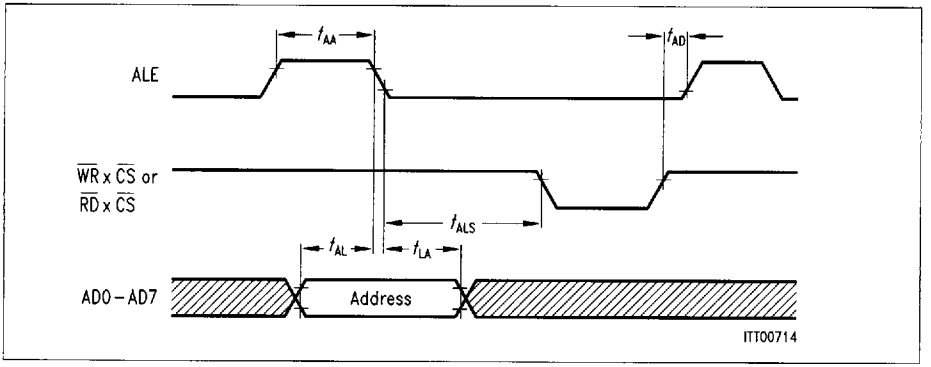


Figure 61
Multiplexed Address Timing

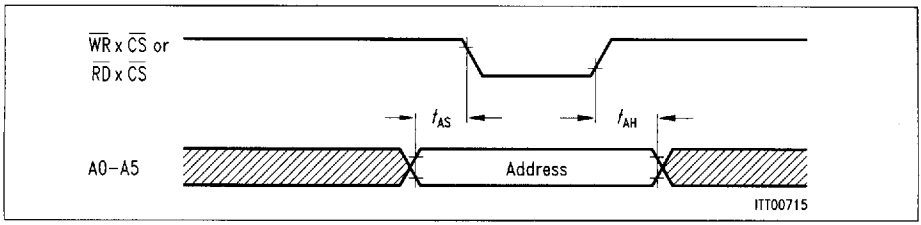


Figure 62
Non-Multiplexed Address Timing

Motorola Bus Mode

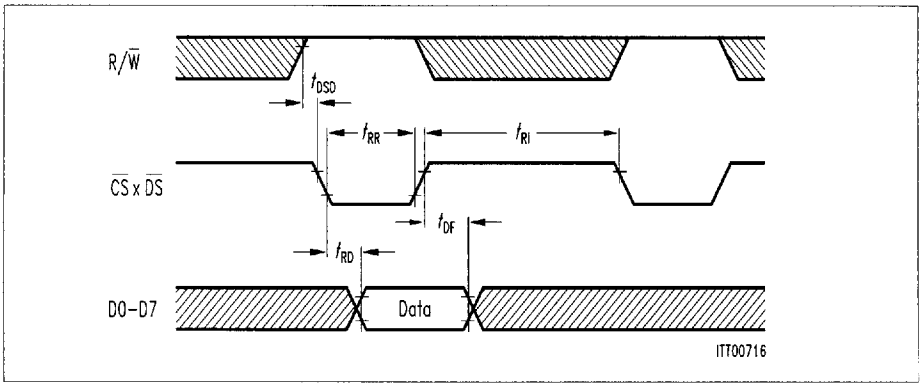


Figure 63
Microprocessor Read Timing

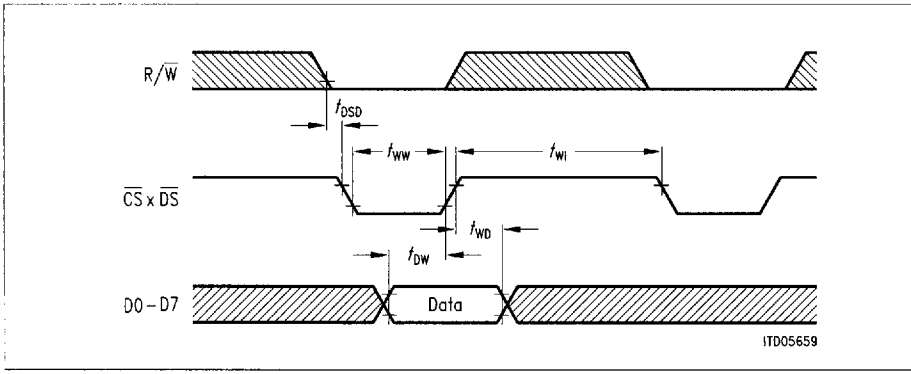


Figure 64
Microprocessor Write Cycle

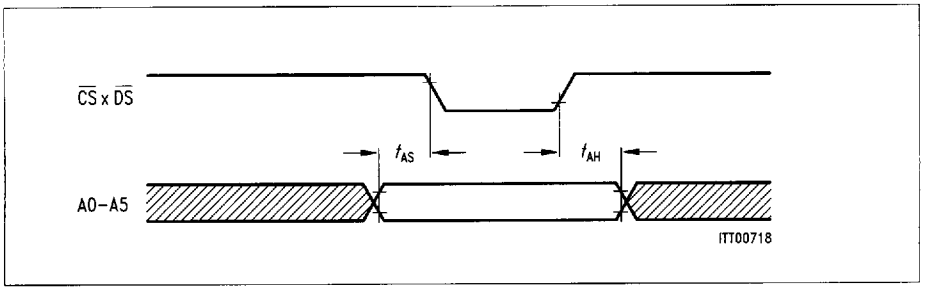


Figure 65
Non-Multiplexed Address Timing

Microprocessor Interface Timing

Parameter	Symbol	Limit Values		Unit
		min.	max.	
ALE pulse width	t_{AA}	50		ns
Address setup time to ALE	t_{AL}	15		ns
Address hold time from ALE	t_{LA}	10		ns
Address latch setup time to $\overline{WR}$, $\overline{RD}$	t_{ALS}	0		ns
Address setup time	t_{AS}	25		ns
Address hold time	t_{AH}	10		ns
ALE guard time	t_{AD}	15		ns
$\overline{DS}$ delay after $\overline{RW}$ setup	t_{DSD}	0		ns
$\overline{RD}$ pulse width	t_{RR}	110		ns
Data output delay from $\overline{RD}$	t_{RD}		110	ns
Data float from $\overline{RD}$	t_{DF}		25	ns
$\overline{RD}$ control interval	t_{RI}	70		ns
$\overline{W}$ pulse width	t_{WW}	60		ns
Data setup time to $\overline{W}$ x $\overline{CS}$	t_{DW}	35		ns
Data hold time from $\overline{W}$ x $\overline{CS}$	t_{WD}	10		ns
$\overline{W}$ control interval	t_{WI}	70		ns

Serial Interface Timing

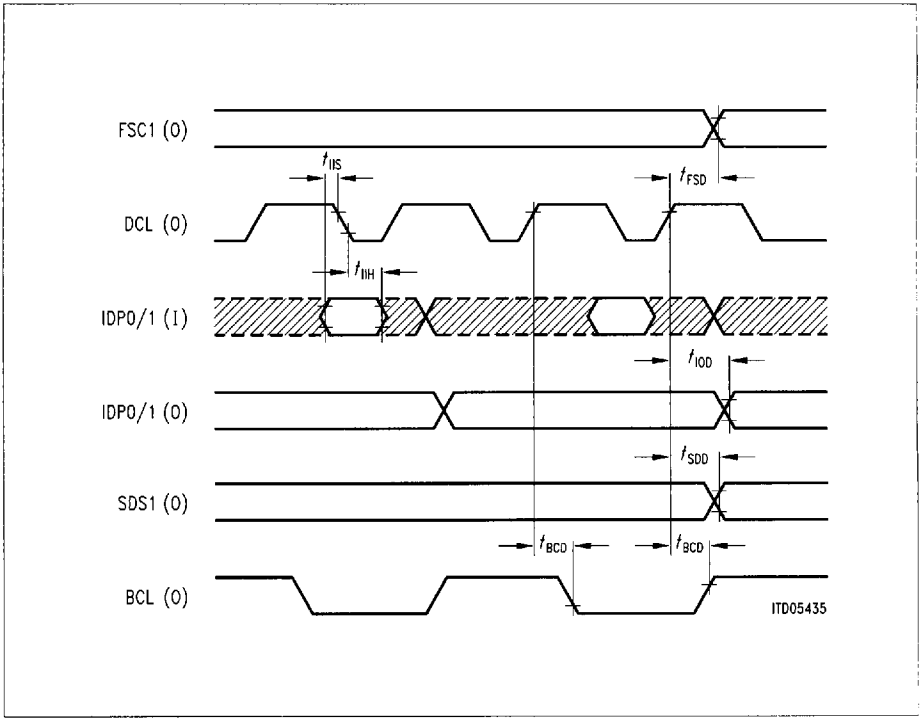


Figure 66
IOM® Timing (TE mode)

IOM® Timing

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
IOM output data delay	t_{IOD}	20	100	ns	IOM-2
IOM input data setup	t_{IIS}	20		ns	IOM-2
IOM input data hold	t_{IIH}	20		ns	
FSC1 strobe delay	t_{FSD}	– 20	20	ns	
Strobe signal delay	t_{SDD}		120	ns	
Bit clock delay	t_{BCD}	– 20	20	ns	

HDLC Mode (ADF2: IMS = 0, ADF1: TEM = 1, MODE: DIM2 – 0 = 101 – 111)

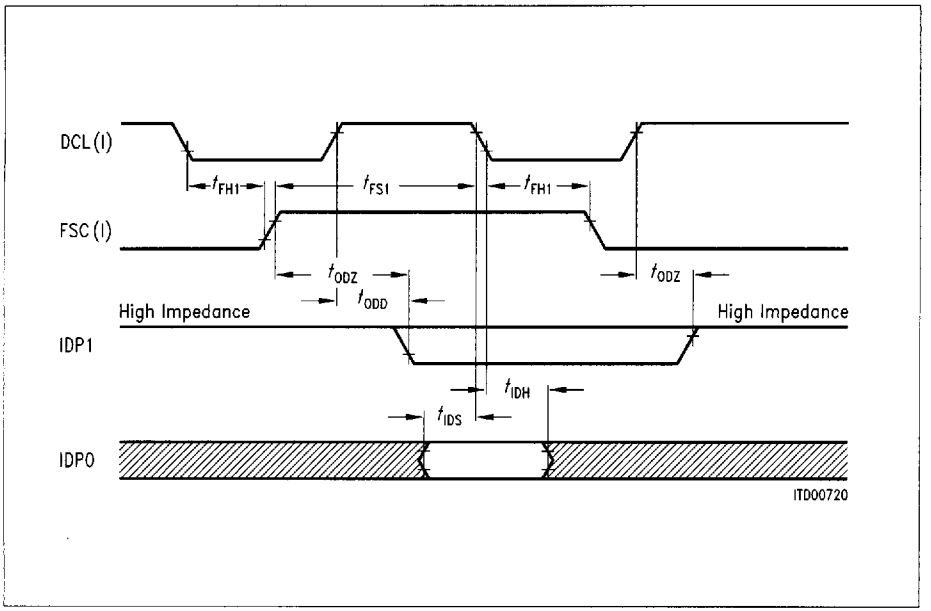


Figure 67
FSC1 (strobe) Characteristics

HDLC Mode Timing

Parameter	Symbol	Limit Values		Unit
		min.	max.	
FSC1 set-up time	t_{FS1}	100		ns
FSC1 hold time	t_{FH1}	30		ns
Output data from high impedance to active	t_{OZD}		80	ns
Output data from active to high impedance	t_{ODZ}		40	ns
Output data delay from DCL	t_{ODD}	20	100	ns
Input data setup	t_{IS}	10		ns
Input data hold	t_{DH}	30		ns

Clock Timing

The clocks are summarized in **table 20**, with the respective duty ratios.

Table 20
ISAC®-S TE Clock Signals (IOM®-2 mode)

Application	DCL	FSC1	BCL	SDS1
TE	o:1536 kHz* 3:2	o:8 kHz* 1:2	o:768 kHz* 1:1	o:8 kHz 1:11 2:10

The 1536-kHz clock is phase-locked to the receive S signal, and derived using the internal DPLL and the 7.68 MHz ± 100 ppm crystal.

A phase tracking with respect to "S" is performed once in 250 µs. As a consequence of this DPLL tracking, the "high" state of the 1536-kHz clock may be either reduced or extended by one 7.68-MHz period (duty ratio 2:2 or 4:2 instead of 3:2) once every 250 µs. Since the other signals are derived from this clock, the "high" or "low" states may likewise be reduced or extended by the same amount once every 250 µs.

The phase relationships of the clocks are shown in **figure 69.**

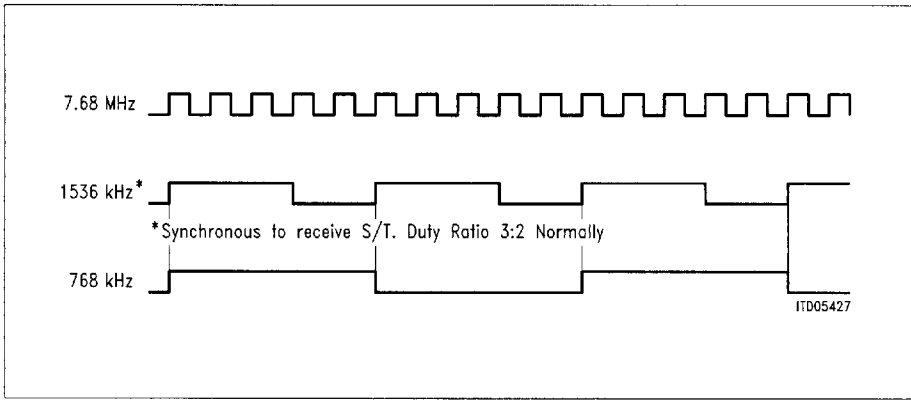


Figure 68
Phase Relationships of ISAC®-S TE Clock Signals

*) Synchronous to receive "S" line

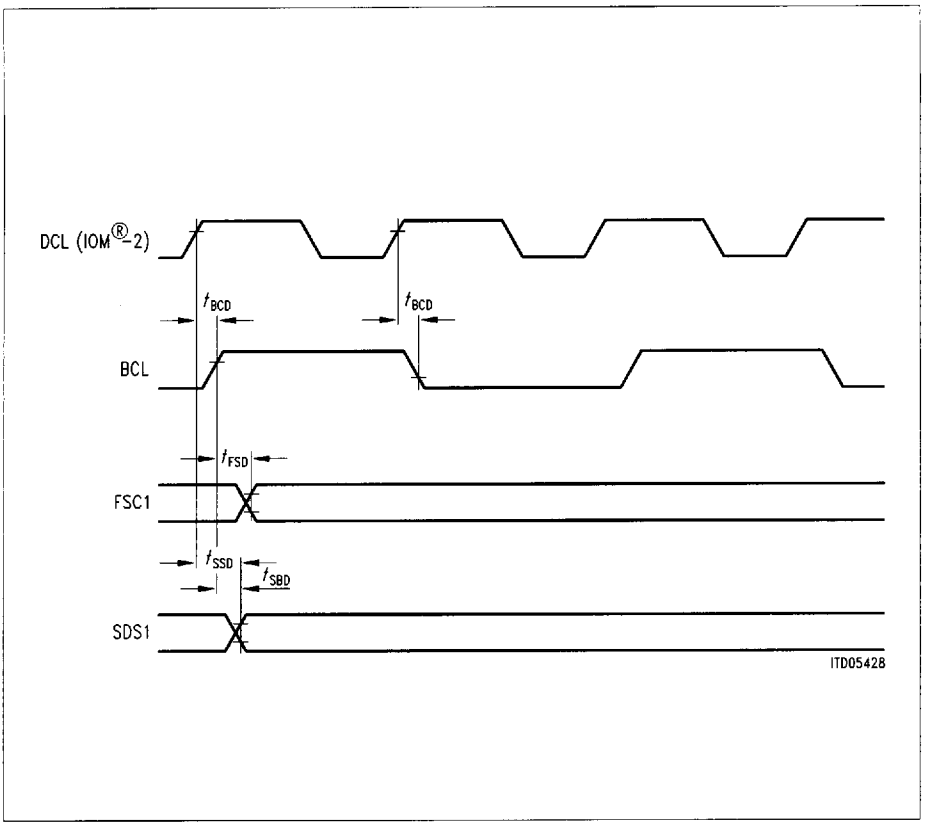


Figure 69
Timing Relationships between ISAC®-S TE Clock Signals

Table 21

Parameter	Symbol	Limit Values		Unit	Condition
		min.	max.		
Bit clock delay	t_{BCD}	– 20	20	ns	IOM-2
SDS1 delay from DCL	t_{SDD}		120	ns	IOM-2
SDS1 delay from BCL	t_{SBD}		120	ns	IOM-2

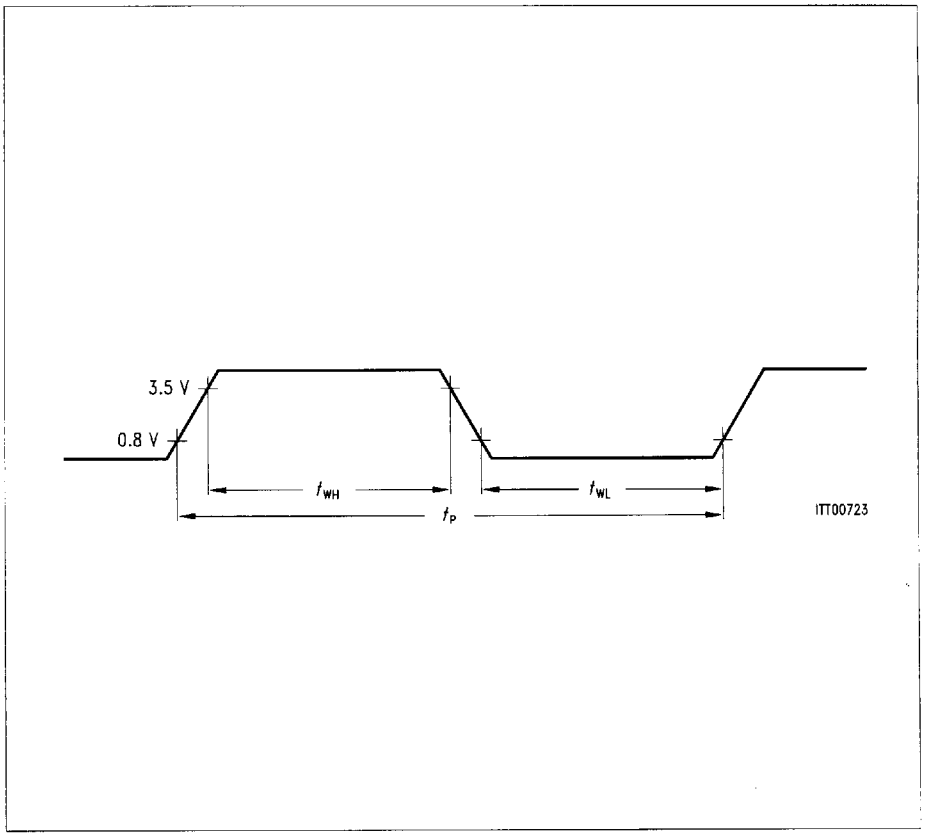


Figure 70
Definition of Clock Period and Width

Table 22
DCL-Clock Characteristics (IOM®-2)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
(TE) 1536 kHz	t_{PO}	520	651	782	ns	osc ± 100 ppm
	t_{WHO}	240	391	541	ns	osc ± 100 ppm
	t_{WLO}	240	260	281	ns	osc ± 100 ppm

Jitter

In TE mode, the timing extraction jitter of the ISAC-S conforms to CCITT Recommendation I.430 (– 7 % to + 7 % of the S-interface bit period).

Description of the Receive PLL (RPLL) of the ISAC-S TE

The receive PLL performs phase tracking each 250 µs after detecting the phase between the F/L transition of the receive signal and the recovered clock. Phase adjustment is done by adding or subtracting 130 ns to or form a 1.536-MHz clock cycle. The 1.536-MHz clock is than used to generate any other clock synchronized to the line.

During (re)synchronization an internal reset condition may effect the 1.536-MHz clock to have high or low times as short as 130 ns. After the S/T-interface frame has achieved the synchronized state (after three consecutive valid pairs of code violations) the FSC output is set to a specific phase relationship, thus causing once an irregular FSC timing.

Reset

Table 23
Reset Signal Characteristics

Parameter	Symbol	Limit Values	Unit	Test Condition
		min.		
Length of active high state	t_{RST}	4	ms	Power-on/Power-Down to Power-Up (Standby)
		2 x DCL clock cycles		During Power-Up (Standby)

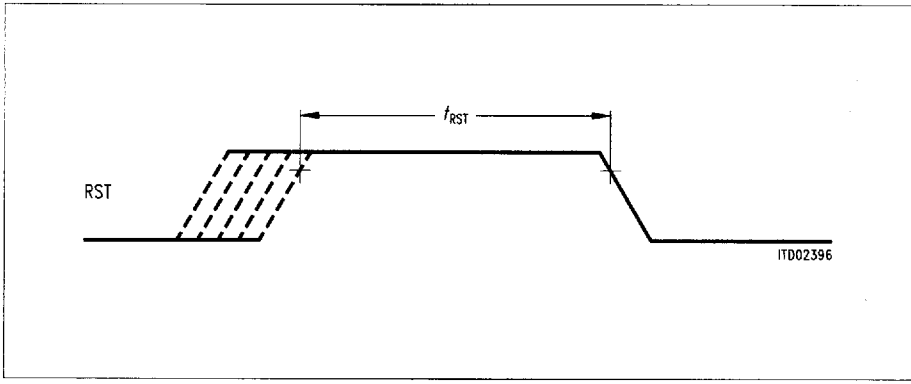
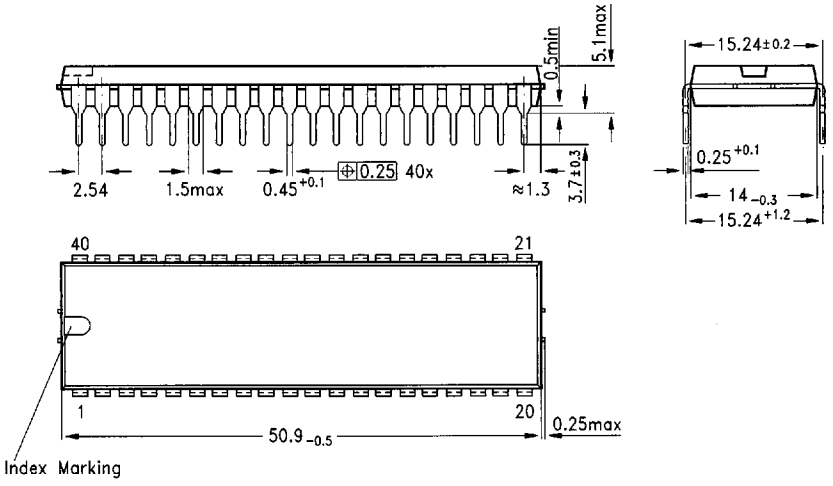


Figure 71
Reset

7 Package Outlines

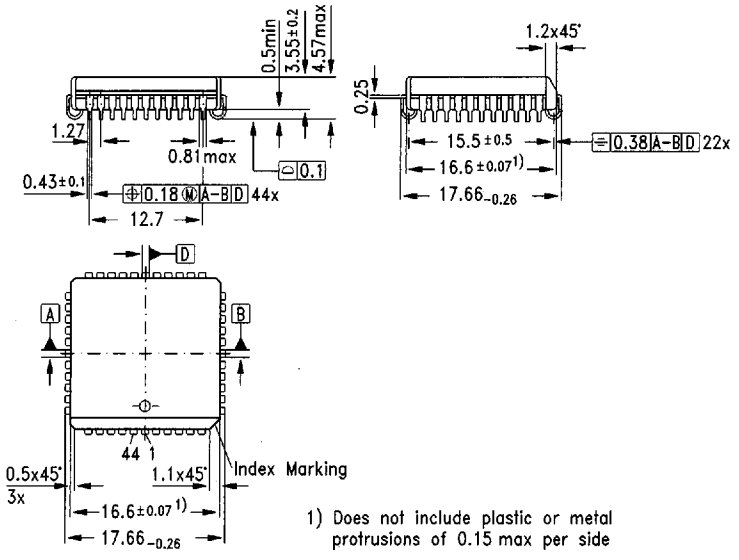
Plastic Package, P-DIP-40-2
(Plastic Dual-In-Line Package)



GPD05055

Dimensions in mm

Plastic Package, P-LCC-44-1 (SMD)
(Plastic-Leaded Chip Carrier)

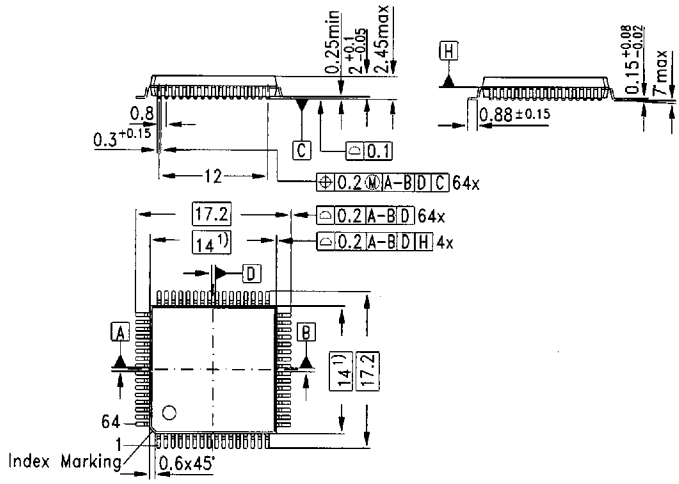


1) Does not include plastic or metal protrusions of 0.15 max per side

GPL05102

Dimensions in mm

Plastic Package, P-MQFP-64-1 (SMD)
(Plastic Metric Quad Flat Package)



1) Does not include plastic or metal protrusions of 0.25 max per side

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book "Package Information"

SMD = Surface Mounted Device

Dimensions in mm