PaceMips™ PR4300SC, PR4300MC 3.3V CPUs THIRD GENERATION RISC PROCESSORS

ADVANCE INFORMATION

T-49-17-38

NOTICE
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2

COMMON FEATURES

- Low-power 64-bit superpipelined third generation RISC μPs
  - Highly integrated CPU with integer unit, FPA, MMU, I & D cache
  - Balanced integer & floating point performance
  - Exploits 2-level instruction-level parallelism
  - No issue restrictions on the instructions used
- 3.3V operation
- Integer unit:
  - 32 entry 64-bit wide register file
  - ALU
  - Dedicated Multiplier/Divider
- Fully binary compatible with PR3000A/PR3010A, PR3400, PIMM, and PIPER
- On-chip 8KBytes of Instruction cache & 8KBytes of Data cache with parity protection
- Fully binary compatible with PR3000A/PR3010A, PR3400, PIMM, and PIPER
- Memory Management Unit
  - 96 entry TLB for fast virtual-to-physical mapping
  - Programmable page sizes: 4KBytes to 16MBytes
  - Total physical memory space of 64GBytes
- Superpipelined FPA
  - 32/16 entry 32/64 bit register file in a 32-bit mode
  - 32 entry 64-bit register file in 64-bit mode
  - Supports single & double precision
  - Conforms to ANSI/ IEEE Standard 754-1985
- 128KBytes to 4MBytes of secondary cache
- Comprehensive system development support
- Very high system performance
- Produced with PACE III™ 3.3V Technology
- Package: 447-pin Ceramic Pin Grid Array

PR4000MC FEATURES

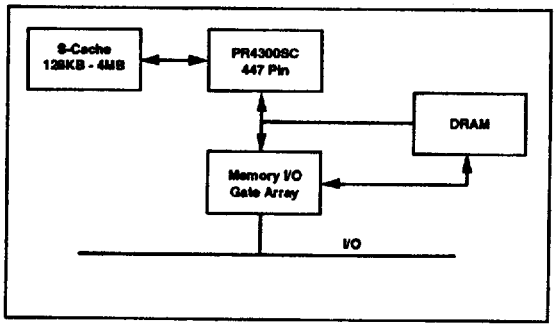
- Configurable multiprocessor cache coherency protocols
- Power dissipation: 8.89W @ 75MHz

1.0 INTRODUCTION

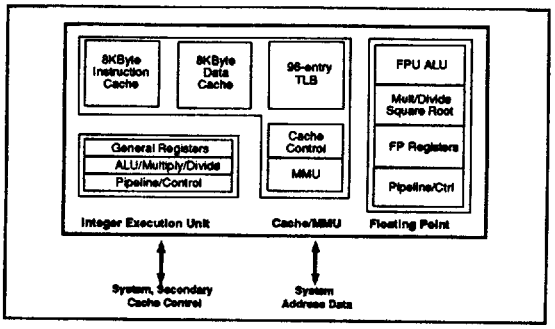
PaceMips PR4300SC and PR4300MC are third generation 64-bit superpipelined 3.3V RISC processors designed for extremely high-performance applications. High-level integration including MMU, FPA, 8KBytes of instruction cache, 8KBytes of data cache, and secondary cache support, coupled with PACE III Technology, delivers the highest possible performance among current RISC microprocessors. These processors are fully binary compatible with the PR3000A. The availability of superpipelined FPA on-chip allows them to provide balanced integer and floating point performance (both single- and double-precision) that is critical to a wide range of applications.

The 8 KBytes each of I & D caches are direct mapped, 64-bit -wide with selectable refill sizes of 4 or 8 words. Byte parity protection is provided in both the caches. Write back scheme is followed for the data cache. The MMU is comprised of 96 entry TLB mapping onto 96 physical pages. The MMU registers are managed by software allowing programmable page sizes from 4KBytes to 16MBytes in 4KByte mulitiples. Each entry in TLB has 8 bits of process indentifier to distinguish virtual addresses of 256 different tasks.

PR4300SC SYSTEM BLOCK DIAGRAM



PR4300SC/PR4300MC BLOCK DIAGRAM



PR4000SC and PR4000MC achieve their highest performance by exploiting 2-level instruction-level parallelism with no issue restrictions. Besides being downward binary compatible with PR3000A, these processors also executes additional instructions that include double loads/stores to the floating point unit, branches with conditional execution of delay slot, single and double precision square root computations, conversions from floating point to integer with specific rounding mode, and conditional traps.

Both PR4000SC and PR4000MC support secondary caches ranging from 128 KBytes to 4MBytes made from standard SRAMs. The PR4000MC also supports configurable multiprocessor cache coherency protocols.

The PaceMips PR4000SC and PR4000MC Microprocessors are available in a 447-lead Ceramic Pin Grid Array package.

2.0 CPU Overview

2.1 Superpipelined Implementation

PR4000SC and PR4000MC are third generation RISC microprocessors designed by MIPS. They implement an 8-stage superpipeline which places no restrictions on instruction issue. Any two instructions can be issued each cycle under normal circumstances. The internal pipeline of these processors operate at a frequency twice that of the external clock frequency. The 8-stage superpipeline of these processors are made possible by pipelining cache accesses, shortening register access times, implementing virtually indexed primary caches, and allowing the latency of functional units to span multiple pipeline cycles.
The operation of the internal pipeline is shown in Figure 2.1.

The execution of a single PR4000SC or PR4000MC CPU instruction consists of the following eight primary steps:

IF Instruction fetch First half. Virtual address is presented to the I-cache and TLB.

IS Instruction fetch Second half. The I-cache outputs the instruction and the TLB generates the physical address.

RF Register File. Three activities occur in parallel:
- instruction is decoded and a check is made for interlock conditions,
- instruction tag check is made to determine if there is a cache hit or not,
- operands are fetched from the register file.

EX Instruction EXecute. One of three activities can occur:
- if the instruction is a register-to-register operation, an arithmetic, logical, shift, multiply, or divide operation is performed;
- if the instruction is a load and store, the data virtual address is calculated;
- if the instruction is a branch, the branch target virtual address is calculated and branch conditions are checked.

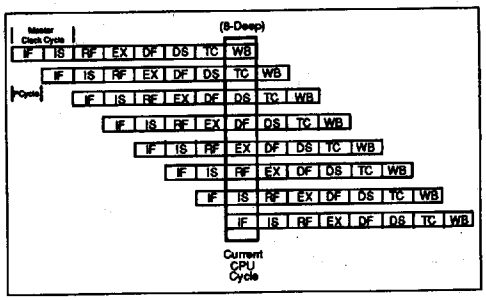


Figure 2.1 Internal Pipeline Operation

DF Data cache First half. A virtual address is presented to the D-cache and TLB.

DS Data cache Second half. The D-cache outputs the instruction and the TLB generates the physical address.

TC Tag Check. A tag check is performed for loads and stores to determine if there is a hit or not.

WB Write Back. The instruction result is written back to the register file.

These processors can be programmed to operate either as 32-bit or a 64-bit microprocessors. When set to operate as a 32-bit microprocessor, they generate 32-bit virtual addresses, and perform 32-bit operations on the contents of the general registers. When operating as a 64-bit microprocessor, they generate 64-bit virtual addresses, and perform 64-bit operations. The PR4000SC and PR4000MC implement MIPS' Instruction Set Architecture III. All instructions in either mode are 32 bits wide.

2.2 Integer Unit

The PR4000SC and PR4000MC integer processing units contain a 32-entry register file, an ALU, and a dedicated multiplier/divider. The integer unit is the core processing unit in these processors and is responsible for instruction fetching, integer operation decoding and execution, and load and store operation execution.

The PR4000SC and PR4000MC have thirty-two general purpose registers either 32 or 64-bits wide depending on operating mode. These registers are used for scalar integer operations and address calculation. The 32 general registers are all equivalent with two exceptions: r0 is hardwired to a zero value, and r31 is the link register for the JUMP AND LINK instruction. r0 maintains a value of zero when used as a source register under all conditions. When used as a target, the result is discarded. The register file consists of two read ports and one write port, and uses bypassing to enable the reading and writing of the same register twice per cycle, which minimizes the operation latency in the pipeline.

The PR4000SC and PR4000MC ALU consist of the integer adder and logic unit. The adder performs address calculations

in addition to arithmetic operations, and the logic unit performs all shift operations. Each of these units is highly optimized and can perform an operation in a single superpipeline cycle. The integer multiplier and divider units perform 32-bit and 64-bit signed and unsigned multiply and divide operations and execute instructions in parallel with the ALU. The results of the operation are placed in the MDHI and MDLO registers. The values can then be transferred to the general purpose register file using the Mfhi/Mflo instructions.

2.3 Floating Point Unit

The PR4000SC and PR4000MC incorporate an entire floating-point unit on chip, including a floating-point register file and an execution unit that supports single and double-precision arithmetic, as specified in the IEEE standard 754. The execution unit is broken into separate multiply, divide, and add/convert/square root units, which allows for overlapped operations. The adder is pipelined, allowing a new add to begin every 4 cycles.

The floating-point register file is made up of sixteen 64-bit registers which can also be configured as thirty-two 32-bit floating-point registers. The floating-point control registers contain a register for determining configuration and revision information for the coprocessor and control and status information. Besides being fully binary compatible with MIPS ISA I, the floating point unit also implements single and double-precision square root, explicitly rounded conversions, and load and store doubleword instructions. Relative to the R3010, the latency (in nanoseconds) of floating-point multiply and divide has been improved by about 25 percent through the use of additional hardware, better process technology, and improved circuit design.

2.4 PR4000SC and PR4000MC Primary Caches

Both incorporate on-chip instruction and data caches. Each cache has its own 64-bit data path that can be accessed twice an external cycle, so the instruction and data caches can be accessed in parallel with full pipelining. Combining this feature with a pipelined access of each cache in a single external cycle, the cache subsystem provides the integer and floating-point units with an aggregate bandwidth of 1.6 GBytes per second at a master clock frequency of 50 MHz. The primary caches are virtually indexed and physically tagged. Using a part of the virtual index to address the cache enables the virtual address translation to happen in parallel with the primary cache lookup. The physically tagged cache implies that the cache need not be flushed on context switches.

These processors incorporate a direct-mapped on-chip instruction cache of 8 KBytes in size and is protected with byte parity. The tag holds a 24-bit physical address and a valid bit, and is parity protected. The instruction cache can be refilled or accessed twice per external cycle. Although the PR4000PC fetches one 64-bit unit per pipeline, only one 32-bit instruction is issued per pipeline cycle for a peak instruction bandwidth of 400 MBytes per second. The line size can be configured as four or eight words to allow different applications to have a line size that delivers optimum performance.

The processors include a direct mapped 8 KByte on-chip data cache. The data cache is protected with byte parity and its tag is protected with a single parity bit. The D-Cache line size can be configured as four or eight words. The write policy is writeback, which means that a Store to a cache line does not immediately cause memory to be updated. This technique increases system performance by reducing bus traffic and eliminating the bottleneck of waiting for each Store operation to finish before issuing a subsequent memory operation.

A store buffer is associated with the D-Cache. When the PR4000SC/MC executes a Store instruction, this 2-entry buffer gets written with the store data while the tag comparison is performed. If the tag matches, then the data gets written into the D-Cache in the next pipeline cycle that the D-Cache is unaccessed. The store buffer allows the PR4000SC/MC to execute two stores per master clock cycle and to perform back-to-back stores without penalty. PR4000SC/MC can also perform two loads or a load and store per master clock cycle without penalty, yielding 800 MBytes per second bandwidth without restrictions on instruction combinations.

2.5 System Control Coprocessor

The system control coprocessor (CP0) translates virtual addresses into physical addresses, manages exceptions, and handles the transitions between kernel and user states. CP0 also controls the cache subsystem and provides diagnostic control and error recovery facilities. A generic system timer is provided for interval timing, time keeping, process accounting, and time slicing.

2.5.1 System Control Coprocessor Register File

The system control coprocessor (CP0) registers provide the path through which the virtual memory system's page mapping is examined and changed, the operating modes (kernel vs. user mode, interrupts enabled or disabled, cache features) controlled, and exceptions handled. In addition, the PR4000SC/MC include registers to implement a real-time cycle counting facility, to address reference traps for debugging, to aid in cache diagnostic testing, and to assist in data error detection and correction.

The on-chip memory management unit controls the virtual memory system's page mapping, the operating modes, and exception handling. It consists of an instruction translation lookaside buffer (ITLB), a joint TLB, and a coprocessor register file.

2.5.2 Joint TLB

For fast virtual-to-physical instruction and data address translation, the processors use a 96-entry translation lookaside buffer. This fully associative TLB is arranged in 48 even-odd page pairs. The TLB maps a 32bit virtual address and an 8-bit address space identifier into a 36bit physical address to access 64 GBytes of physical memory.

The page size can be configured, on a per-entry basis, to equal 4 KBytes to 16 MBytes in increments of powers of four. The large page size allows the TLB to map up to 1.6 GBytes

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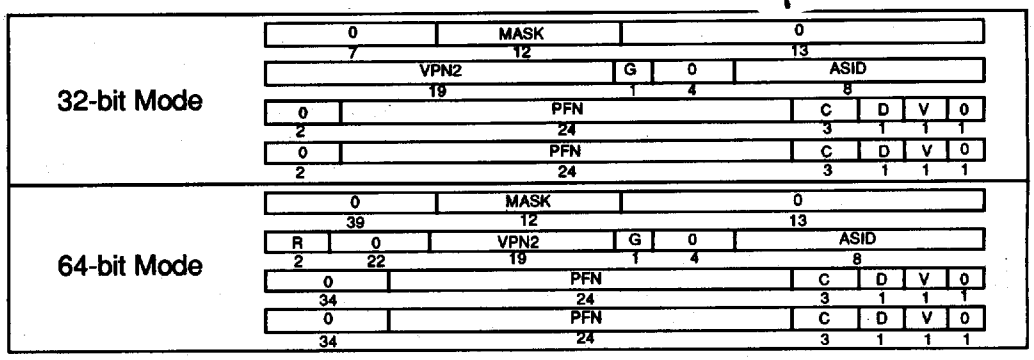

where:

MASK	is the comparison mask.	V	if set, entry is Valid.
VPN2	is the Virtual Page Number / 2.	G	if set, page is Global (ignore ASID in match logic).
ASID	is the Address Space Identifier.	0	Reserved. Must be written as zeros; returns 0 on reads.
PFN	is the Page Frame Number.	R	is the Region (00 user, 01 supervisor, 11 (kernel) used to match Virtual address bits 63 and 62.
C	is the Cache algorithm for the page.		
D	if set, page is Dirty.		

Figure 2.2 Format of a TLB Entry

of memory at any one time. The second feature is extremely important in systems where a deterministic response time to an interrupt is necessary. Each entry in the TLB can be "locked" to guarantee that translations remains in the buffer.

2.5.3 TLB Structure

Mapped virtual addresses are translated into physical addresses using an on-chip, fully-associative translation lookaside buffer (TLB). The TLB contains translations for 48 even-odd pairs of pages, each of which map pages ranging from 4 KBytes to 16 MBytes in size. The page size is controlled on a per-pair basis by a page mask.

2.5.4 Instruction TLB

PR4000SC and PR4000MC also incorporate a 2-entry instruction TLB. Each entry maps a 4 KByte page. The instruction TLB improves performance by allowing instruction address translation to occur in parallel with data address translation.

When a miss occurs on an instruction address translation, the ITLB is filled from the JTLB. The operation of the ITLB is invisible to the user.

Both processors provide three modes of virtual addressing: User mode, Kernal mode, and Supervisior mode. These three modes are available to system software to provide a secure environment for user processes. Bits in a status register determine which virtual addressing mode is used and whether the 32-bit or 64-bit addressing model is used. Table 2.1 shows the available virtual address space in the three modes of virtual addressing.

Table 2.1 Virtual Address Space

	KERNEL MODE	USER MODE	SUPERVISOR MODE
32-Bit	2 GBYTES	4 GBYTES	2.5 GBYTES
64-Bit	1 TERABYTE	3 TERABYTES	2 TERABYTES

2.6 Instruction Set

PR4000SC and PR4000MC implement the extended MIPS Instruction Set Architecture (MIPS ISA III) which improves performance and adds functional capabilities while maintaining complete applications binary compatibility with earlier MIPS microprocessors. The extensions result in better code density, greater multiprocessing support, improved performance for commonly used code sequences in operating system kernels, and faster execution of floating-point intensive applications. Every instruction is 32-bits wide to allow easy and fast decode. Figure 2.3 shows the three instruction formats.

When operating as a 32-bit microprocessor, the PR4000SC/MC take an exception on those instructions that take advantage of the 64-bit architecture.

2.6.1 Load and Store Instructions

Load and Store instructions move data between memory and general registers. Only one addressing mode is specified: base register plus a signed 16-bit immediate offset. Bytes, halfwords, and words may be loaded to and stored from general registers by specifying aligned addresses. Unaligned memory references are efficiently supported by two pairs of load and store instructions.

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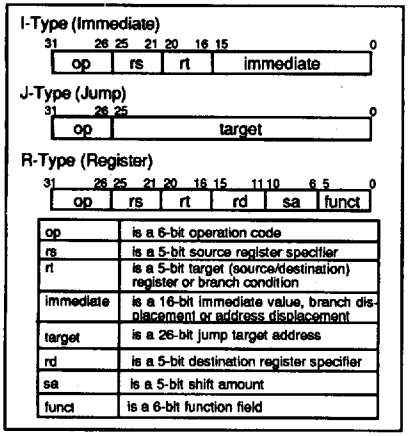

op	is a 6-bit operation code
rs	is a 5-bit source register specifier
rt	is a 5-bit target (source/destination) register or branch condition
immediate	is a 16-bit immediate value, branch displacement or address displacement
target	is a 26-bit jump target address
rd	is a 5-bit destination register specifier
sa	is a 5-bit shift amount
funct	is a 6-bit function field

Figure 2.3 Instruction Set Formats

The PR4000SC/MC implementation allows the instruction immediately following a load to use the contents of the register loaded. In such cases, the hardware interlocks until the load is completed. This mechanism reduces code size in the cases where the compiler is unable to schedule a useful instruction between a load and the use of the value loaded. It is still desirable to separate a load instruction from the instruction that uses the register loaded, but not required for correct functionality.

2.6.2 Computational Instructions

Computational instructions perform arithmetic, logical, and shift operations on values in registers.

2.6.3 Jump and Branch Instructions

All Jump and Branch instructions have an architectural delay of exactly one instruction to reduce the pipeline branch penalty. However, the PR4000SC/MC implementation of the architecture has a three-cycle branch delay. RISC compilers manage the instruction scheduling such that the delay slot is occupied by a real instruction (instead of a nop) in most instances of Jump and Branch instructions.

Jump instructions provide an unconditional transfer of flow during program execution. Branch instructions provide a mechanism to branch based on the outcome of a specified test. An extensive set of such tests allows the efficient compilation of high-level languages. In addition, there is a variant of the branch instructions in which the instruction in the delay slot is nullified if the branch is not taken.

2.6.4 Exception Instructions

Exception instructions cause a trap to be executed. The trap causes a branch to the general exception handling vector.

2.6.5 Coprocessor Instructions

Coprocessor instructions perform operations in special-purpose hardware blocks called coprocessors.

2.6.6 Synchronization Instructions

There are two instructions that support synchronization between processes executing on the same processor or on different processors: Load Linked and Store Conditional. The Load Linked instruction, in addition to doing a simple load, sets a state bit called the link bit. The link bit forms a breakable link between the load linked instruction and a subsequent Store Conditional instruction. The Store Conditional instructions performs a simple store if, and only if, the link bit is set when the store is executed. If the link bit is not set, then the store will fail to execute. The success or failure of the Store Conditional instructions is indicated in the target register of the store.

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2..7 Data Formats

Integer operations are performed on 32-bit or 64-bit unsigned and signed (two's complement) data. Floating-point operations are performed on data in the single-precision and double-precision floating-point formats. Loads and stores are performed on 8-bit, 16-bit, 32-bit, and 64-bit operands. The MIPS Instruction Set Architecture defines an 8-bit byte, a 16-bit halfword, a 32-bit word, and a 64-bit doubleword. The byte ordering is user configurable into either big-endian or little-endian byte ordering.

2.8 Clocking/Frequency

Both processors base all clocking methodology on a single clock input. This clock is then multiplied by two using internal phase lock loop techniques in order to get the internal pipeline operating frequency. The phase lock loops also eliminate skew in all clocks used and generated by the PR4000PC. This internal clock is then divided to generate two system interface clocks, RClock and TClock. The frequency of these clocks is programmable and can be set to be either half, one third, or one fourth the processor internal clock frequency. This feature makes it easier to interface to memory and I/O systems of various frequencies.

2.9 System Interface

The PR4000PC supports a 64-bit system interface that can be used to construct systems as simple as a uniprocessor with a direct DRAM interface and no secondary cache or as sophisticated as a fully cache coherent multiprocessor. The interface consists of a 64-bit Address/Data bus with 8 check bits and a 9-bit command bus protected with parity. In addition, there are 8 handshake signals. The interface has a simple timing specification and is capable of transferring data between the processor and memory at a peak rate of 400 MBytes/second at 50 MHz. The interface signals are shown in Figure 2.4.

2.9.1Secondary Cache Interface

The R4000SC and R4000MC support a secondary cache that can range in size from 128 KBytes to 4 MBytes. The cache can be configured as a unified cache or split into an instruction cache and a data cache, and it can be designed using industry standard SRAMs. The R4000 provides all of the secondary cache control circuitry on chip, including ECC.

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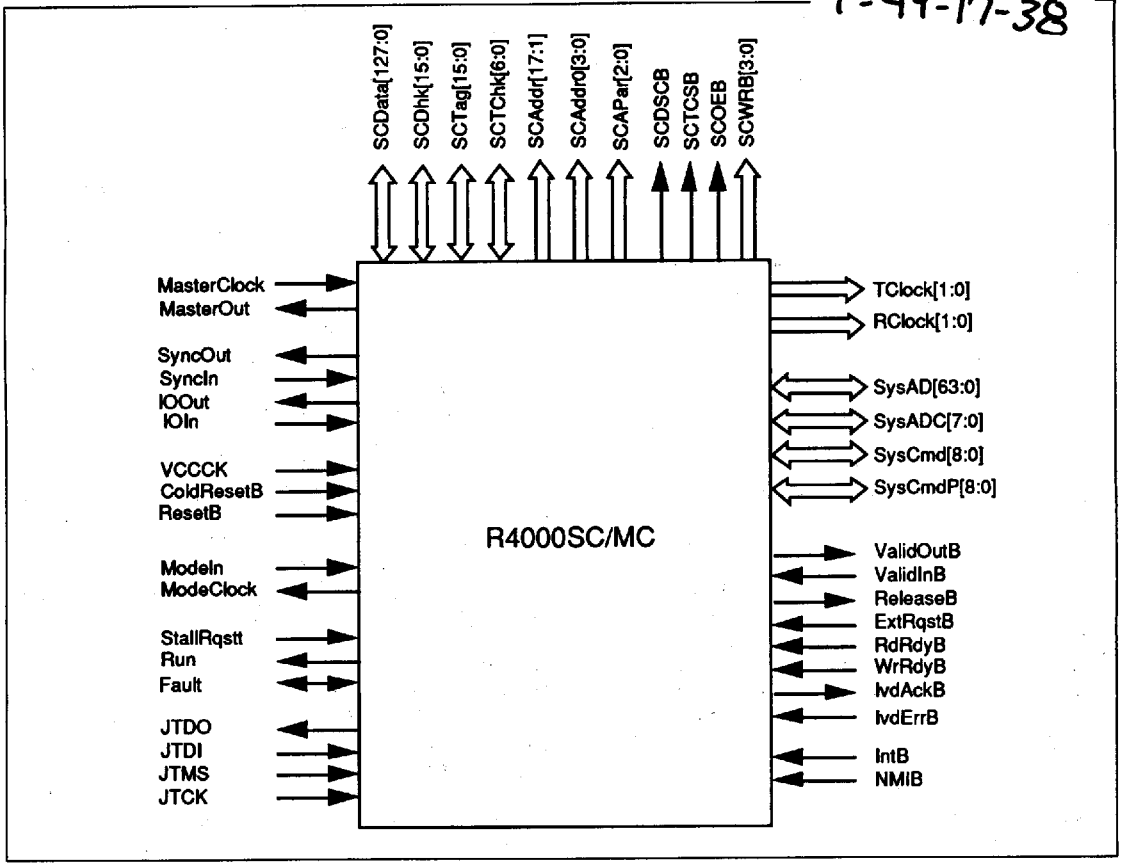

Figure 2.4 PR4000SC/MC Symbolic Pinout

The secondary cache interface consists of a 128-bit data bus, a 25-bit tag bus, an 18-bit address bus, and SRAM control signals. The wide data bus improves performance by providing a high bandwidth data path to fill the primary caches. ECC check bits are added to both the data and tag buses to improve data integrity. All double-bit errors can be detected and all single bit errors can be corrected on both buses.

The secondary cache access time is configurable, providing system designers with the flexibility to tailor the cache design to specific applications. The line size of the secondary cache is also configurable and can be 4, 8, 16, or 32 words. The line size of the primary cache must always be less than or equal to the line size of the secondary cache which is physically tagged and physically indexed. The physical cache prevents problems that could arise due to virtual address aliasing. Also, a physical cache makes multiprocessing cache coherency protocols easier to implement. The R4000MC provides a set of cache states and a mechanism for manipulating the contents and state of the cache, which are sufficient to implement a variety of cache coherency protocols, using either bus snooping or directory-based schemes.

2.10 Support for Multiprocessing

The PR4000MC implements sophisticated caches capable of supporting a number of cache coherence schemes, and synchronization primitives for the efficient implementation of tightly-coupled multiprocessor systems. In the PR4000MC, cache coherence is maintained by hardware. The system control coprocessor permits the specification of different caching protocols on a per-page basis.

A page may be:

- Uncached.
- Cached but non-coherent.
- Cached and coherent exclusive (only one copy of the data in any one cache on loads and stores).
- Cached and coherent exclusive on writes (write invalidate scheme–only one copy of the data in any one cache when that datum is written to).
- Cached and coherent with updates on writes (write-update scheme).

Depending upon the amount and type of data sharing in an application, the operating system can choose the most appropriate caching strategy. Support for processor

T-49-17-38

synchronization is provided by Load Linked and Store Conditional instructions which have the following features:

1. They provide a simple mechanism for generating all of the common synchronization primitives including test-and-set, bit-level locks, semaphores, counters, sequencers, etc. with no additional hardware overhead.

2. They operate in such a fashion that bus traffic is only generated when the state of the cache line changes.

3. They need not lock a system bus—a very important feature for larger systems.

2.11 System Address/Data Bus

The 64-bit System Address Data (SysAD) bus is used to transfer addresses and data between the processors and the rest of the system. It is protected with an 8-bit check bus, SysADC. The check bits can be configured as either parity or ECC, for flexibility in interfacing to either parity or ECC memory systems.

The data rate and bus frequency at which the processors transmit data to the system interface are programmable via boot time mode control bits. Also, the rate at which the processor receives data is fully controlled by the external device. Therefore, either a low-cost interface requiring no write buffering or a fast, high-performance interface can be designed to communicate with these processors.

The PR4000SC and PR4000MC interface have a 9-bit System Command (SysCmd) bus, which indicates whether the SysAD bus carries an address or data. If the SysAD carries an address, then the SysCmd bus also indicates what type of transaction is to take place (for example, a read or write). The SysCmd bus is bidirectional to support both processor requests and external requests to PR4000SC/MC.

These processors support byte, halfword, tribyte, word, doubleword, and block transfers on the SysAD bus. For a sub-doubleword transfer, the low-order 3 address bits gives the byte address of the transfer, and the SysCmd bus indicates the number of bytes being transferred.

2.12 Handshake Signals

There are eight handshake signals on the system interface. Two, RdRdy* and WrRdy*, are used by an external device to indicate to the PR4000SC/MC whether it can accept a new read or write transaction. The PR4000SC/MC samples these signals before deasserting the address on read and write requests.

ExtRqst* and Release* are used to transfer control of the SysAD and SysCmd buses between the processor and an external device. When an external device needs to control the interface, it asserts ExtRqst*. The PR4000SC/MC responds by asserting Release* to release the system interface to slave state. ValidOut* and ValidIn* are used by the PR4000SC/MC and the external device respectively to indicate that there is a valid command or data on SysAD and SysCmd buses. The PR4000SC/MC asserts ValidOut* when it is driving these buses with a valid command or data, and the external device drives ValidIn* when it has control of the buses and is driving a valid command or data.

2.13 PR4000SC/MC Requests

The PR4000SC/MC are capable of issuing requests to a memory and I/O subsystem through non-overlap and overlap modes of operation.

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Non-Overlap Mode

This means that only one processor request may be outstanding at a time and that the request must be serviced by an external device before the PR4000SC/MC issues another request. The PR4000SC/MC can issue read and write requests to an external device, and an external device can issue read and write requests to the PR4000SC/MC.

Figure 2.5 shows a processor read request. The PR4000SC/MC asserts ValidOut* and simultaneously drives the address and read command on the SysAD and SysCmd buses. If the system interface has RdRdy* asserted, then the processor tristates its drivers and releases the system interface to slave state by asserting Release*. The external device can then begin sending the data to the PR4000SC/MC. Figure 2.6 shows a processor write request.

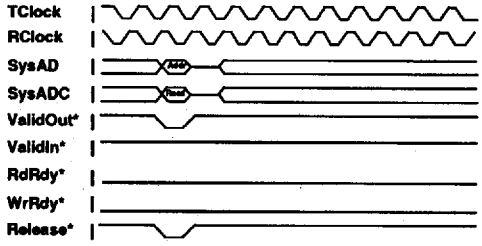


Figure 2.5 Processor Read Request

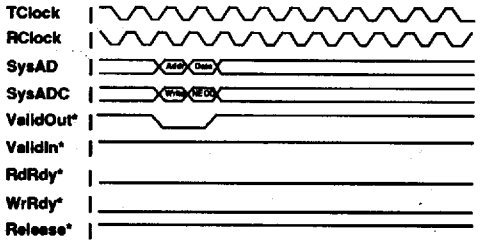


Figure 2.6 Processor Write Request

Overlap Mode

The R4000SC and R4000MC, when configured with a secondary cache, must operate in overlap mode in which they may issue multiple system interface transactions in parallel. The processor may issue a combination of a read

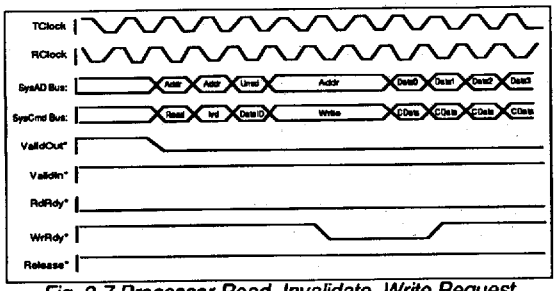


Fig. 2-7 Processor Read, Invalidate, Write Request

request, an update or invalidate request, and a write request. For instance, when a dirty cache line needs to be replaced, the processor issues a read request immediately followed by a write request, without waiting for the read data to return. This has the advantage of "hiding" the write transaction between the read request and read response, thus increasing overall system performance. Overlap mode is not necessary or useful in the R4000PC since the processor contains a write buffer capable of accepting an entire primary cache line of data. Figure 2-7 illustrates a processor request in overlap mode. This request is made up of a read, invalidate, and write request. Note that the protocol for the read, the invalidate, and the write are all similar to each other, with the exception that the processor also sends out valid data during the write request. In Figure 2-7 the processor write transaction not only occurs before the read response from the external device, but it also illustrates how an external device can hold off a write request through the deassertion of WrRdy*.

2.14 External Requests

The PR4000SC/MC responds to requests issued by an external device. The requests can take several forms. An external device may need to supply data in response to an PR4000SC/MC read request or it may need to gain control over the system interface bus to access other resources which may be on that bus. It also may issue cache coherency requests to the processor, such as a request for the PR4000SC/MC to update, invalidate, or snoop upon its caches, or to supply a cache line of data. Additionally, an external device may need to write to the PR4000SC/MC interrupt register.

The following is a list of the supported external requests:Read,Write,Invalidate,Update,Snoop,Intervention,Null. Figure 2-8 shows an example of an external snoop request. The process by which the external device issues the request is very similar to the way theP R4000SC/MC issues a request. The external device first gains ownership of the system interface by asserting ExtRqst* and waiting for the R4000 to assert Release*. The external device then sends in a valid command by asserting ValidIn* and driving the SysCmd and SysAD buses with the snoop command and address. The PR4000SC/MC responds to the request by asserting ValidOut* and driving the SysCmd bus with the cache state of the snooped upon line.

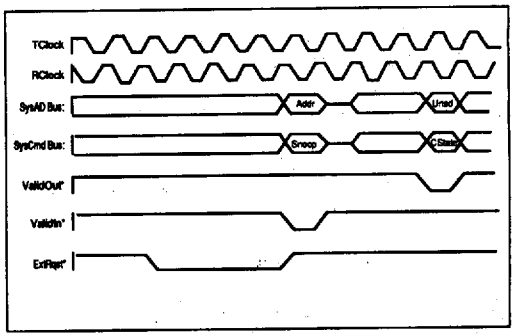


Fig. 2-8 External Snoop Request

2.15 Interrupts

The PR4000SC/MC processors supports six hardware interrupts and two software interrupts. The six hardware interrupts are accessible via an external write request in both the configurations.

2.16 JTAG Boundary Scan

The PR4000SC/MC implements JTAG boundary scan, which is intended to provide a capability for testing the interconnect between the PR4000SC/MC processor, the printed circuit board, and the other components on the board. In addition, the mechanism is intended to provide a means to test the secondary cache RAM. In accordance with the JTAG specification, the PR4000SC/MC contains a TAP controller, JTAG instruction registers, JTAG boundary scan register, JTAG identification register, and JTAG bypass register.

2.17 Boot Time Mode Control

PR4000SC/MC fundamental operational modes are initialized viaboot time mode control interface. This serial interface operates at a very low frequency (1/64th of the input clock frequency), which allows the initialization information to be kept in a low-cost EPROM. Upon reset, PR4000SC/MC reads serial PROM to access configuration information.

2.18 Resets

The PR4000SC/MC processosr uses a multi-level reset sequence that allows the implementation of a power-on reset, cold reset, and warm reset. Upon power on and cold reset, all processor internal state machines reset, and the PR4000SC/MC begins fetching instructions from hex address BFC00000, which is in uncached, unmapped space. During a warm reset, however, processor internal state is preserved.

T-49-17-38

2

2.19Fault Tolerant Support

Two PR4000SC/MCs can be connected together to form a self-checking pair. In this mode, each PR4000SC/MC checks the other and a difference is indicated with the assertion of a fault signal.

2.20 Debugging Support

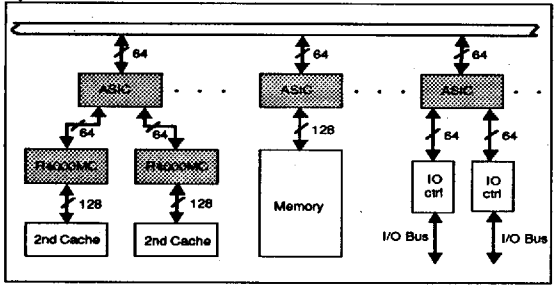
The coprocessor Watch Register allows the setting of data break points, which cause traps when either a load or store instruction is executed to a specified physical address. Also, instruction breakpoints can be set by using the Breakpoint instruction. Development of Cache and TLB diagnostic software is facilitated by PR4000SC/MC instructions that allow the reading and writing of any location in the cache and TLB.

2.21 Software Development Tools

MIPS offers a number of programs, utilities, and tools designed for the system programmer which aid in the development of operating systems and stand-alone software for machines based on the MIPS R4000. These tools are valid for PR4000SC and PR4000MC also. Among the software tools are a cache simulator, which allows the user to model the cache and memory hierarchy; an instruction set simulator, which allows the user to debug stand-alone programs; and tools and utilities that allow the user to program PROMS for a test system, download stand-alone programs from a development system to the test system, and initiate program execution and debugging.

2.22 PR4000MC System

Tightly coupled multiprocessor systems can be built with PR4000MCs following either snooping or directory-based cache coherence schemes. Figure 2-8 shows a high-end system.



T-49-17-38

3.0 System Interface

These signals comprise the interface between the PR4000PC and other components in the system.

ExtRqst*:	**I**	**External request** **Input** An external agent asserts ExtRqst* to request use of the system interface. The PR4000PC grants the request by asserting Release*.
Release*:	**O**	**Release interface** **Output** In response to the assertion of ExtRqst*, the PR4000PC asserts Release* to signal the requesting device that the system interface is available.
RdRdy*:	**I**	**Read ready** **Input** The external agent asserts RdRdy* to indicate that it can accept processor read, invalidate, or update requests in both overlap and non-overlap mode or can accept a read followed by a potential invalidate or update request in overlap mode.
SysAD(63:0):	**I/O**	**System address/data bus** **Input/Output** A 64-bit address and data bus for communication between the processor and an external agent.
SysADC(7:0):	**I/O**	**System address/data check bus** **Input/Output** An 8-bit bus containing check bits for the SysAD bus.
SysCmd(8:0):	**I/O**	**System command/data identifier bus parity** **Input/Output** A 9-bit bus for command and data identifier transmission between the processor and an external agent.
SysCmdP:	**I/O**	**System command/data identifier bus parity** **Input/Output** A single, even-parity bit for the SysCmd bus.
ValidIn*:	**I**	**Valid input** **Input** An external agent asserts ValidIn* when it is driving a valid address or data on the SysAD bus and a valid command or data identifier on the SysCmd bus.
ValidOut*:	**O**	**Valid output** **Output** The PR4000PC asserts ValidOut* when it is driving a valid address or data on the SysAD bus and a valid command or data identifier on the SysCmd bus.
WrRdy*:	**I**	**Write ready** **Input** An external agent asserts WrRdy* when it can accept a processor write request.

Clock/Control Interface

These signals comprise the interface for clocking and maintenance functions.

IOOut:	**O**	**I/O output** **Output** Output slew rate control feedback loop output. Must be connected to IOIn through a delay loop that models the IO path from the PR4000PC to an external agent.
IOIn:	**I**	**I/O input** **Input** Output slew rate control feedback loop input (see IOOut).
MasterClock:	**I**	**Master clock** **Input** Master clock input establishes the processor operating frequency.
MasterOut:	**O**	**Master clock out** **Output** Master clock output aligned with MasterClock.

T-49-17-38

RClock(1:0):	**O**	**Receive clocks** **Output** Two identical receive clocks that establish the system interface frequency.
SyncOut:	**O**	**Synchronization clock out** **Output** Synchronization clock output. Must be connected to SyncIn through an interconnect that models the interconnect between MasterOut, TClock, RClock, and the external agent.
SyncIn:	**I**	**Synchronization clock in** **Input** Synchronization clock input.
TClock(1:0):	**O**	**Transmit clocks** **Output** Two identical transmit clocks that establish the system interface frequency.
GrpRun*:	**O**	**Group run** **Output** The PR4000PC pulses GrpRun* after completing a group of instructions.
GrpStall*:	**I**	**Group stall** **Input** An external agent asserts GrpStall* to stall the processor after completion of the current group of instructions.
Fault*:	**O**	**Fault** **Output** The PR4000PC asserts Fault* to indicate a mismatch output of boundary comparators.
Status(7:0):	**O**	**Status** **Output** An 8-bit bus that indicates the current operation status of the processor.
VccP:	**I**	**Quiet VCC for PLL** **Input** Quiet Vcc for the internal phase locked loop.
VccSense:	**I/O**	**VCC sense** **Input/Output** This is a special pin used only in component testing and characterization. It provides a separate, direct

Secondary Cache Interface

These signals comprise the interface between the R4000 and the secondary cache and are available only on the R4000MC and SC.

SCAddr(17:1):	**O**	**Secondary cache address bus** **Output**
SCAddr0W:	**O**	**Secondary cache address lsb** **Output**
SCAddr0X:	**O**	**Secondary cache address lsb** **Output**
SCAddr0Y:	**O**	**Secondary cache address lsb** **Output**
SCAddr0Z:	**O**	**Secondary cache address lsb** **Output** The 18-bit address bus for the secondary cache. Bits 17 through 1 are bidirectional. Bit 0 has four output lines to provide additional drive current.
SCAPar(2:0):	**O**	**Secondary cache address parity bus** **Output** A 3-bit bus that carries the parity of the SCAddr bus and the cache control lines SCOE*, SCWR*, SCDCS* and SCTCS*.
SCData(127:0):	**I/O**	**Secondary cache data bus** **Input/Output** A 128-bit bus used to read or write cache data from and to the secondary cache data RAM.
SCDChk(15:0):	**I/O**	**Secondary cache data ECC bus** **Input/Output** A 16-bit bus that carries two Error Checking and Correcting (ECC) fields covering the upper or lower 64 bits of the SCData from and to the secondary cache.

T-49-17-38

SCDCS*:	**O**	**Secondary cache data chip select** **Output** Chip select enable signal for the secondary cache data RAM.
SCOE*:	**O**	**Secondary cache output enable** **Output** Output enable for the secondary cache data and tag RAM.
SCTag(24:0):	**I/O**	**Secondary cache tag bus** **Input/Output** A 25-bit bus used to read or write cache tags from and to the secondary cache.
SCTChk(6:0):	**I/O**	**Secondary cache tag ECC bus** **Input/Output** A 7-bit bus that carries an Error Checking and Correcting (ECC) field covering the SCTag from and to the secondary cache.
SCTCS*:	**O**	**Secondary cache data chip select** **Output** Chip select enable signal for the secondary cache tag RAM.
SCWrW*:	**O**	**Secondary cache write enable** **Output**
SCWrX*:	**O**	**Secondary cache write enable** **Output**
SCWrY*:	**O**	**Secondary cache write enable** **Output**
SCWrZ*:	**O**	**Secondary cache write enable** **Output** Write enable for the secondary cache data and tag RAM.

T-49-17-38

Interrupt Interface

These signals comprise the interface used by external agents to interrupt the PR4000PC processor.

Int*(5:1):	**I**	**Interrupt** **Input** Five of six general processor interrupts, bit-wise ORed with bits 5:1 of the interrupt register.
Int*(0):	**I**	**Interrupt** **Input** One of six general processor interrupts, bit-wise ORed with bit 0 of the interrupt register.
NMI*:I		**Non-maskable interrupt** **Input** Non-maskable interrupt, ORed with bit 6 of the interrupt register.

Initialization Interface

These signals comprise the interface by which an external agent initializes the PR4000PC operating parameters.

ColdReset*:	**I**	**Cold reset** **Input** This signal must be asserted for a power on reset or a cold reset. The clocks SClock, TClock, and RClock begin to cycle and are synchronized with the de-assertion edge of ColdReset*. ColdReset* must be de-asserted synchronously with MasterOut.
ModeClock:	**O**	**Boot mode clock** **Output** Serial boot-mode data clock output at the system clock frequency divided by two hundred and fifty six.
ModeIn:	**I**	**Boot mode data in** **Input** Serial boot-mode data input.
Reset*:	**I**	**Reset** **Input** This signal must be asserted for any reset sequence. It may be asserted synchronously or asynchronously for a cold reset, or synchronously to initiate a warm reset. Reset* must be de-asserted synchronously with MasterOut.
VCCOk:	**I**	**VCC is OK** **Input** When asserted, this signal indicates to the PR4000PC that the +5 volt power supply has been above 4.75 volts for more than 100 milliseconds and will remain stable. The assertion of VCCOk initiates the initialization sequence.

JTAG Interface

These signals comprise the interface by which the JTAG boundary scan mechanism is provided.

JTDI:	**I**	**JTAG data in** **Input** Data is serially scanned in through this pin.
JTCK:	**I**	**JTAG clock input** **Input** The R4000 outputs a serial clock on JTCK. On the rising edge of JTCK both JTDI and JTMS are sampled.
TDO:	**O**	**JTAG data out** **Output** Data is serially scanned out through this pin.
JTMS:	**I**	**JTAG command** **Input** JTAG command signal, signals that the incoming serial data is command data.

T-49-17-38

4.0 Timing Diagrams

Figure 4.1 MasterClock

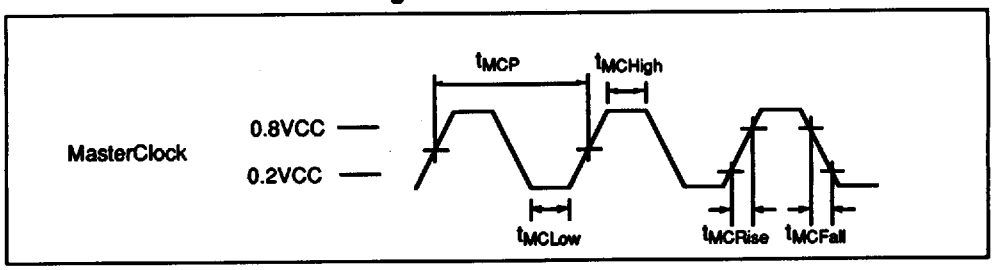
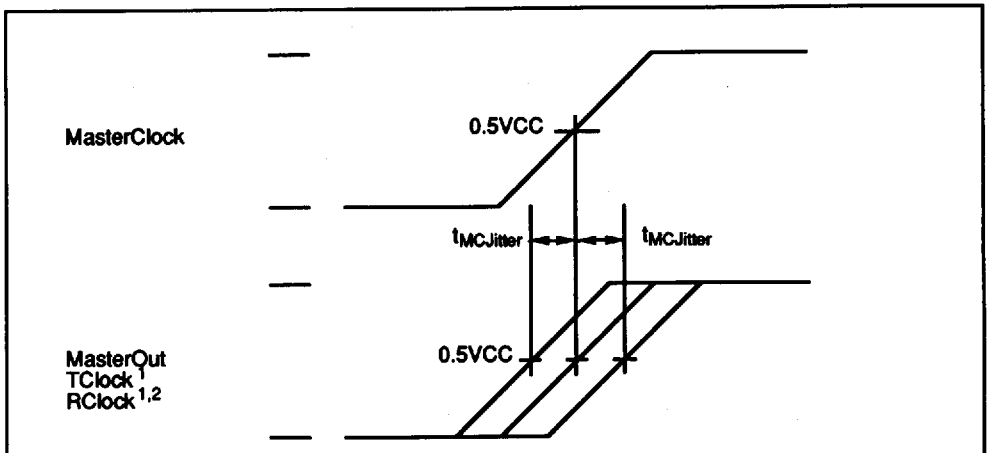


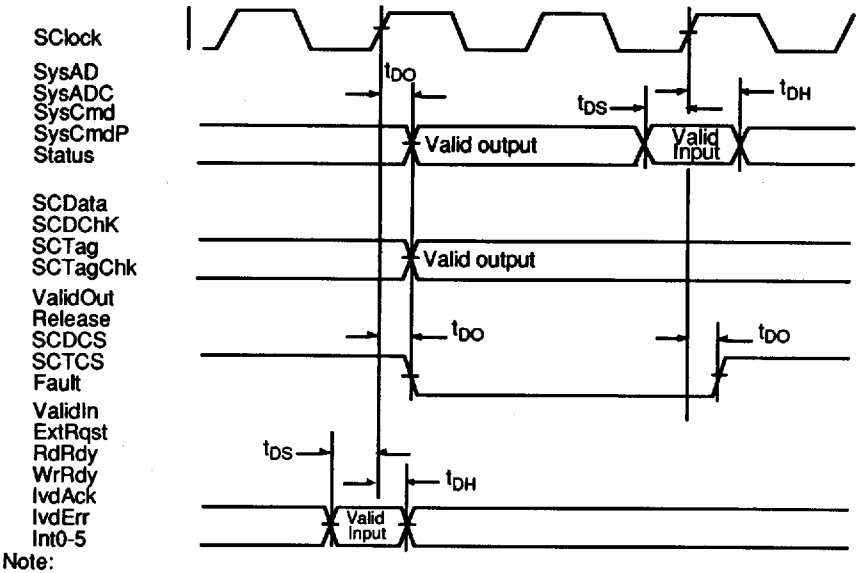
Figure 4.2 Clock Jitter



(1) With SyncOut shorted to SyncIn by the shortest path, the 50% point of TClock lines up with the 50% point of MasterClock.
(2) RClock leads TClock by 90°.
(3) The SyncIn/SyncOut path, TClock and RClock must have the same capacitive loading to match the MasterClock edges.

T-49-17-38

Figure 4.3 Processor Clock, PClock to SClock Divisor of 2



Note:

These waveforms only describe edge to edge timing relationships. Functional descriptions are contained in previous chapters.

T-49-17-38

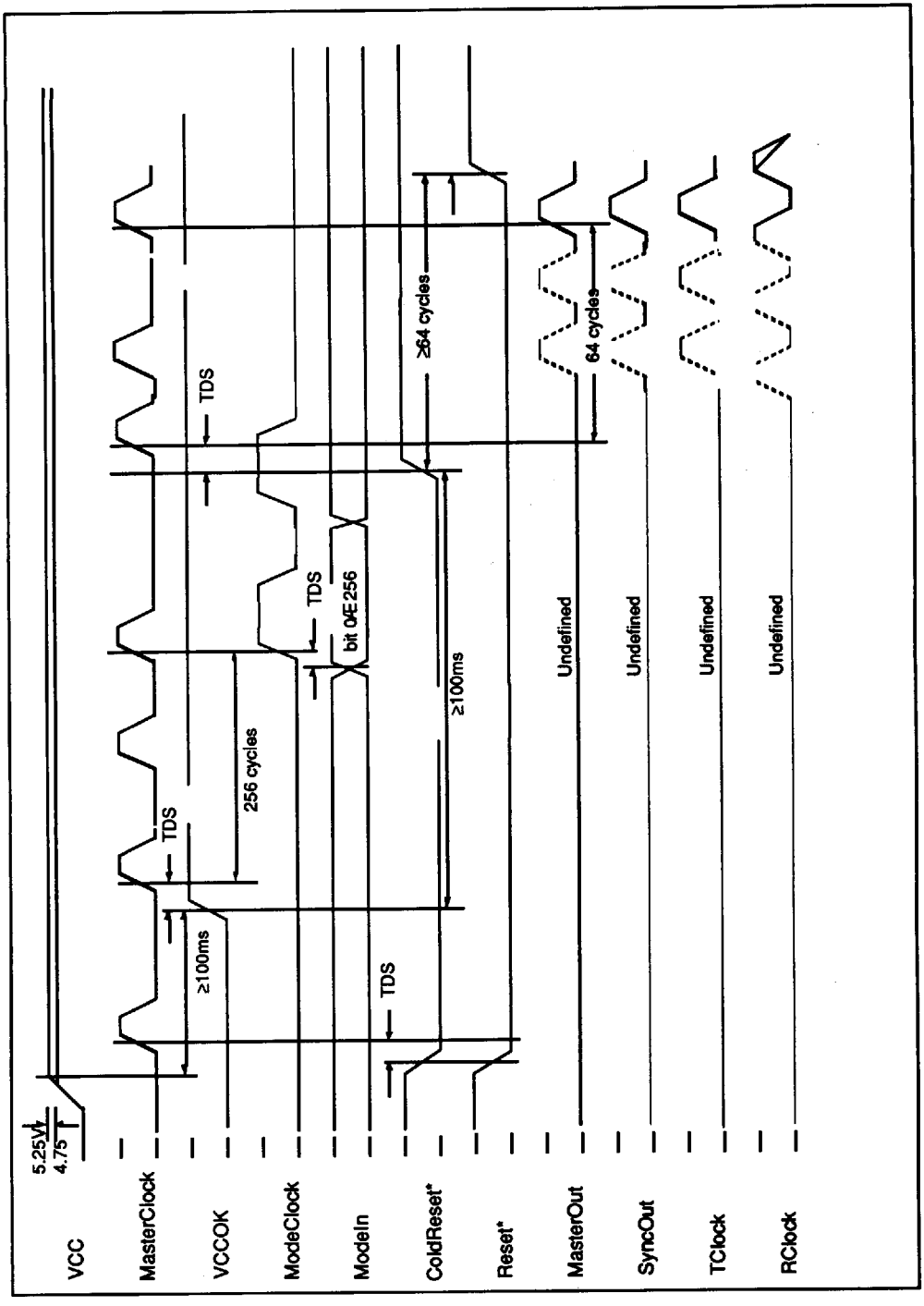
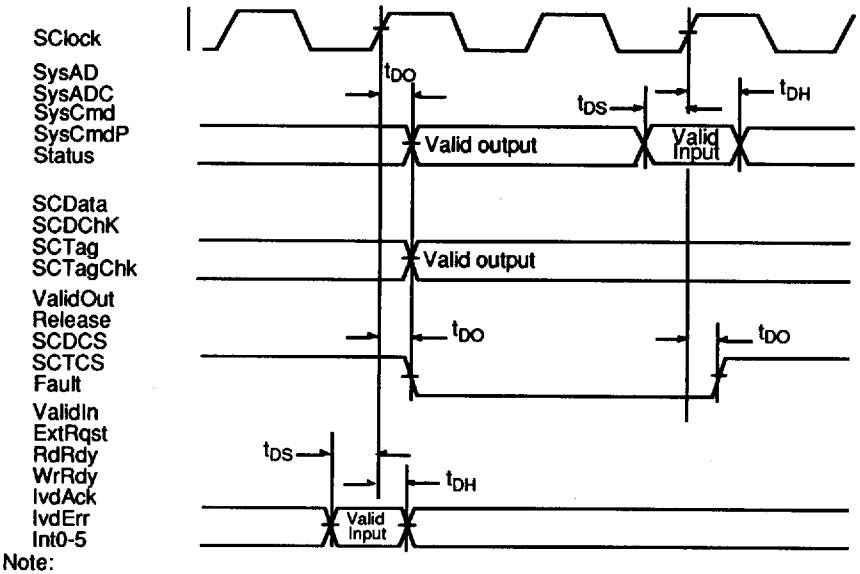


Figure 4.8 Power-On Reset or Cold Reset

T-49-17-38

Figure 4.3 Processor Clock, PClock to SClock Divisor of 2



Note:

These waveforms only describe edge to edge timing relationships. Functional descriptions are contained in previous chapters.

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T-49-17-38

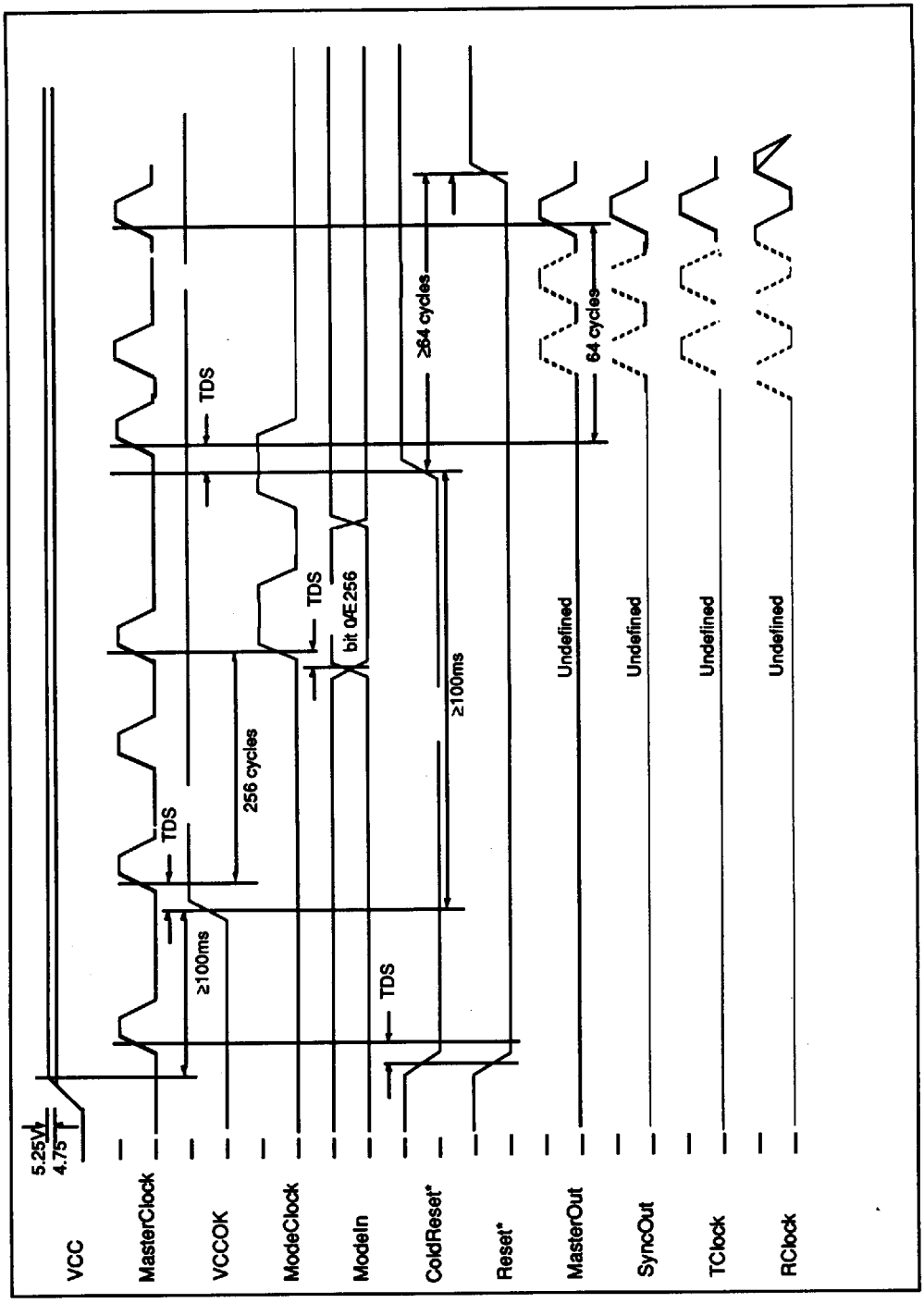


Figure 4.8 Power-On Reset or Cold Reset

8.0 PR4000SC/MC Processor Signal Summary

T-49-17-38

Description	Name	I/O	Asserted State	3-State
Secondary cache data bus	SCData(127:0)	I/O	High	Yes
Secondary cache data ECC bus	SCDChk(15:0)	I/O	High	Yes
Secondary cache tag bus	SCTag(24:0)	I/O	High	Yes
Secondary cache tag ecc bus	SCTChk(6:0)	I/O	High	Yes
Secondary cache address bus	SCAddr(17:1)	O	High	No
Secondary cache address lsb	SCAddr0Z	O	High	No
Secondary cache address lsb	SCAddr0X	O	High	No
Secondary cache address lsb	SCAddr0X	O	High	No
Secondary cache address lsb	SCAddr0W	O	High	No
Secondary cache address parity bus	SCAPar(2:0)	O	High	No
Secondary cache output enable	SCOE*	O	Low	No
Secondary cache write enable	SCWrZ*	O	Low	No
Secondary cache write enable	SCWrY*	O	Low	No
Secondary cache write enable	SCWrX*	O	Low	No
Secondary cache write enable	SCWrW*	O	Low	No
Secondary cache data chip select	SCDCS*	O	Low	No
Secondary cache data chip select	SCTCS*	O	Low	No
System address/data bus	SysAD(63:0)	I/O	High	Yes
System address/data check bus	SysADC(7:0)	I/O	High	Yes
System command/data identifier bus parity	SysCmd(8:0)	I/O	High	Yes
System command/data identifier bus parity	SysCmdP	I/O	High	Yes
Valid input	ValidIn*	I	Low	No
Valid output	ValidOut*	O	Low	Yes
External request	ExtRqst*	O	Low	No
Release interface	Release*	O	Low	No
Read ready	RdRdy*	I	Low	No
Write ready	WrRdy*	I	Low	No
Invalidate acknowledge	IvdAck*	I	Low	No
Invalidate error	IvdErr*	I	Low	No
Interrupt	Int*(0)	I	Low	No

2

T-49-17-38

8.0 PR4000SC/MC Processor Signal Summary (continued)

Description	Name	I/O	Asserted State	3-State
Transmit clocks	TClock(1:0)	O	High	No
Receive clocks	RClock(1:0)	O	High	No
Master clock	MasterClock	I	High	No
Master clock out	MasterOut	O	High	No
Synchronization clock out	SyncOut	O	High	No
Synchronization clock in	SyncIn	I	High	No
I/O output	IOOut	O	High	No
I/O input	IOIn	I	High	No
VCC is OK	VCCOk	I	High	No
Cold reset	ColdReset*	I	Low	No
Reset	Reset*	I	Low	No
Group run	GrpRun*	O	Low	No
Group stall	GrpStall*	I	Low	No
Fault	Fault*	O	Low	No
Quiet VCC for PLL	VccP	I	High	No
Quiet VSS for PLL	VssP	I	High	No
Status	Status(7:0)	O	High	No
VCC sense	VccSense	I/O	N/A	No
VSS sense	VssSense	I/O	N/A	No

T-49-17-38

9.0 Specifications

9.1 DC Characteristics

Maximum Ratings

Operation beyond the limits set forth in Table 9.1 may impair the useful life of the device.

Table 9.1 Maximum Ratings

Parameter	Symbol	Min	Max	Units
Supply Voltage	VCC	-0.5	+7.0	VDC
Input Voltage	VIN	-0.5(1)	+7.0	VDC
Storage Temperature	TST	-65.	+150.	°C
Operating Temperature	TA	0.	+70.	°C

Note: (1) VIN Min. = –3.0V for pulse width less than 15ns.

9.2 Operating Range

Table 9.2 Operating Range

Range	Case	VCC
Commercial	0 to 85°C	5V ± 5%

9.3 Operating Parameters

Table 9.3 Operating Parameters

Parameter	Symbol	Conditions	50MHz		Units
			Min	Max	
Output HIGH Voltage	VOH	IOH = -4mA	3.5		V
Output HIGH Voltage (MasterOut, TClock, RClock, SyncOut)	VOHC	IOH = -4mA	4.0		V
Output LOW Voltage	VOL	IOL = 4mA		0.4	V
Input HIGH Voltage	VIH		2.0	VCC+.5	V
Input LOW Voltage	VIL		-0.5(1)	0.8	V
Input HIGH Voltage (MasterClock, SyncIn)	VIHC		3.0	VCC+.5	V
Input LOW Voltage (MasterClock, SyncIn)	VILC		-0.5(1)	0.4	V
Input Capacitance	CIn			10.0	pF
Output Capacitance	COut			10.0	pF
Operating Current	ICC	VCC = 5.5V		1.82	A

Note: (1) VIL Min. = –3.0V for pulse width less than 15ns.

9.4 AC Characteristics

T-49-17-38

Table 9.3 Master Clock and Clock Parameters

Parameter	Symbol	Test Conditions	50 MHz		75 MHz		
			Min	Max	Min	Max	Units
MasterClock High	MCkHigh	Transition ≤ 5ns	8		5.33		ns
MasterClock Low	MCkLow	Transition ≤ 5ns	8		5.33		ns
MasterClock Freq			25	50	25	75	MHz
MasterClock Period	MCkP		20	40	13.33	40	ns
Clock Jitter (± on RClock, TClock,MasterOut, SyncOut)				1		1	ns

9.5 System Interface Parameters

Table 9.4 System Interface Parameters

Parameter	Symbol	50MHz		Units
		Min	Max	
Data Output Min	T_{DM}	2		ns
Data Output Max	T_{DO}		10	ns
Data Setup	T_{DS}	3		ns
Data Hold	T_{DH}	2		ns

All output timing specifications given assume 50pF of capacitive load.Output timing specifications should be derated where appropriate as shown in Table 9.5 below.

9.6 Capacitive Load Deration

Table 9.5 Capacitive Load Deration

Parameter	Symbol	50MHz		Units
		Min	Max	
Data Output Min	T_{DM}	2		ns

10.0 Physical Specifications

T-49-17-38

10.1 Pinout of R4000SC/MC

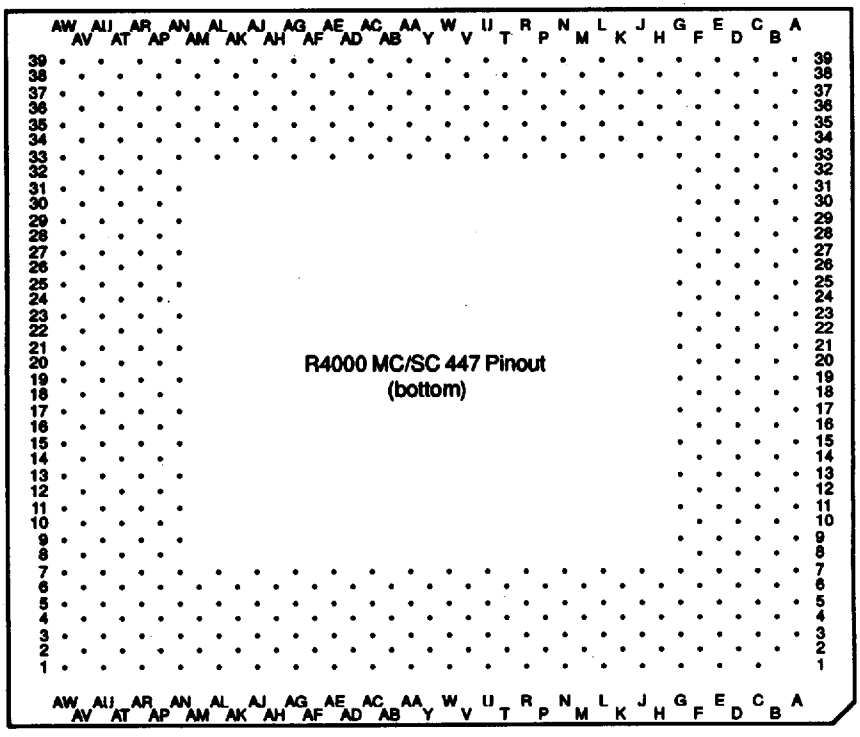


Figure 10.1 Pinout of the R4000SC/MC

PR4000SC/MC PACKAGE PINOUT

T-49-17-38

R4000SC/MC Function	Pkg Pin	R4000SC/MC Function	Pkg Pin	R4000SC/MC Function	Pkg Pin
ColdResetB	AW37	SCAddr13	Y6	SCData16	AE3
ExtRqstB	AV2	SCAddr14	W5	SCData17	AG5
FaultB	C39	SCAddr15	W7	SCData18	AK4
GrpRunB	AV24	SCAddr16	W1	SCData19	AN9
GrpStallB	AV20	SCAddr17	U3	SCData20	AU9
IOIn	AV32	SCAddr0W	AN7	SCData21	AN13
IOOut	AV28	SCAddr0X	AN5	SCData22	AT14
IntB0	AL1	SCAddr0Y	AM6	SCData23	AR17
IvdAckB	AA35	SCAddr0Z	AL7	SCData24	AT22
IvdErrB	AA39	SCDCSB	M6	SCData25	AU25
JTCK	U39	SCDChk0	G19	SCData26	AN27
JTDI	N39	SCDChk1	T34	SCData27	AR29
JTDO	J39	SCDChk2	AP20	SCData28	AN31
JTMS	G37	SCDChk3	AD34	SCData29	AR35
MasterClock	AA37	SCDChk4	C19	SCData30	AK36
MasterOut	AJ39	SCDChk5	R37	SCData31	AG35
ModeClock	B8	SCDChk6	AU19	SCData32	T6
ModeIn	AV8	SCDChk7	AE37	SCData33	L3
NMIB	AV16	SCDChk8	C17	SCData34	L7
PLLCap0	****	SCDChk9	N37	SCData35	E7
PLLCap1	****	SCDChk10	AU17	SCData36	G11
RClock0	AM34	SCDChk11	AG37	SCData37	E13
RClock1	AL33	SCDChk12	E19	SCData38	E15
RdRdyB	AW7	SCDChk13	R35	SCData39	G17
ReleaseB	AV12	SCDChk14	AR19	SCData40	C23
ResetB	AU39	SCDChk15	AE35	SCData41	F24
SC64Addr	Y2	SCData0	R3	SCData42	E27
SCAPar0	U5	SCData1	R7	SCData43	D30
SCAPar1	U1	SCData2	L5	SCData44	C33
SCAPar2	P4	SCData3	F8	SCData45	E35
SCAdd1	AL5	SCData4	C9	SCData46	L35
SCAdd2	AG1	SCData5	F12	SCData47	R33
SCAdd3	AE7	SCData6	G15	SCData48	AF4
SCAdd4	AC1	SCData7	E17	SCData49	AJ3
SCAdd5	AC5	SCData8	G21	SCData50	AJ7
SCAdd6	AC3	SCData9	C25	SCData51	AP8
SCAdd7	AA1	SCData10	G25	SCData52	AT10
SCAdd8	AB4	SCData11	E29	SCData53	AR13
SCAdd9	AA5	SCData12	G31	SCData54	AR15
SCAddr10	AA7	SCData13	C35	SCData55	AT18
SCAddr11	AA3	SCData14	K36	SCData56	AU23
SCAddr12	W3	SCData15	N35	SCData57	AT26

PR4000SC/MC PACKAGE PINOUT (CONTINUED)

T-49-17-38

R4000SC/MC Function	Pkg Pin	R4000SC/MC Function	Pkg Pin	R4000SC/MC Function	Pkg Pin
SCData58	AR27	SCData100	E9	SCTag5	D18
SCData59	AN29	SCData101	C11	SCTag6	F20
SCData60	AP32	SCData102	C13	SCTag7	E23
SCData61	AN35	SCData103	F16	SCTag8	D26
SCData62	AJ35	SCData104	E21	SCTag9	C29
SCData63	AE33	SCData105	G23	SCTag10	G29
SCData64	V4	SCData106	C27	SCTag11	E33
SCData65	R5	SCData107	F28	SCTag12	G35
SCData66	N5	SCData108	E31	SCTag13	L33
SCData67	E5	SCData109	G33	SCTag14	L37
SCData68	G9	SCData110	J37	SCTag150	P36
SCData69	E11	SCData111	N33	SCTag16	AF36
SCData70	G13	SCData112	AD6	SCTag17	AJ37
SCData71	D14	SCData113	AG3	SCTag18	AJ33
SCData72	C21	SCData114	AJ5	SCTag19	AN37
SCData73	D22	SCData115	AU5	SCTag20	AU35
SCData74	E25	SCData116	AN11	SCTag21	AR31
SCData75	G27	SCData117	AU11	SCTag22	AU29
SCData76	C31	SCData118	AU13	SCTag23	AN25
SCData77	F32	SCData119	AN17	SCTag24	AR23
SCData78	J35	SCData120	AR21	SCWrWB	J5
SCData79	M34	SCData121	AP24	SCWrXB	J7
SCData80	AC7	SCData122	AU27	SCWrYB	H6
SCData81	AE5	SCData123	AT30	SCWrZB	G5
SCData82	AG7	SCData124	AU33	Status0	U33
SCData83	AR5	SCData125	AN33	Status1	U35
SCData84	AR9	SCData126	AL37	Status2	V36
SCData85	AR11	SCData127	AG33	Status3	W35
SCData86	AN15	SCOEB	N1	Status4	W37
SCData87	AP16	SCTCSB	J1	Status5	AC37
SCData88	AU21	SCTChk0	AN21	Status6	AC35
SCData89	AN23	SCTChk1	AN19	Status7	AC33
SCData90	AR25	SCTChk2	AU15	SyncIn	W39
SCData91	AP28	SCTChk3	AP12	SyncOut	AN39
SCData92	AU31	SCTChk4	AU7	SysAD0	T2
SCData93	AR33	SCTChk5	AR7	SysAD1	M2
SCData94	AL35	SCTChk6	AH6	SysAD2	J3
SCData95	AH34	SCTag0	K4	SysAD3	G3
SCData96	U7	SCTag1	G7	SysAD4	C1
SCData97	N3	SCTag2	C7	SysAD5	A3
SCData98	N7	SCTag3	D10	SysAD6	A9
SCData99	C5	SCTag4	C15	SysAD7	A13

T-49-17-38

PR4000SC/MC PACKAGE PINOUT (CONTINUED)

R4000SC/MC Function	Pkg Pin	R4000SC/MC Function	Pkg Pin	R4000SC/MC Function	Pkg Pin
SysAD8	A21	SysAD50	AM2	Vcc	A39
SysAD9	A25	SysAD51	AR1	Vcc	B6
SysAD10	A29	SysAD52	AU3	Vcc	B10
SysAD11	A33	SysAD53	AW5	Vcc	B18
SysAD12	B38	SysAD54	AW11	Vcc	B26
SysAD13	E37	SysAD55	AW15	Vcc	B34
SysAD14	G39	SysAD56	AW23	Vcc	D4
SysAD15	L39	SysAD57	AW27	Vcc	D8
SysAD16	AD2	SysAD58	AW31	Vcc	D16
SysAD17	AH2	SysAD59	AW35	Vcc	D24
SysAD18	AL3	SysAD60	AU37	Vcc	D32
SysAD19	AN3	SysAD61	AR39	Vcc	D36
SysAD20	AU1	SysAD62	AL39	Vcc	F2
SysAD21	AW3	SysAD63	AG39	Vcc	F14
SysAD22	AW9	SysADC0	A17	Vcc	F22
SysAD23	AW13	SysADC1	R39	Vcc	F30
SysAD24	AW21	SysADC2	AW17	Vcc	F38
SysAD25	AW25	SysADC3	AD38	Vcc	H4
SysAD26	AW29	SysADC4	A19	Vcc	H36
SysAD27	AW33	SysADC5	T38	Vcc	K6
SysAD28	AV38	SysADC6	AW19	Vcc	K38
SysAD29	AR37	SysADC7	AC39	Vcc	Y38
SysAD30	AM38	SysCmd0	G1	Vcc	AB2
SysAD31	AH38	SysCmd1	E3	Vcc	AB34
SysAD32	R1	SysCmd2	B2	Vcc	AD4
SysAD33	L1	SysCmd3	B12	Vcc	AD36
SysAD34	H2	SysCmd4	B20	Vcc	AF6
SysAD35	E1	SysCmd5	B24	Vcc	AF38
SysAD36	C3	SysCmd6	B28	Vcc	AK2
SysAD37	A5	SysCmd7	B32	Vcc	AK34
SysAD38	A11	SysCmd8	A37	Vcc	AM4
SysAD39	A15	SysCmdP	H34	Vcc	AM36
SysAD40	A23	TClock0	H34	Vcc	AP2
SysAD41	A27	TClock1	J33	Vcc	AP10
SysAD42	A31	VCCOk	AE39	Vcc	AP18
SysAD43	A35	ValidInB	AN1	Vcc	AP26
SysAD44	C37	ValidOutB	AR3	Vcc	AP38
SysAD45	B39	WrRdyB	A7	Vcc	AT4
SysAD46	H38	VccSense	W33	Vcc	AT8
SysAD47	M38	VssSense	U37	Vcc	AT16
SysAD48	AE1	VccP	AA33	Vcc	AT24
SysAD49	AJ1	VssP	Y34	Vcc	AT32

PR4000SC/MC PACKAGE PINOUT (CONTINUED)

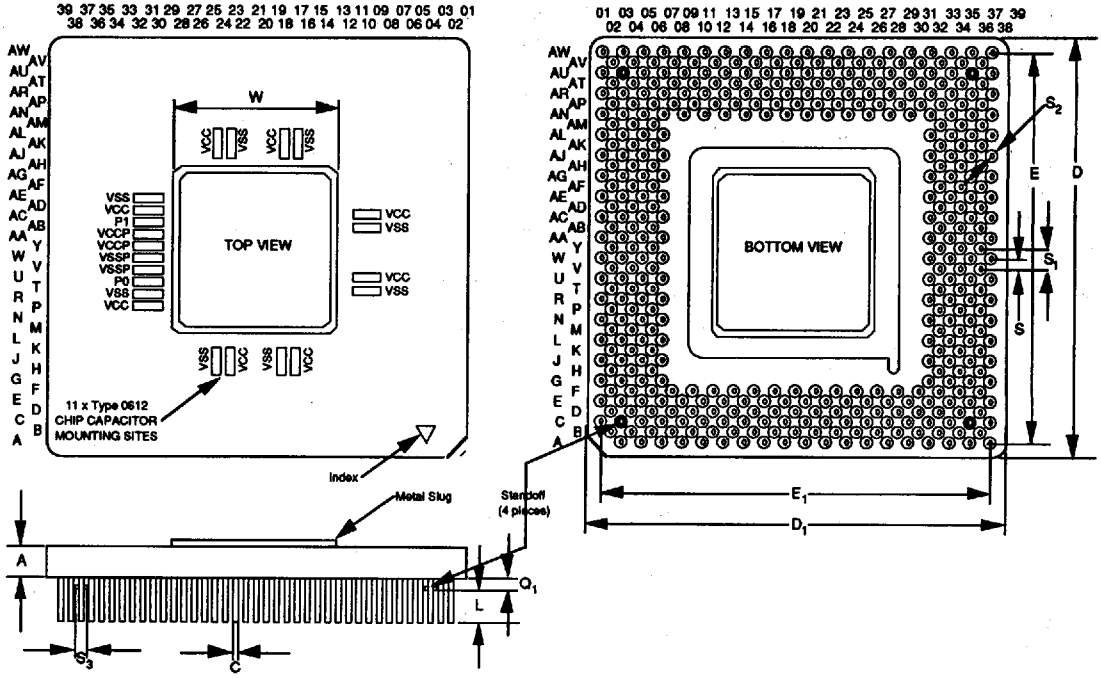
T-49-17-38

R4000SC/MC Function	Pkg Pin	R4000SC/MC Function	Pkg Pin
Vcc	AT36	Vss	P38
Vcc	AV6	Vss	V2
Vcc	AV14	Vss	Y4
Vcc	AV22	Vss	Y36
Vcc	AV30	Vss	AB6
Vcc	AV34	Vss	AB36
Vcc	AW1	Vss	AB38
Vcc	AW39	Vss	AF2
Vss	B4	Vss	AF34
Vss	B14	Vss	AH4
Vss	B22	Vss	AH36
Vss	B30	Vss	AK6
Vss	B36	Vss	AK38
Vss	D2	Vss	AP4
Vss	D6	Vss	AP6
Vss	D12	Vss	AP14
Vss	D20	Vss	AP22
Vss	D28	Vss	AP30
Vss	D34	Vss	AP34
Vss	D38	Vss	AP36
Vss	F4	Vss	AT2
Vss	F6	Vss	AT6
Vss	F10	Vss	AT12
Vss	F18	Vss	AT20
Vss	F26	Vss	AT28
Vss	F34	Vss	AT34
Vss	F36	Vss	AT38
Vss	K2	Vss	AV4
Vss	K34	Vss	AV10
Vss	M4	Vss	AV18
Vss	M36	Vss	AV26
Vss	P6	Vss	AV36

2

12.0 PR4000SC/MC 447-PIN CERAMIC PIN GRID ARRAY

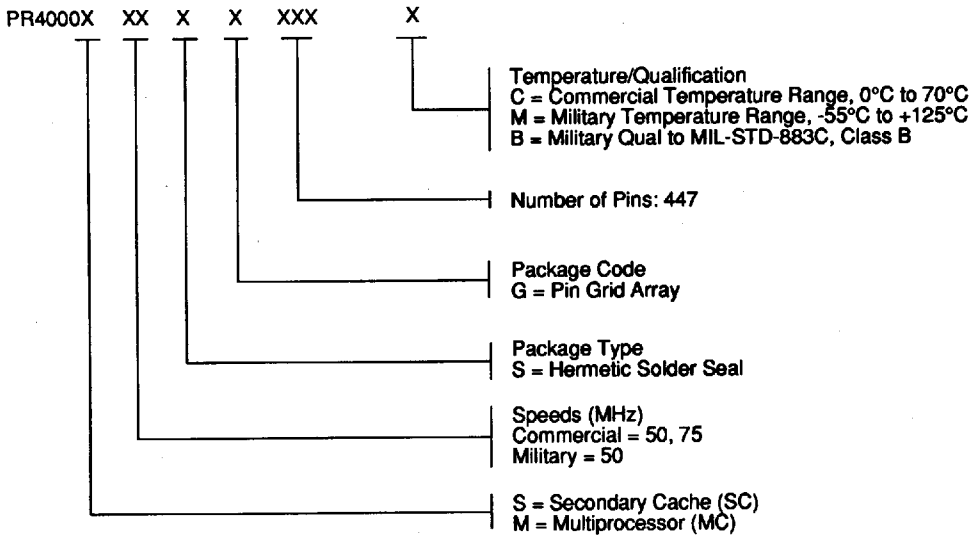
T-49-17-38



Symbol	Min.		Max	
	in.	mm.	in.	mm.
A	0.156	3,96	0.196	4,98
D	2.040	5,18	2.080	5,28
D_1	2.040	5,18	2.080	5,28 TYP
E	1.900	4,82	1.900	4,82 TYP
E_1	1.900	4,82	1.900	4,82 TYP
L	0.100	2,54	0.200	5,08
M	20	20	20	20
N	447	447	447	447
S	0.050 BSC	1,27 BSC	0.050 BSC	1,27 BSC
S_1	0.100 BSC	2,54 BSC	0.100 BSC	2,54 BSC
S_2	N/A	N/A	N/A	N/A
S_3	N/A	N/A	N/A	N/A
C	0.016	0,40	0.020	0,50
Q	N/A	N/A	N/A	N/A
Q_1	0.050	1,27	0.050	1,27
W	1.000	25,4	1.100	28,0

13.0 ORDERING INFORMATION

T-49-17-38



2