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LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

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	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15										

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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APPROVED BY: William K. Heckman

DRAWING APPROVAL DATE: 28 SEPTEMBER 1990

REVISION LEVEL:

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, DIGITAL, CMOS, 8 X 8 MULTIPLIER, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-90708

SHEET 1 OF 1

DESC FORM 193
SEP 87

* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-[illegible]/60911

5962-E1820

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:

5962-90708	01	X	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device type. The device type shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	TMC2208J4V	8 X 8 CMOS multiplier/accumulator

1.2.2 Case outline. The case outline shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
X	D-14 (48-lead, 2.435" x .620" x .225"), dual-in-line package

1.3 Absolute maximum ratings.

Supply voltage range (V_{DD})	-0.5 V dc to +7.0 V dc
Input voltage range	-0.5 V dc to (V_{DD} +0.5) V dc
Output:	
Applied voltage 1/	-0.5 V dc to (V_{DD} +0.5) V dc
Forced current 2/	-3.0 mA to +6.0 mA
Power dissipation 3/	200 mW
Storage temperature range	-65°C to +150°C
Junction temperature	+175°C
Case operating temperature range (T_C)	-60°C to +130°C
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-M-38510, appendix C

1/ Applied voltage must be current limited to specified range, and measured with respect to GND.
2/ Forcing voltage must be limited to specified range.
3/ Must withstand the added P_D due to short circuit test (e.g., I_{OS}).

1.4 Recommended operating conditions.

Supply voltage (V_{DD})	4.5 V dc to 5.5 V dc
Clock pulse width low (t_{PWL})	15 ns minimum
Clock pulse width high (t_{PWH})	15 ns minimum
Input setup time (t_s) (except PREL)	11 ns minimum
Input setup time (PREL, t_{sp})	13 ns minimum
Input hold time (t_H)	2 ns minimum
Input voltage low (V_{IL})	0.8 V dc maximum
Input voltage high (V_{IH})	2.0 V dc minimum
Case operating temperature range (T_C)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Case outline. The case outline shall be in accordance with 1.2.2 herein.

3.2.3 Truth table. The preload truth table shall be as specified on figure 2.

3.2.4 Block diagram. The block diagram shall be as specified on figure 3.

3.2.5 Data format. The data input/output formats shall be as specified on figure 4.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.7 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7 herein). The certificate of compliance submitted to DESC-ECC prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECC shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition B or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C < T_C < +125°C$ unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Supply current, quiescent	I_{DDQ}	V_{DD} = Max, V_{IN} = 0 V	01	1,2,3		10	mA
Supply current	I_{DD}	V_{DD} = Max, F = 20 MHz TSL, TSM, TSX = 5.0 V	01	1,2,3		28	mA
Input current, low	I_{IL}	V_{DD} = Max, V_I = 0 V	01	1,2,3		-10	µA
Input current, high	I_{IH}	V_{DD} = Max, V_I = V_{DD}	01	1,2,3		10	µA
Output voltage, low	V_{OL}	V_{DD} = Min, I_{OL} = 4 mA	01	1,2,3		0.4	V
Output voltage, high	V_{OH}	V_{DD} = Min, I_{OH} = -2 mA	01	1,2,3	2.4		V
Short circuit current 1/	I_{OS}	V_{DD} = Max	01	1,2,3		-100	mA
Output leakage current, low	I_{OZL}	V_{DD} = Max, V_I = 0V	01	1,2,3		-40	µA
Output leakage current, high	I_{OZH}	V_{DD} = Max, V_I = V_{DD}	01	1,2,3		40	µA
Input capacitance	C_{IN}	f = 1.0 MHz, T_A = 25°C see 4.3.1c	01	4		15	pF
Output capacitance	C_{OUT}	f = 1.0 MHz, T_A = 25°C see 4.3.1c	01	4		15	pF
Functional testing		V_{DD} = 5.0 V see 4.3.1d	01	7,8			
Multiply/Accumulate time 2/	t_{MA}	V_{DD} = Min, see figure 5	01	9,10,11		50	ns
Output delay time 2/	t_D	V_{DD} = Min, see figure 5	01	9,10,11		25	ns
Three-state enable time	t_{ENA}	V_{DD} = Min, see figure 5	01	9,10,11		21	ns
Three-state disable time	t_{DIS}	V_{DD} = Min, see figure 5	01	9,10,11		18	ns

1/ One output to ground, one second duration maximum, output high.

2/ All transitions are measured at 1.5 V level. Inputs are driven at V_{IL} = 0 V and V_{IH} = 3 V during dynamic testing.

Device type 01

Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	P_{12}	25	X_3
2	P_{11}	26	X_4
3	P_{10}	27	X_5
4	P_9	28	X_6
5	P_8	29	X_7
6	TSM	30	CLK X
7	CLK P	31	CLK Y
8	PREL	32	Y_0
9	P_7	33	Y_1
10	P_6	34	Y_2
11	P_5	35	Y_3
12	GND	36	Y_4
13	P_4	37	V_{DD}
14	P_3	38	Y_5
15	P_2	39	Y_6
16	P_1	40	Y_7
17	P_0	41	TC
18	TSL	42	TSX
19	SUB	43	P_{18}
20	ACC	44	P_{17}
21	RND	45	P_{16}
22	X_0	46	P_{15}
23	X_1	47	P_{14}
24	X_2	48	P_{13}

FIGURE 1. Terminal connections.

Device type 01

PREL	TSX	TSM	TSL	XTP	MSP	LSP
L	L	L	L	Register->Output pin	Register->Output pin	Register->Output pin
L	L	L	H	Register->Output pin	Register->Output pin	Hi-Z
L	L	H	L	Register->Output pin	Hi-Z	Register->Output pin
L	L	H	H	Register->Output pin	Hi-Z	Hi-Z
L	H	L	L	Hi-Z	Register->Output pin	Register->Output pin
L	H	L	H	Hi-Z	Register->Output pin	Hi-Z
L	H	H	L	Hi-Z	Hi-Z	Register->Output pin
L	H	H	H	Hi-Z	Hi-Z	Hi-Z
H	L	L	L	Hi-Z	Hi-Z	Hi-Z
H	L	L	H	Hi-Z	Hi-Z	Hi-Z Preload
H	L	H	L	Hi-Z	Hi-Z Preload	Hi-Z
H	L	H	H	Hi-Z	Hi-Z Preload	Hi-Z Preload
H	H	L	L	Hi-Z Preload	Hi-Z	Hi-Z
H	H	L	H	Hi-Z Preload	Hi-Z	Hi-Z Preload
H	H	H	L	Hi-Z Preload	Hi-Z Preload	Hi-Z
H	H	H	H	Hi-Z Preload	Hi-Z Preload	Hi-Z Preload

FIGURE 2. Preload truth table.

Device type 01

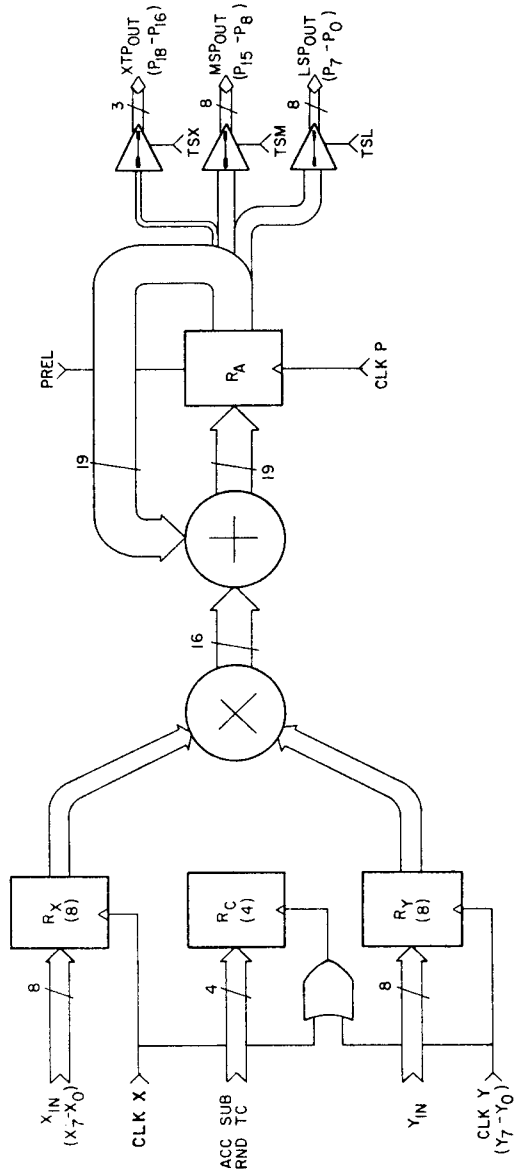

FIGURE 3. Block diagram.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-90708
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Device type 01

Fractional two's complement notation

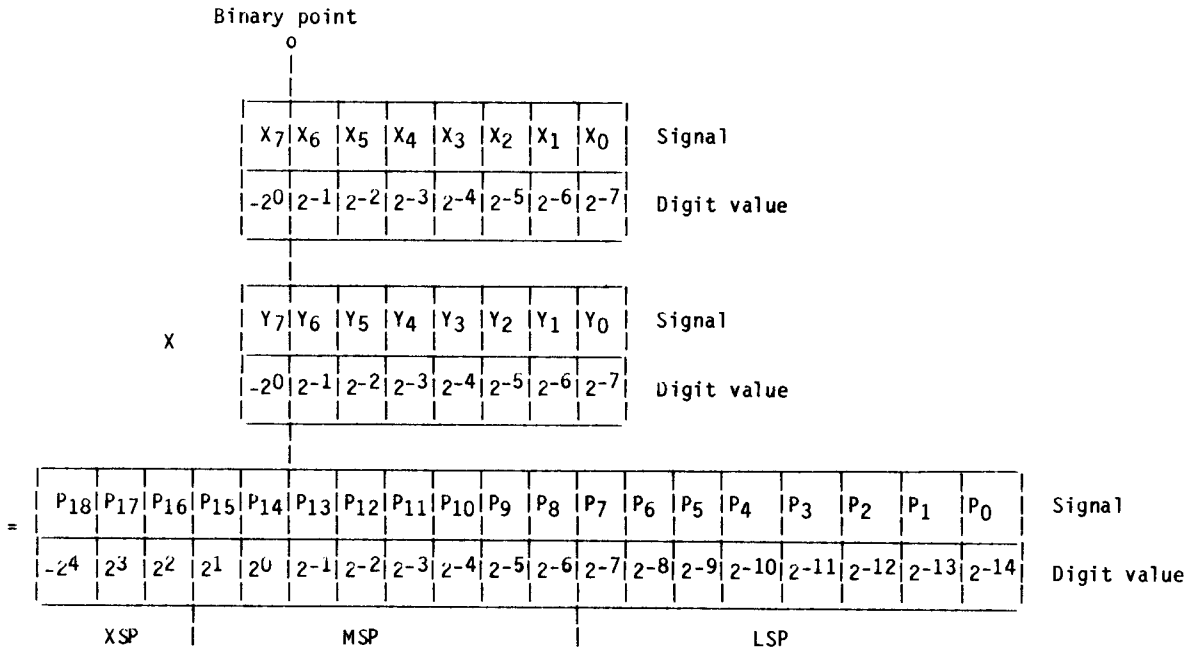

FIGURE 4. Input/output data formats.

Device type 01

Fractional unsigned magnitude notation

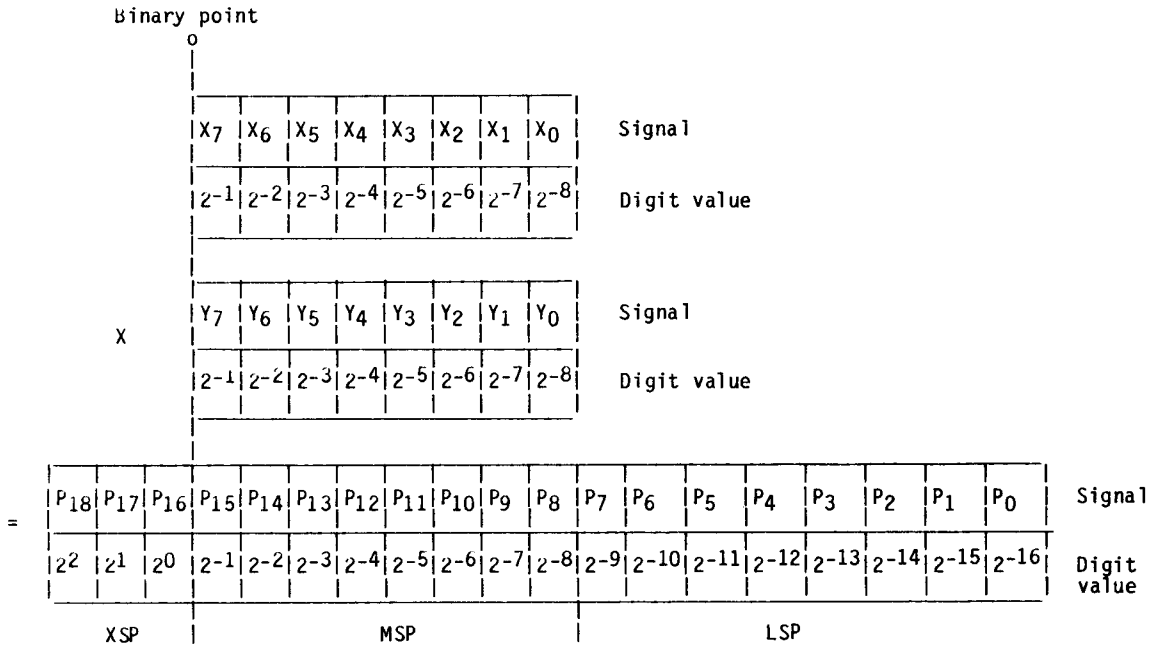

FIGURE 4. Input/output data formats - Continued.

Integer two's complement notation

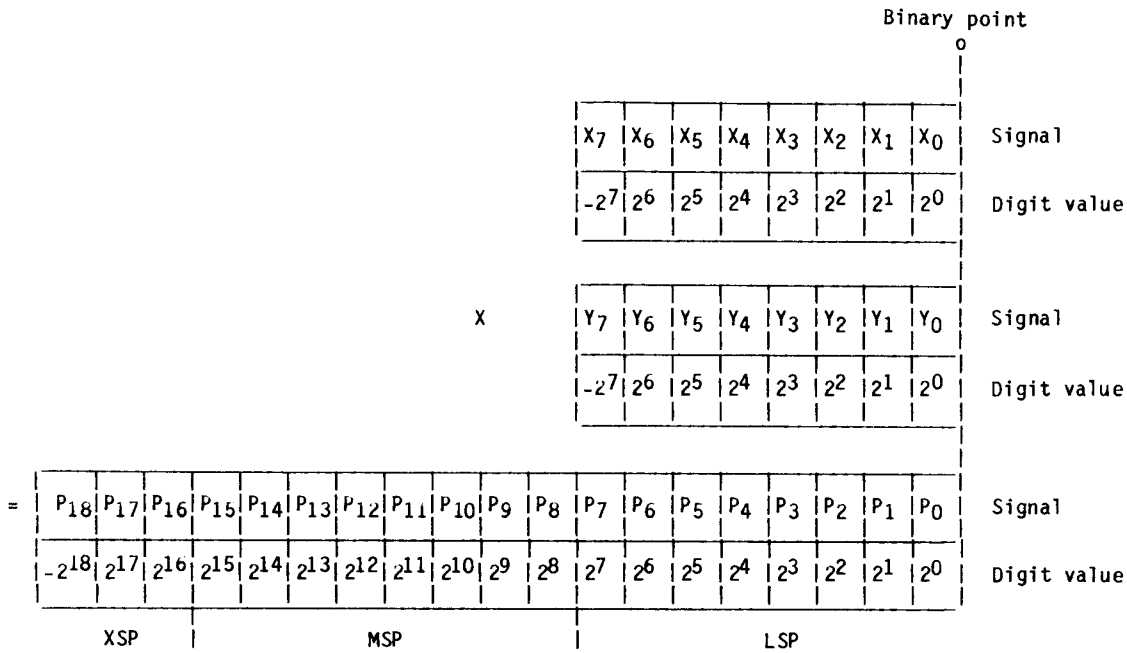

FIGURE 4. Input/output data formats - Continued.

Integer unsigned magnitute notation

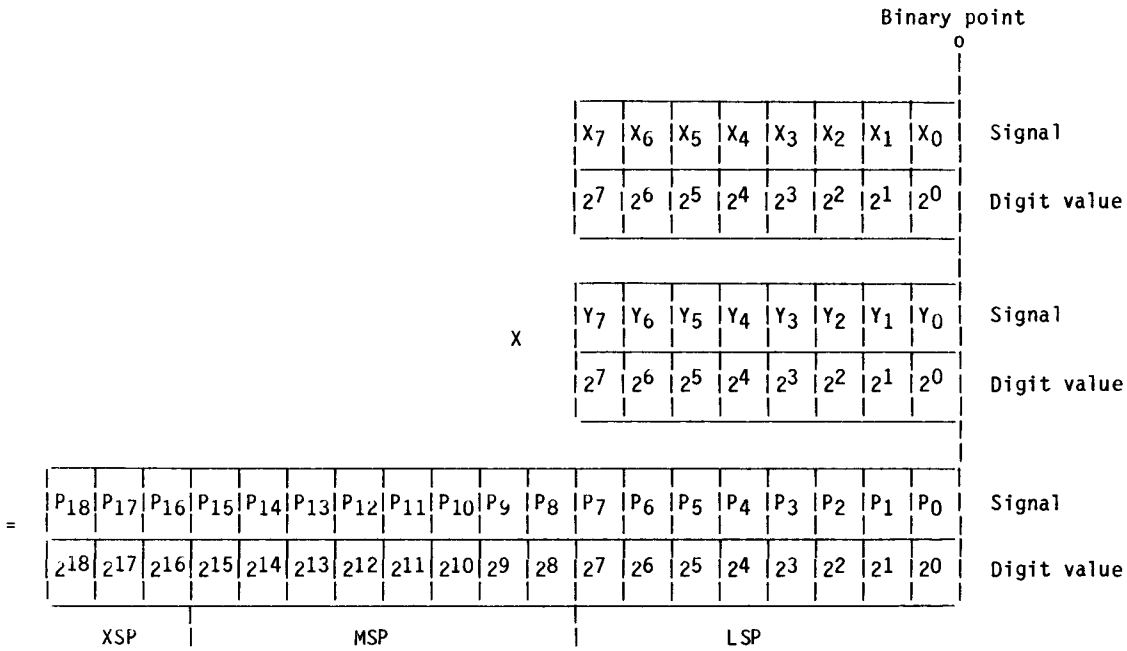

FIGURE 4. Input/output data formats - Continued.

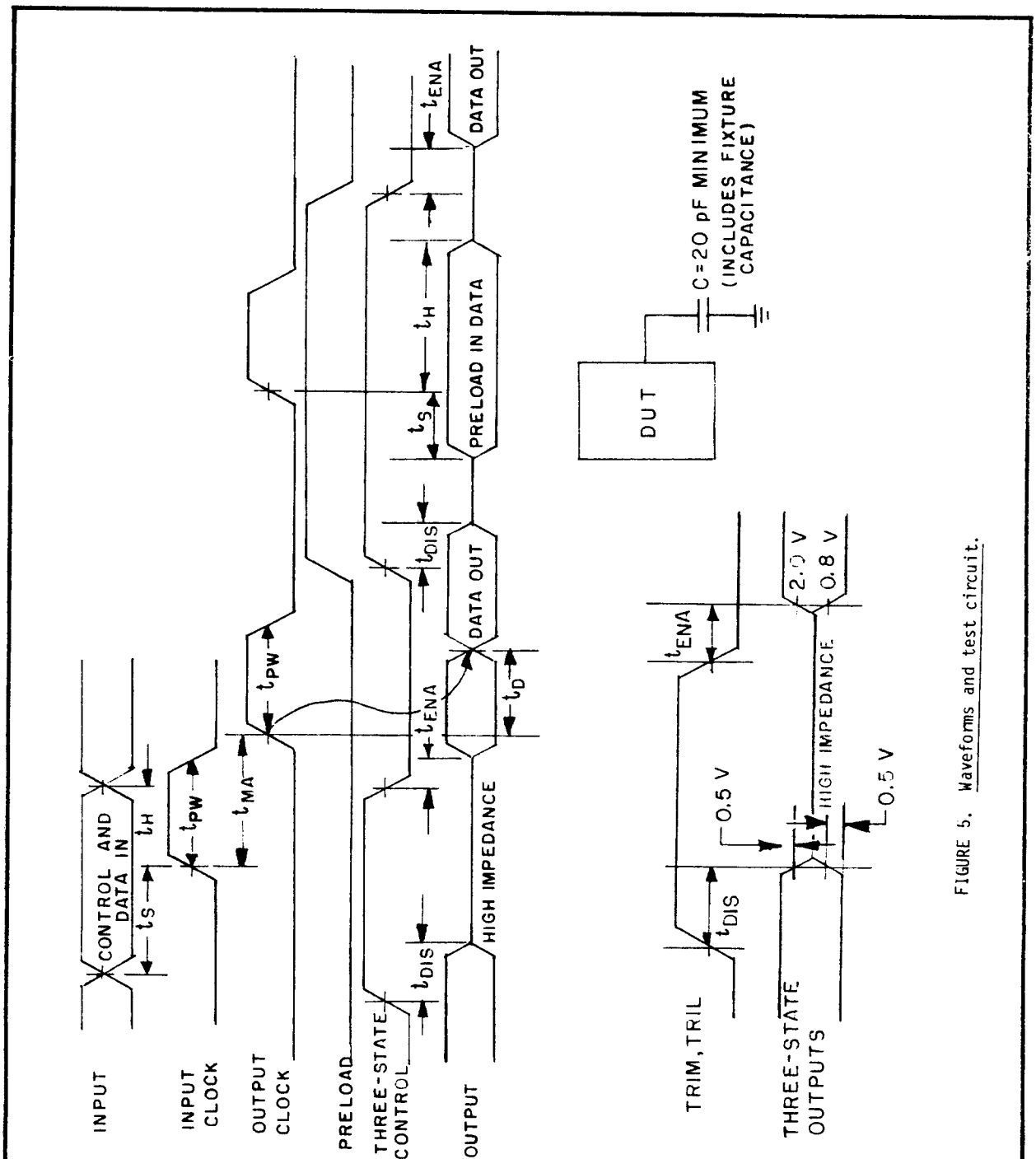

FIGURE 5. Waveforms and test circuit.

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TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 7, 9

*PDA applies to subgroup 1.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial test and after process or design changes which may affect input capacitance. A minimum sample size of five devices with zero rejects shall be required.

d. Subgroups 7 and 8 shall consist of verifying the functionality of the device. These tests form a part of the vendor's test tape and shall be maintained and available from the approved sources of supply.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition B or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECC, telephone (513) 296-6022.

6.5 Comments. Comments on this drawing should be directed to DESC-ECC, Dayton, Ohio 45444, or telephone (513) 296-5375.

6.6 Terminal and pin definitions.

V_{DD}, GND. The device operates from a single +5 V supply. All power and ground lines must be connected.

X_{7-0}. The 8-bit two's complement or unsigned magnitude X data input. X_7 is the MSB and contains the sign information for two's complement notation. The data on the X input is clocked into the input register on the rising edge of CLK X.

Y_{7-0}. The 8-bit two's complement or unsigned magnitude Y data input. Y_7 is the MSB and contains the sign information for two's complement notation. The data on the Y input is clocked into the input register on the rising edge of CLK Y.

P_{18-0}. P_{18-0} is the accumulated product result. The 19-bit output is either the two's complement or unsigned magnitude result of the accumulated products. The output is divided into two 8-bit output words (MSP, LSP) and one 3-bit output word (XTP). P_{18} is the MSB and contains the sign information for two's complement notation. Formats for two's complement, fractional unsigned magnitude, integer two's complement and integer unsigned notation are shown on figure 4.

CLK X, CLK Y. The rising edge of CLK X and CLK Y loads the data lines into the appropriate input register. The RouND (RND), Two's Complement (TC), ACCumulate (ACC), and SUBtract (SUB) control inputs are registered and loaded on the logical OR of both CLK X and CLK Y. Special attention to the clock signals is required if normally high clock signals are used. Problems can be avoided by the use of normally low clocks.

CLK P. This input is used to clock the accumulated product sum into the output register. If $\overline{ACC}$ is high, the content of the output register is added to the next product generated and loaded into the output register. CLK P is also used to preload the output register from the output pins.

TSX, TSM, TSL. TSX is the three-state control for the 3-bit XTP output drivers. TSM and TSL are the three-state controls for the MSP and LSP output, respectively. The outputs are in the high-impedance state when the control is high, and enabled when the control is low.

PREL. PRELoad is the active-high control used to directly load the output register. When PREL is high, all output buffers are forced into the high-impedance state. Second, when any or all of the TSX, TSM, TSL controls are also high, external data present at the output pins will be preloaded into the corresponding section of the output register on the rising edge of CLK P. Normal data setup and hold times apply both to the logical AND of PREL and the relevant three-state control (TSX, TSM, TSL) and to the data being preloaded.

RND. The RouND input is used to control the rounding of results. When RND is high, a 1 is added to the most significant bit (MSB) of the LSP for the rounding the product in the MSP and XTP rather than truncating it. The control is to improve accuracy when the LSP will not be used.

TC. The Two's Complement input is used to control how the device interprets the data on the X and Y inputs. TC high makes both inputs two's complement, while TC low makes both inputs unsigned magnitude numbers.

ACC. When ACCumulate is high, the content of the output register is added or subtracted from the next product generated, and their sum stored back into the output register on the next rising edge of CLK P. When ACC is low, multiplication without accumulation is performed, and the next product generated is stored into the output registers directly. This operation is used for the first term in a summation to avoid a separate "clear" operation.

SUB. SUBtract is used in conjunction with the ACC control. When both the ACC and SUB controls are high, the content of the output register is subtracted from the next product generated and the difference is stored back into the output register. Note that the previous output is subtracted from the product, not the product from the previous output.

6.7 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECC.

STANDARDIZED MILITARY DRAWING SOURCE APPROVAL BULLETIN

DATE: 28 SEPT 1990

An approved source of supply for SMD 5962-90708 is listed below for immediate acquisition only and shall be added to MIL-BUL-103 during the next revision. MIL-BUL-103 will be revised to include the addition or deletion of sources. The vendor listed below has agreed to this drawing and a certificate of compliance has been submitted to and accepted by DESC-ECS. This bulletin is superseded by the next dated revision of MIL-BUL-103.

Standardized military drawing PIN	Vendor CAGE number	Vendor similar PIN 1/
5962-9070801XX	59621	TMC2208J4V

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
59621	TRW LSI Products Inc. 4243 Campus Point Court San Diego, CA 92121

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in this information bulletin.