REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

REV STATUS OF PAGES	REV																
	PAGES	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

Defense Electronics
Supply Center
Dayton, Ohio

Original date of drawing:

30 June 1987

AMSC N/A

PREPARED BY Ray Monnin

CHECKED BY DA DiCenzo

APPROVED BY

MILITARY DRAWING

This drawing is available for use by all Departments and Agencies of the Department of Defense

TITLE: MICROCIRCUITS, DIGITAL, INTEGRATED BUS CONTROLLER, MONOLITHIC SILICON

SIZE	CODE IDENT. NO.	DWG NO.
A	14933	5962-87672

REV

PAGE 1 **OF** 16

5962-E493

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

DESC FORM 193
MAY 86

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

5962-87672	01	Y	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device type. The device type shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	82188	Integrated bus controller

1.2.2 Case outline. The case outline shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
Y	D-10 (28-lead, 1/2" x 1 3/8"), dual-in-line package

1.3 Absolute maximum ratings.

Storage temperature range - - - - - - - - - - - - - - - -	-65°C to +150°C
Voltage on any pin with respect to ground - - - - - -	-1.0 V dc to +7 V dc
Maximum power dissipation (P_D)- - - - - - - - - - - - -	0.7 W
Lead temperature (soldering, 10 seconds)- - - - - - -	+300°C
Thermal resistance, junction to case (θ_{JC})- - - - - -	40°C/W
Junction temperature- - - - - - - - - - - - - - - - - -	+200°C

1.4 Recommended operating conditions.

Case operating temperature range (T_C) - - - - - - - - -	-55°C to +125°C
Supply voltage (V_{CC})- - - - - - - - - - - - - - - - - -	5 V dc ±10%

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Block diagram. The block diagram shall be as specified on figure 2.

3.2.3 Case outline. The case outline shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full recommended case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein.

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55^{\circ}C \leq T_C \leq +125^{\circ}C$ $V_{CC} = 5\ V \pm 10\%$	Group A subgroups	Limits		Unit
				Min	Max	
Input low voltage	V_{IL}		1,2,3	-.5 1/	.8	V
Input high voltage	V_{IH}		1,2,3	2.0	V_{CC}+ 0.5 1/	V
Output low voltage	V_{OL}	$I_{OL} = 2$ mA	1,2,3		.45	V
Output high voltage	V_{OH}	$I_{OH} = -400\ \mu A$	1,2,3	2.4		V
Power supply current	I_{CC}		1,2,3		100	mA
Input leakage current	I_{LI}	$0\ V < V_{IN} < V_{CC}$	1,2,3		±10	µA
Output leakage current	I_{LO}	$.45\ V < V_{OUT} < V_{CC}$ Only $\overline{WR}$, $\overline{RD}$ and $\overline{DEN}$ pins are three-statable.	1,2,3		±10	µA
CLK input low voltage	V_{CLI}		1,2,3	-.5 1/	.6	V
CLK input high voltage	V_{CHI}		1,2,3	3.9	V_{CC}+ 1.0 1/	V
Input capacitance	C_{IN}	See 4.3.1c	4		10	pF
I/O capacitance	C_{IO}	See 4.3.1c	4		20	pF
Clock period	t_{CLCL}	See figures 3 and 4	9,10,11	125	500	ns
Clock low time	t_{CLCH}		9,10,11	1/2 (t_{CLCL}) -7.5		ns
Clock high time	t_{CHCL}		9,10,11	1/2 (t_{CLCL}) -7.5		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55^{\circ}C \leq T_C \leq +125^{\circ}C$ $V_{CC} = 5\ V \pm 10\%$	Group A subgroups	Limits Min	Limits Max	Unit
ARDY active setup time	t_{ARYHCL}	See figures 3 and 4	9,10,11	20		ns
ARDY hold time 2/	t_{CHARYL}		9,10,11	15		ns
ARDY inactive setup time	t_{ARYLCH}		9,10,11	35		ns
SRDY input setup time 3/	t_{SRYHCL}		9,10,11	65,50		ns
STATUS active setup time	t_{SVCH}		9,10,11	55		ns
STATUS inactive setup time	t_{SXCL}		9,10,11	50		ns
QSOI, QS1I setup time	t_{QIVCL}		9,10,11	15		ns
HLDA setup time	t_{HAVGV}		9,10,11	50		ns
SYSHOLD asynchronous setup time	t_{SHVCL}		9,10,11	25		ns
$\overline{RQ}/\overline{GT}$ input setup time 4/ 5/	t_{GVCH}		9,10,11	0		ns
Status valid to ALE delay 6/	t_{SVLH}		9,10,11		30	ns
ALE inactive delay	t_{CHLL}		9,10,11		30	ns
$\overline{RD}$, $\overline{WR}$ active delay	t_{CLML}		9,10,11	10	70	ns
$\overline{RD}$, $\overline{WR}$ inactive delay	t_{CLMH}		9,10,11	10	55	ns
Status to DT/$\overline{R}$ delay 7/	t_{SVDTV}		9,10,11		30	ns
DT/$\overline{R}$ active delay 7/	t_{CLDTV}		9,10,11		55	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55^\circ C \le T_C \le +125^\circ C$ $V_{CC} = 5\ V \pm 10\%$	Group A subgroups	Limits		Unit
				Min	Max	
$\overline{\text{DEN}}$ active delay	t_{CHDNV}	See figures 3 and 4	9,10,11	10	55	ns
$\overline{\text{DEN}}$ inactive delay 1/	t_{CHDNX}		9,10,11	10	55	ns
QS00, QS10 delay	t_{CLQOV}		9,10,11	5	50	ns
Hold delay 1/ 5/	t_{CHHV}		9,10,11		50	ns
SYSHLDA delay 5/	t_{CLSAV}		9,10,11		50	ns
$\overline{\text{RQ/GT}}$ output delay 5/	t_{CLGV}		9,10,11		40	ns
$\overline{\text{RQ/GTO}}$ to hold delay 1/ 5/	t_{GVHV}		9,10,11		50	ns
ALE active delay 6/	t_{CLLH}		9,10,11		30	ns
Command enable delay	t_{AELCV}		9,10,11		40	ns
Command disable delay	t_{AEHCX}		9,10,11		40	ns
SRO output delay 5/ 8/	t_{CHRO}		9,10,11	5	30	ns
SRDY to SRO delay 8/	t_{SRYHRO}		9,10,11		30	ns
$\overline{\text{CSIN}}$ to $\overline{\text{CSOUT}}$ delay	t_{CSISCO}		9,10,11		30	ns
CLK low to $\overline{\text{CSOUT}}$ delay 1/	t_{CLCSOV}		9,10,11	10		ns
CLK low to $\overline{\text{CSOUT}}$ inactive delay 1/	t_{CLCSOH}		9,10,11	10		ns

See footnotes on next page.

1/ Guaranteed, if not tested.

2/ The falling edge of ARDY must be synchronized to CLK.

3/ t_{SRYHOL} = (80186's) t_{SRYCL} + 30 ns = 65 ns for 6 MHz operation and 50 ns for 8 MHz operation.

4/ Due to test equipment limitations, actual tested values may differ from those specified, but specified values are guaranteed.

5/ C_L = 20 pF to 100 pF.

6/ ALE will be asserted to the latest of t_{SVLH} and t_{CLLH}.

7/ DT/$\overline{R}$ will be asserted to the latest of t_{SVDTV} and t_{CLDTV}.

8/ SRO will be asserted to the latest of t_{CHRO} and t_{SRYHRO}.

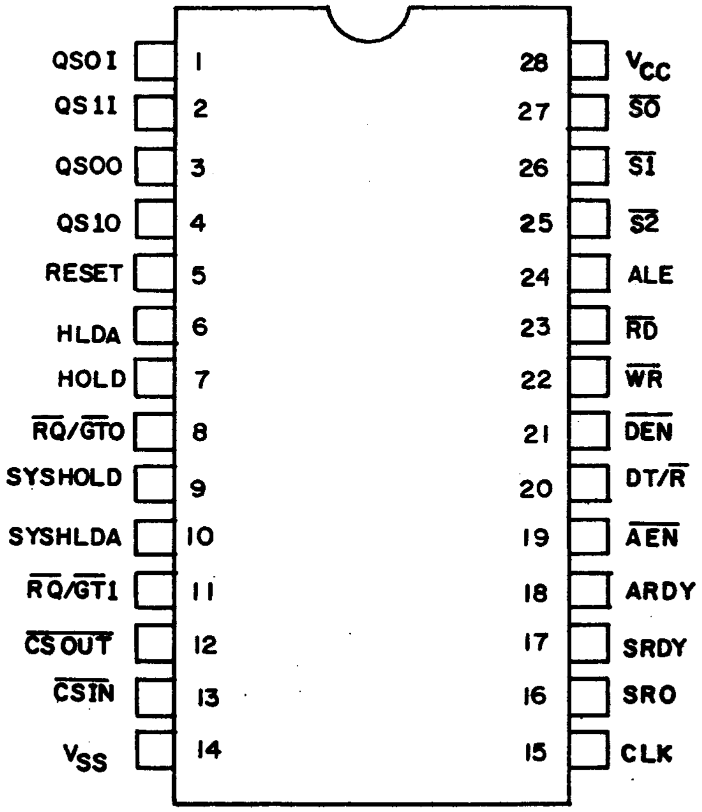


FIGURE 1. Terminal connections.

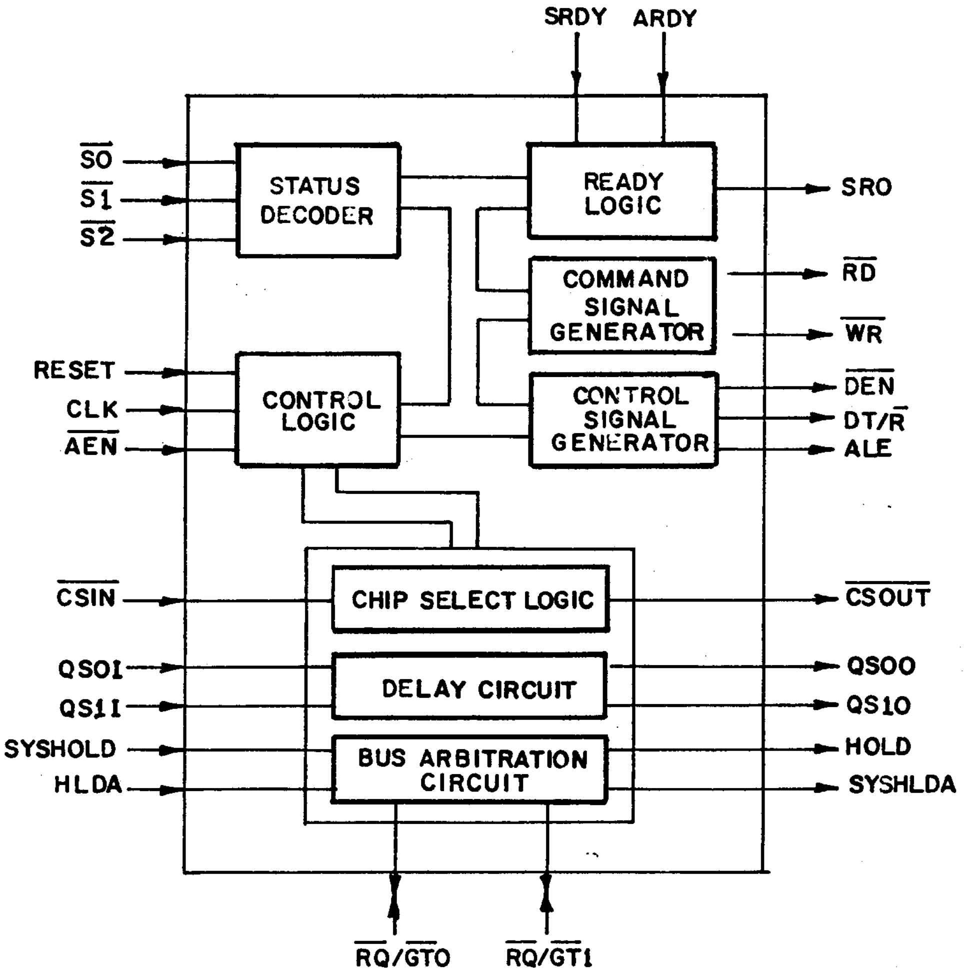
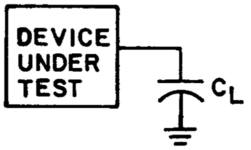


FIGURE 2. Block diagram.

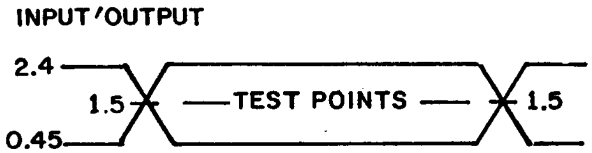
AC testing load circuit



C_L includes jig capacitance
C_L = 20 to 200 pF jig capacitance

FIGURE 3. Load circuit.

AC Testing input, output waveform



AC testing: Inputs are driven at 2.4 V for a logic '1' and 0.45 V for a logic '0'.

FIGURE 4. Switching waveforms.

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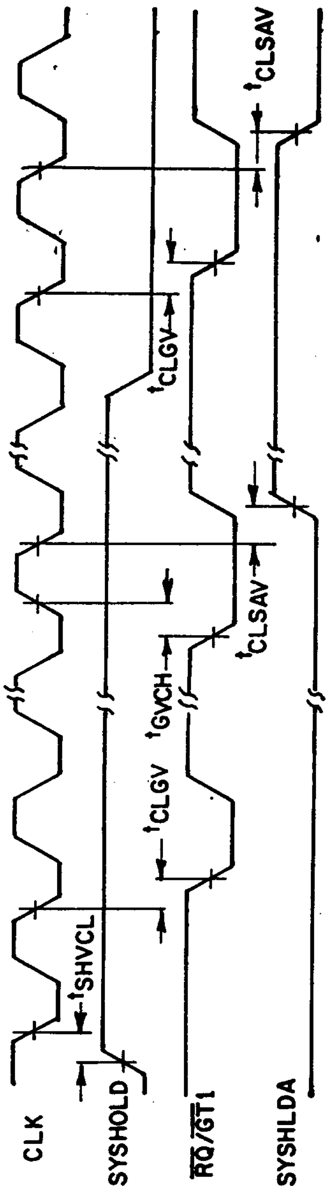
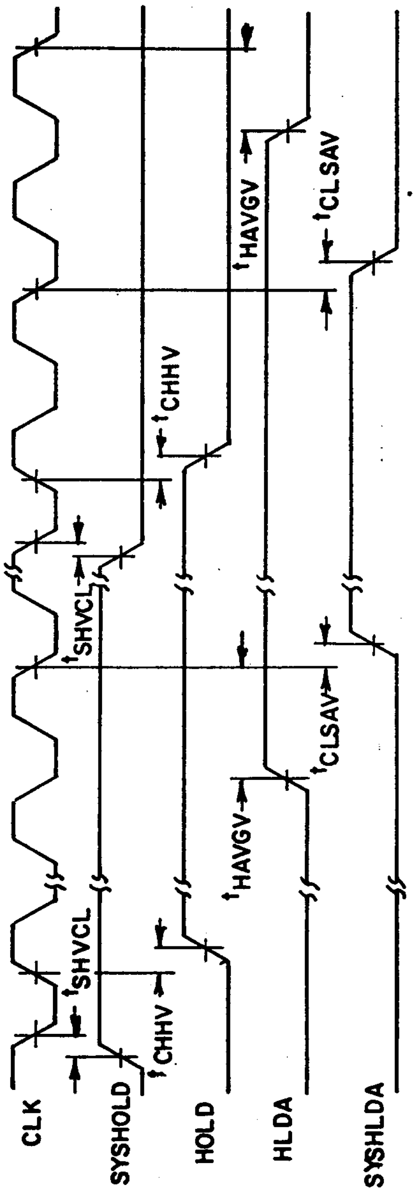
		REV	PAGE 10



SYSHOLD-SYSHLDA to $\overline{RQ}/\overline{GT1}$ timing-80186 mode and 8086 mode



SYSHOLD-SYSHLDA to HOLD-HLDA timing-80186 mode

FIGURE 4. Switching waveforms - Continued.

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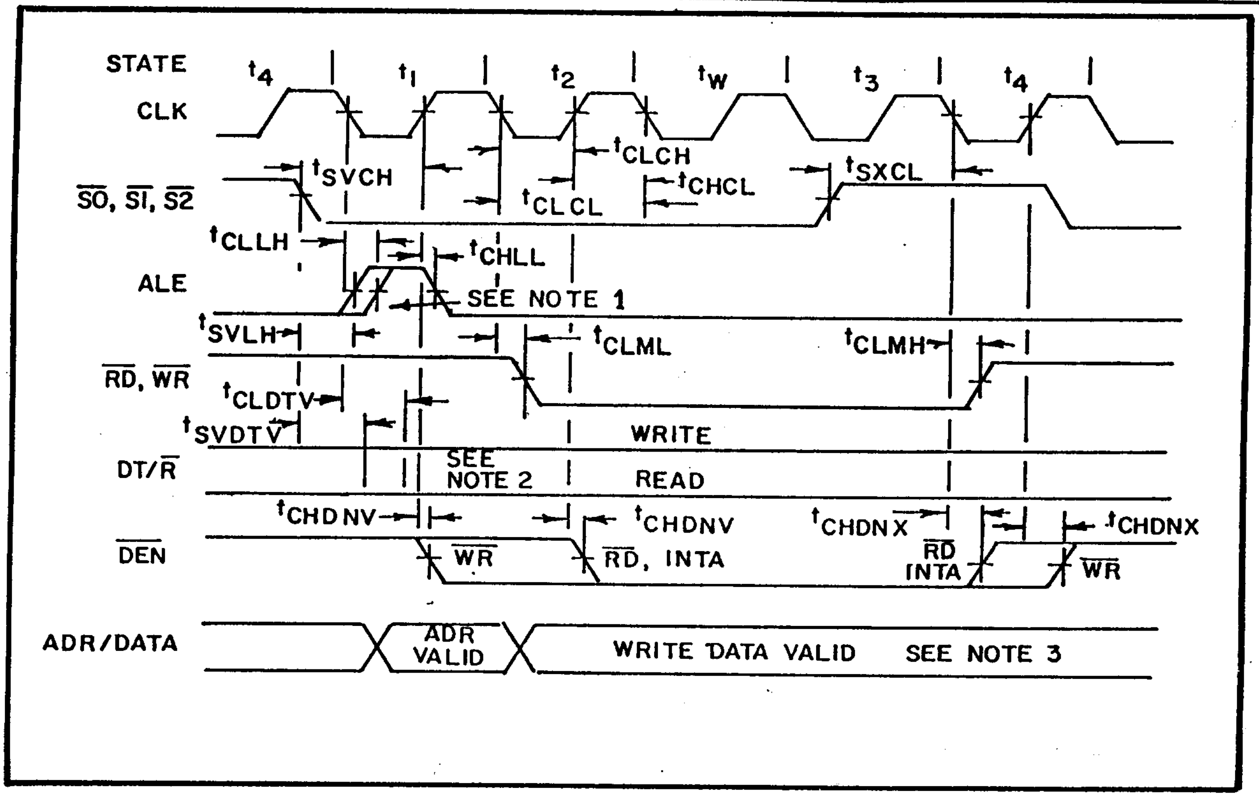
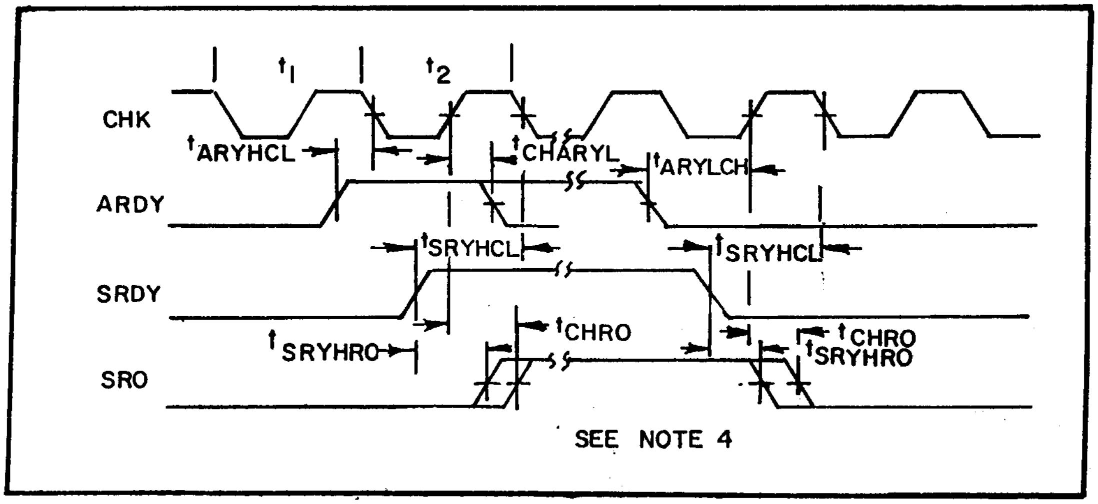
		REV	PAGE 11

DESC FORM 193A
FEB 86



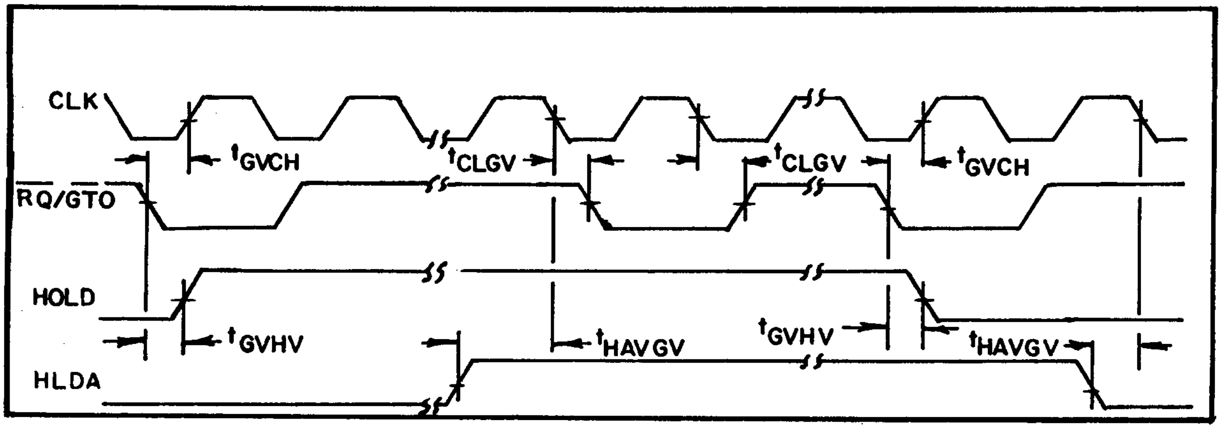
Command and control waveforms-80186 mode



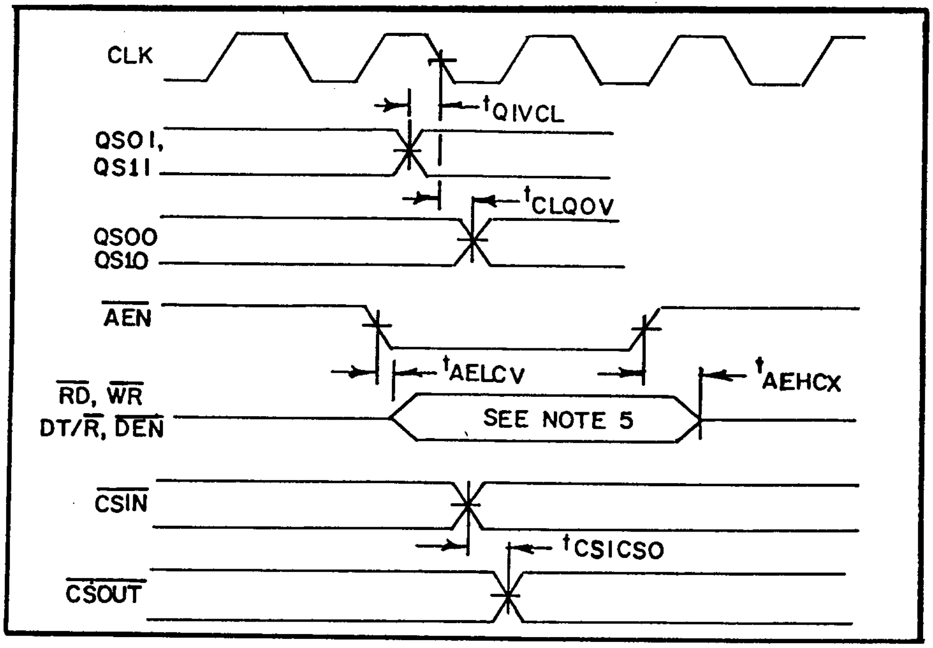
READY timing-80186 mode

FIGURE 4. Switching waveforms - Continued.

MILITARY DRAWING **DEFENSE ELECTRONICS SUPPLY CENTER** **DAYTON, OHIO**	SIZE A	CODE IDENT. NO. **14933**	DWG NO. 5962-87672
		REV	PAGE 12



$\overline{RQ}/\overline{GT0}$ to HOLD-HLDA timing-80186 mode



Queue status, $\overline{ALE}$, chip select delay timing-80186 mode.

NOTES:

1. ALE will asserted to the latest of t_{SVLH} and t_{CLLH}.
2. DT/$\overline{R}$ will asserted to the latest of t_{SVDTV} and t_{CLDTV}.
3. Address/data bus shown for references only.
4. SRO will be asserted to the latest of t_{CHRO} and t_{SRVHRO}.
5. DT/$\overline{R}$ pin is not three-statable.

FIGURE 4. Switching waveforms - continued.

MILITARY DRAWING **DEFENSE ELECTRONICS SUPPLY CENTER** **DAYTON, OHIO**	SIZE A	CODE IDENT. NO. **14933**	DWG NO. 5962-87672
		REV	PAGE 13

DESC FORM 193A
FEB 86

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test (method 1015 of MIL-STD-883).

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{IO} measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test (method 1005 of MIL-STD-883) conditions:

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by appendix B of MIL-M-38510 and method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*,2,3,7*,8,9,10,11
Group A test requirements (method 5005)	1,2,3,7,8,9,10,11
Groups C and D end-point electrical parameters (method 5005)	2, 8(Hot), 10
Additional electrical subgroups for group C periodic inspections	---

* PDA applies to subgroups 1 and 7.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.4 Approved source of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/	Replacement military specification part number
5962-8767201YX	34649	MD82188/B	---

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34649	Intel Corporation 5000 W. Williams Field Road Chandler, AZ 85224

MILITARY DRAWING **DEFENSE ELECTRONICS SUPPLY CENTER** **DAYTON, OHIO**	SIZE A	CODE IDENT. NO. 14933	DWG NO. 5962-87672
		REV	PAGE 16