XN01113 (XN1113)

Silicon PNP epitaxial planar type

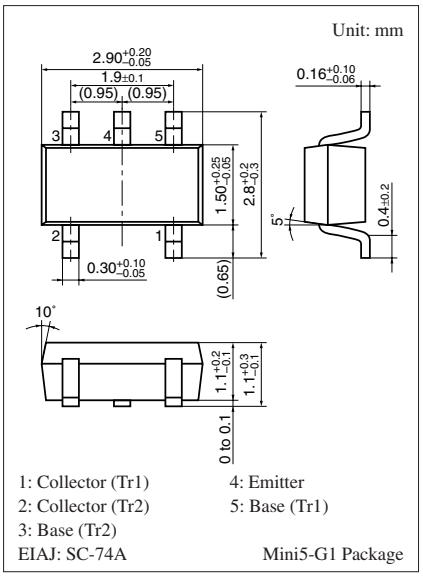
For switching/digital circuits

■ Features

- Two elements incorporated into one package (Emitter-coupled transistors with built-in resistor)
- Reduction of the mounting area and assembly cost by one half

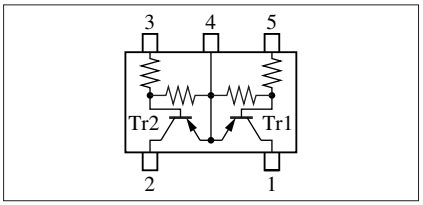
■ Basic Part Number

- UNR2113 (UN2113) × 2



Marking Symbol: 7L

Internal Connection



■ Absolute Maximum Ratings $T_a = 25°C$

Parameter	Symbol	Rating	Unit
Collector-base voltage (Emitter open)	V_{CBO}	−50	V
Collector-emitter voltage (Base open)	V_{CEO}	−50	V
Collector current	I_C	−100	mA
Total power dissipation	P_T	300	mW
Junction temperature	T_j	150	°C
Storage temperature	T_{stg}	−55 to +150	°C

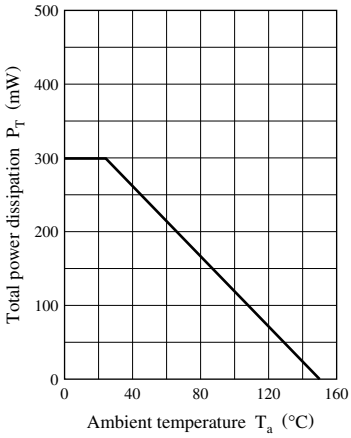
■ Electrical Characteristics $T_a = 25°C \pm 3°C$

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Collector-base voltage (Emitter open)	V_{CBO}	$I_C = -10$ µA, $I_E = 0$	−50			V
Collector-emitter voltage (Base open)	V_{CEO}	$I_C = -2$ mA, $I_B = 0$	−50			V
Collector-base cutoff current (Emitter open)	I_{CBO}	$V_{CB} = -50$ V, $I_E = 0$			− 0.1	µA
Collector-emitter cutoff current (Base open)	I_{CEO}	$V_{CE} = -50$ V, $I_B = 0$			− 0.5	µA
Emitter-base cutoff current (Collector open)	I_{EBO}	$V_{EB} = -6$ V, $I_C = 0$			− 0.1	mA
Forward current transfer ratio	h_{FE}	$V_{CE} = -10$ V, $I_C = -5$ mA	80			—
h_{FE} Ratio *	$h_{FE(Small/Large)}$	$V_{CE} = -10$ V, $I_C = -5$ mA	0.50	0.99		—
Collector-emitter saturation voltage	$V_{CE(sat)}$	$I_C = -10$ mA, $I_B = -0.3$ mA			− 0.25	V
Output voltage high-level	V_{OH}	$V_{CC} = -5$ V, $V_B = -0.5$ V, $R_L = 1$ kΩ	−4.9			V
Output voltage low-level	V_{OL}	$V_{CC} = -5$ V, $V_B = -3.5$ V, $R_L = 1$ kΩ			− 0.2	V
Input resistance	R_1		−30%	47	+30%	kΩ
Resistance ratio	R_1 / R_2		0.8	1.0	1.2	—
Transition frequency	f_T	$V_{CB} = -10$ V, $I_E = 1$ mA, f = 200 MHz		80		MHz

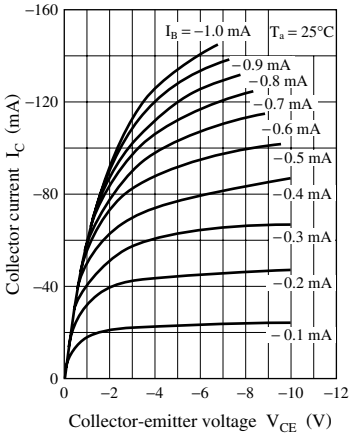
Note) 1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.
2. *: Ratio between 2 elements

Note) The part number in the parenthesis shows conventional part number.

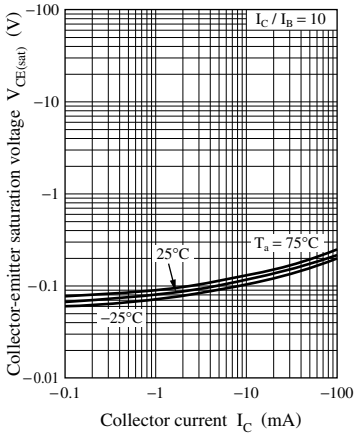
P_T — T_a



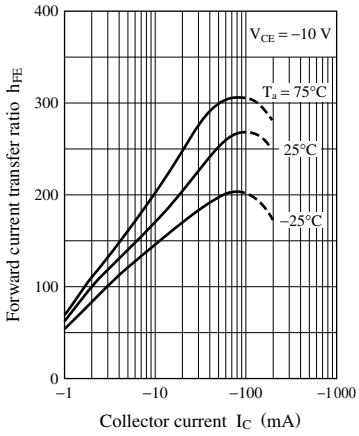
I_C — V_{CE}



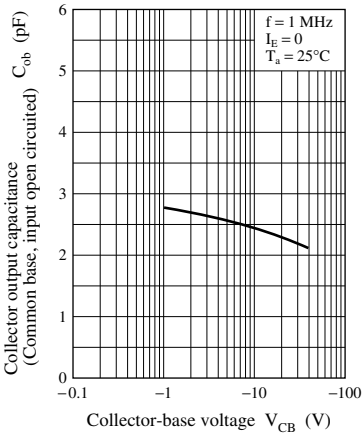
$V_{CE(sat)}$ — I_C



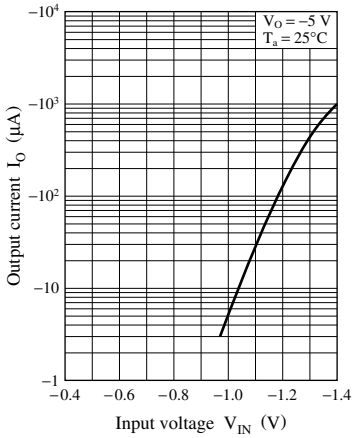
h_{FE} — I_C



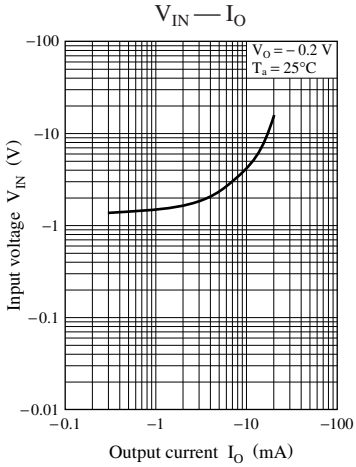
C_{ob} — V_{CB}



I_O — V_{IN}



V_{IN} — I_O



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