VTC Inc.
Value the Customer™

VM347N

4-CHANNEL, CENTER-TAPPED FERRITE, THIN-FILM AND MIG HEAD, READ/WRITE PREAMPLIFIER

PRELIMINARY

July, 1993

FEATURES

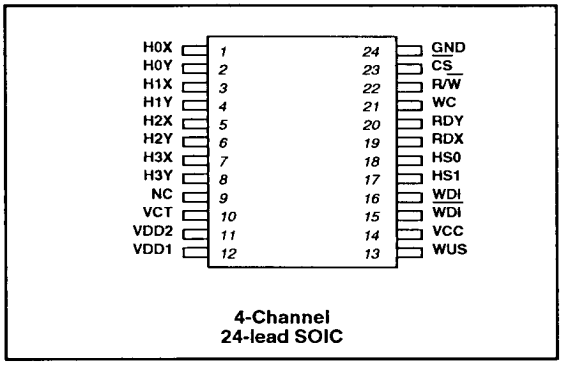
- High-Performance
  - Low Noise = 0.75nV/$\sqrt{Hz}$ typical
  - Input Capacitance = 11 pF typical
  - Read Gain = 120 V/V typical
  - Differential Head Swing = 24 Vp-p minimum
  - I_W Current Range = 10 - 50 mA
- Power Supply Fault Protection
- Enhanced Write to Read Recovery Time
- For Use with Center-Tapped Ferrite or MIG Heads
- Write-Unsafe Detection Circuitry
- Operates on +5V and +12V Power Supplies
- Differential Pseudo ECL Write Data Inputs

DESCRIPTION

The VM347N is a bipolar, monolithic read/write preamplifier circuit, designed for use with up to ten center-tapped ferrite or MIG recording heads. The VM347N offers the same performance functions of the VM327R with the addition of differential Pseudo-ECL write data inputs. System write-to-read recovery is also improved by holding the RDX, RDY common mode outputs constant. The circuit provides a low noise read data path, write current control, write and power supply fault circuitry, and minimum power dissipation in the idle mode.

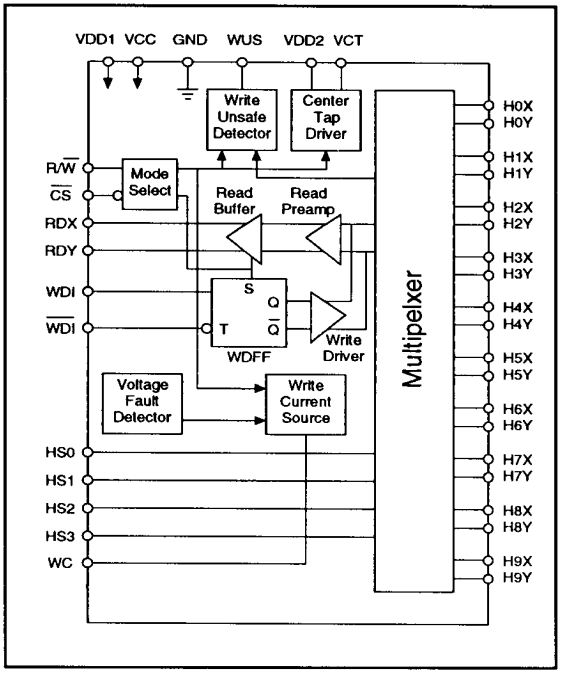
The VM347N is fabricated on VTC's high-performance complementary bipolar process. The circuit has a very fast mode and head select switching characteristics. The VM347N operates on +5V and +12V power supplies and is available in a variety of package options. Please consult factory for availability.

CONNECTION DIAGRAM



4-Channel
24-lead SOIC

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Power Supply:
- V_{DD1} ..... -0.3V to 14V
- V_{DD2} ..... -0.3V to 14V
- V_{CC} ..... -0.3V to 6V

Input Voltages:
- Head Select (HS) ..... -0.3V to V_{CC} + 0.3V
- Write Unsafe (WUS) ..... -0.3V to10V
- Write Data Input (WDI) ..... -0.3V to V_{CC} + 0.3V
- Chip Select ..... -0.3V to V_{CC} + 0.3V
- Read/Write Select (R/W)..... -0.3V to V_{CC} + 0.3V

Output Current:
- Write Current (I_W)..... 120mA
- Read Data (RDX, RDY) 10mA
- Center Tap Current (I_{CT})..... 120mA
- Write Unsafe (WUS) 12mA

Operating Temperature Range ..... 0° to 70°C
Storage Temperature Range ..... -65° to 150°C
Lead Temp. (Soldering 60 Seconds) ..... 300°C
Thermal Characteristics, Θ_{JA}:
- Junction Temperature ..... 150°C
- 24-lead SOIC .....TBD

RECOMMENDED OPERATING CONDITIONS

DC Power Supply Voltage:
- V_{DD1} ..... 12V ± 10%
- V_{DD2} ..... 10V to VDD1
- V_{CC} ..... 5V ± 10%

Head Inductance (L_H) ..... 0.3 to 15µH
R_{CT} Resistor (Note 1) (I_W = 40mA) 130Ω
RDX, RDY Output Current (Read Mode) ..... 0 to .5mA
Write Current Range ..... 10 to 50mA
Operating Junction Temperature ..... 0° to +125°C

Note 1: Resistor (R_{CT}) used to limit power dissipation R_{CT} (Ω) = $5.2/I_W$(A). Use of the R_{CT} resistor may limit the differential voltage swing and increase write current rise times.

CIRCUIT OPERATION

The VM347N has three modes of operation: read, write and idle. In the read mode the circuit functions as a low-noise differential amplifier with selection of up to ten recording heads. In the write mode the circuit operates as a write current switch and provides write fault data protection. In the idle mode both the read amplifier and write driver are disabled and the power dissipation of the circuit is kept to a minimum. Mode selection is controlled by the R/W and CS TTL inputs as shown in Table 1. Both R/W and CS have internal pull-up resistors to prevent an accidental write condition. Head selection is controlled by the HS0, HS1, HS2 and HS3 TTL inputs as shown in Table 2. Each of the head select inputs have internal pull down resistors such that, if all head select inputs are open circuited, selection defaults to head zero.

Write Mode

The write mode configures the VM347N as a current switch and activates the write unsafe (WUS) detection circuitry. The head current is toggled between the X and Y side of a selected head on each high-to-low transitions on pin WDI-WDI (differential write data input). A preceding read operation initializes the write data flip-flop (WDFF) so that upon entering the write mode current flows into the "X" head port.

The write current magnitude is determined by an external resistor connected between the R_{WC} pin and ground. An internally generated 7.1V reference voltage is present at the RWC pin. The magnitude of the write current (0 - pk) is given in Table 3 and is approximated by:

$$I_W = 7.1V/R_{WC} \bullet 20 \quad \text{(factor of 20 is the current gain)}$$

In multiple-device applications, a single R_{WC} resistor may be made common to all devices.

The write unsafe (WUS), open collector output, will give a high level for any of the following unsafe conditions:

- Open Head
- No Write Current
- Read/Idle Mode
- Write Data Frequency to Low
- Head Center-Tap Open

After the fault condition is corrected, two negative transitions are required on WDI to clear the WUS line. The write unsafe circuitry allows a large inductance range and is not dependent on the magnitude of I_W. The VM347N will serve a wide range of head loads and write current values.

To further protect accidental writing to the disk, a voltage fault detection circuit ensures no write current during power loss or power sequencing. If either V_{CC} < 3.7 or V_{DD} < 8.7V, the WC pin is clamped to ground and the write current source is disabled.

Read Mode

The read mode configures the VM347N as a low noise differential amplifier and deactivates the write current generator and write unsafe detection circuitry. The RDX and RDY outputs are emitter followers and are in phase with the "X" and "Y" head ports. These outputs should be AC coupled to the load. The RDX, RDY common-mode voltage is maintained in the write mode, minimizing the transient delay between write-to-read. Thermal offset effects are also minimized to enhance write-to-read recovery when doing a DC erase.

Idle Mode

In the idle mode ($\overline{CS}$ = high level) both the read amplifier and write driver are disabled and the devices power dissipation is minimal. The RDX, RDY outputs are in a high impedance state and may be wire OR'ed for multiple chip usage to a common pulse detector circuit.

Table 1: Mode Select

$\overline{CS}$	$R/\overline{W}$	MODE
0	0	Write
0	1	Read
1	X	Idle

Table 2: Head Select

HS3	HS2	HS1	HS0	HEAD
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9

PIN DESCRIPTIONS

NAME	I/O	DESCRIPTION
HS0-HS3	I*	Head Select Inputs
$\overline{CS}$	I	Chip Select: a low level enables device
$R/\overline{W}$	I*	Read/Write: a high level selects read mode
WUS	O*	Write Unsafe: a high level indicates an unsafe writing condition
WDI, $\overline{WDI}$	I*	Write Data In: negative transition (WDI - $\overline{WDI}$) toggles the head current
H0X-H9X H0Y-H9Y	I / O	X,Y head connections
RDX, RDY	O*	X,Y Read Data: differential read signal outputs
WC		Write Current: used to set the magnitude of the write current
VCT		Voltage Center Tap: voltage source for head center tap
VCC		+5 V
VDD1		+12 V
VDD2		Positive power supply for the center tap voltage source
GND		Ground

* May be wire-OR'ed for multi-chip usage.

Table 3: External Resistor vs. Write Current

External resistor vs. DC write current I_W into the selected head terminal X or Y with V_{CT} shorted only to the respective X or Y terminal.

External Resistor R_{WC} (kΩ)	Write Current I_W (mA)
14.81	10
7.20	20
4.75	30
3.52	40
2.87	50

$$I_{FLUX} = I_W\left(\frac{R_D}{R_H + R_D}\right)$$

Note: Effective current I_{FLUX} generated in the magnetic head is related to I_W by the expression:

Where R_H equals the full coil resistance of a center-tapped ferrite head and R_D is the damping resistor connected internally or externally between the X and Y terminals. Nominal internal resistance on VM347N is 650Ω.

DC CHARACTERISTICS Unless otherwise specified, recommended operating conditions apply.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
POWER SUPPLY						
Positive Supply Current R_{WC} = 3517Ω	I_{DD}	Read Mode		21	29	mA
		Write Mode		18 + I_W	23 + I_W	
		Idle Mode		6	9	
	I_{CC}	Read Mode		19	26	mA
		Write Mode		17	21	
		Idle Mode		8	11	
Power Dissipation T_J = 125°C, R_{WC} = 3517Ω	P_D	Idle Mode		115	180	mW
		Read Mode		350	525	
		Write Mode I_W = 40mA, R_{CT} = 130Ω		750	900	
		Write Mode I_W = 40mA, R_{CT} = 0Ω		625	725	
DIGITAL TTL INPUTS: $\overline{CS}$, R/$\overline{W}$, HS, WDI						
Input High Voltage	V_{IH}		2		V_{CC} + 0.3	V
Input Low Voltage	V_{IL}		-0.3		0.8	V
Input High Current	I_{IH}	V_{IH} = 2.0V, V_{CC} = 5.5V			20	µA
Input Low Current	I_{IL}	V_{IL} = 0.4V, V_{CC} = 5.5V	-0.4			mA
PSEUDO ECL INPUTS WDI, $\overline{WDI}$						
WDI, $\overline{WDI}$ Input High Voltage	V_{IH}		V_{CC} -1.0		V_{CC} - 0.7	V
WDI, $\overline{WDI}$ Input Low Voltage	V_{IL}		V_{CC} -1.9		V_{CC} - 1.6	V
WDI, $\overline{WDI}$ Input High Current	I_{IH}	V_{IH} = V_{CC} - 0.7V			100	µA
WDI, $\overline{WDI}$ Input Low Current	I_{IL}	V_{IH} = V_{CC} - 1.6V			80	µA
WUS OUTPUT						
Low Voltage	V_{OL}	I_{OL} = 8 mA (Safe)			0.5	V
High Current	I_{OH}	V_{OH} = 5V (Unsafe)			100	µA

READ CHARACTERISTICS Unless otherwise specified, recommended operating conditions apply.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Differential Voltage Gain	A_V	V_{IN}= 1mVrms, f = 500KHz R_L (RDX,RDY) = 1kΩ	100		140	V/V
Dynamic Range	DR	DC Input Voltage where AC Gain Falls 10%, $V_{IN} = V_{DC}$ + 0.5mVp-p f = 500KHz	-2		2	mV
Bandwidth (- 3 dB)	BW	V_{IN} = 1mVrms, $Z_S < 5Ω$	30			MHz
Input Noise Voltage	e_{in}	L_H = 0, R_H = 0, BW = 15MHz		0.75	1.0	$nV/\sqrt{Hz}$
Differential Input Capacitance	C_{IN}	f = 5MHz		9	13	pF
Differential Input Resistance	R_{IN}	VM327R	400		800	Ω
Input Current	I_{IN}	$V_{CM} = V_{CT}$ + 100mVp-p, f = 5MHz			65	µA
Common Mode Rejection Ratio	CMRR	$V_{CM} = V_{CT}$ + 100mVp-p, f = 5MHz	50			dB
Power Supply Rejection Ratio	PSRR	V_{DD} or V_{CC}= 100mVp-p, f = 5MHz	45			dB
Channel Separation	CS	V_{IN} = 100mVp-p, f = 5MHz Three channels driven, selected channel measured	45			dB
Output Offset Voltage	V_{OS}		-300		300	mV
Common Mode Output Voltage	V_{OCM}		2		3	V
Single-Ended Output Resistance	R_{SEO}				30	Ω
Center-Tap Voltage	V_{CT}			4.2		V

WRITE CHARACTERISTICS Unless otherwise specified, recommended operating conditions apply, I_W = 40mA, L_H = 150nH, R_H = 20Ω, single ended, f_{DATA} = 5MHz.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Write-Current Range	I_W	(See table 3)	10		50	mA
Differential Head Voltage	V_{DH}	L_H = 8.8µH, R_H = 0Ω	12			Vpk
Unselected Head Current	I_{UH}				2	mAp-p
Current Gain	A_I			20		mA/mA
Head Current Propagation Delay	t_{PD}	L_H = 0µH, R_H = 0, 50% WDI to 50% I_W		11	20	ns
Rise/Fall Time	t_r , t_f	L_H = 0µH, R_H = 0, 10% to 90%		3	8	ns
Write Current Tolerance	ΔI_W	R_{WC} = 3517Ω	36.8	40	44.0	mA
Differential Output Resistance	R_{OUT}	VM327R	500		900	Ω
Differential Output Capacitance	C_{OUT}				15	pF
Center-Tap Voltage	V_{CT}			10		V

SWITCHING CHARACTERISTICS Unless otherwise specified, recommended operating conditions apply.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Read-to-Write Switching Delay	t_{RW}	50% of R/W to 90% of Write Output Envelope			500	ns
Write-to-Read Switching Delay	t_{WR}	50% of R/W to 90% of 100mVp-p RDX, RDY Envelope			500	ns
Idle-to-Write Switching Delay	t_{IW}	50% of CS to 90% of Write Output Envelope			500	ns
Idle-to-Read Switching Delay	t_{IR}	50% of CS to 90% of 100mVp-p RDX, RDY Envelope			500	ns
Write-to-Idle Switching Delay	t_{WI}	50% of CS to 10% of Write Output Envelope			500	ns
Read-to-Idle Switching Delay	t_{RI}	50% of CS to 10% of RDX, RDY Envelope			500	ns
Head Select Switching Delay	t_{HS}	50% of HS Transition to 90% of 100mVp-p RDX, RDY Envelope from Selected Head			500	ns
Write Unsafe Delay Safe-to-Unsafe	t_{D1}	Gate WDI. Measure from 50% of Last Data Pulse to 50% WUS.	1.6		8	µs
Write Unsafe Delay Unsafe-to-Safe	t_{D2}	Gate WDI. Measure from 50% of Falling Edge of First Data Pulse to 50% WUS			1	µs
Rise/Fall Time	t_r , t_f	L_H = 0 10% to 90%		3	10	ns
Head Current Prop. Delay	t_{D3}	L_H = 0		15	30	ns
Asymmetry	A_S	WDI has 50% Duty, Cycle and 1ns Rise/Fall Time, L_H = 0		0.1	1	ns

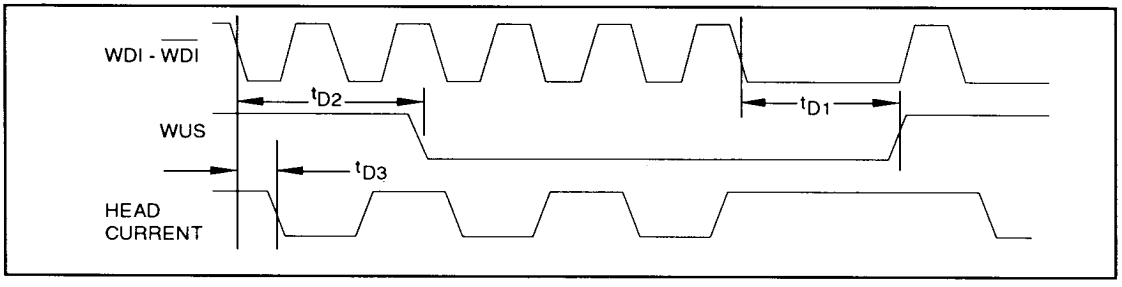


Figure 1: Write Mode Timing Diagram