2 MEG x 8/1 MEG x 16
SMART 3 EVEN-SECTORED FLASH

FLASH MEMORY MT28F160S3

FEATURES

- x8/x16 organization
- Thirty-two 64KB erase blocks
- V_{CC} and V_{PP} voltages:
  - 3V–3.6V V_{CC} operation, 75ns (MIN) access time
  - 2.7V–3.6V V_{CC} operation, 100ns (MIN) access time
  - 2.7V–5V I/O capable*
  - 2.7V–3.6V, or 5V V_{PP} application programming
- Enhanced data protection feature with V_{PP}
  - Flexible sector locking
  - Sector erase/program lockout during power transition
- Industry-standard pinout
- Inputs and outputs that are fully TTL-compatible
- Common flash interface (CFI) and scalable command set (SCS)
- Deep power-down: I_{CC} = 15µA
- Automatic write and erase algorithm
- 2.7µs per byte effective programming time using write buffer
- Automatic suspend options:
  - BLOCK ERASE SUSPEND-to-READ
  - BLOCK ERASE SUSPEND-to-PROGRAM
  - PROGRAM SUSPEND-to-READ

OPTIONS MARKING

- Timing
  - 75ns access -75
  - 100ns access -10
- Package
  - Plastic 56-pin TSOP Type 1 RG

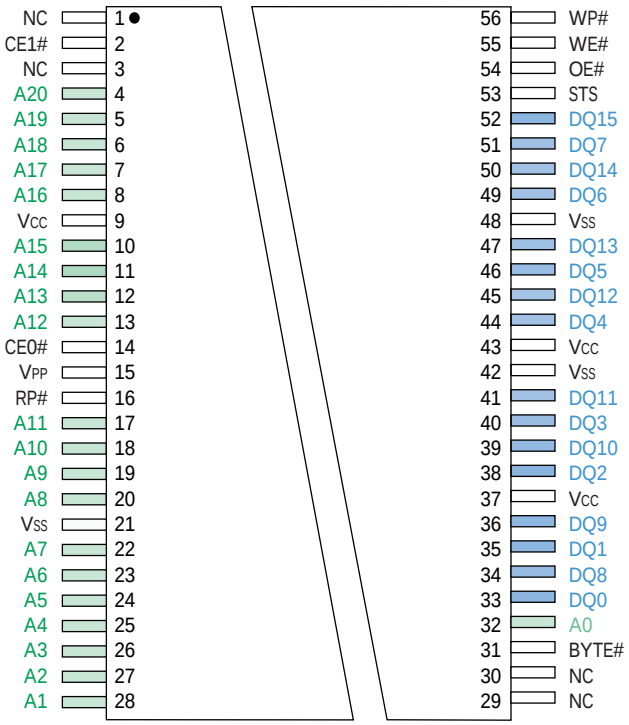
*5V I/O is a manufacturing option. Contact factory for availability.

Part Number Example:

MT28F160S3RG-10

PIN ASSIGNMENT (Top View)

56-Pin TSOP



NOTE: The # symbol indicates signal is active LOW.

GENERAL DESCRIPTION

The MT28F160S3 is a nonvolatile, electrically block-erasable (flash), programmable, memory containing 16,777,216 bits organized as 2,097,152 bytes (8 bits) or 1,048,576 words (16 bits). The 16Mb device is organized as thirty-two 64KB erase blocks and features in-system block locking that is either lockable or unlockable, selectively and individually.

The MT28F160S3 also features a common flash interface (CFI) that permits software algorithm for the device. The software is device-independent and JEDEC ID-independent, with forward and backward compatibility. Additionally, the scalable command set (SCS) allows a single, simple software driver in all host systems to work with all SCS-compliant flash memory devices. The SCS provides the fastest system/device data transfer rates and minimizes the device and system-level implementation costs.

GENERAL DESCRIPTION (continued)

To achieve optimization of the processor-memory interface, the device accommodates V_{PP}, which is either switchable during block erase, program, or lock bit configuration or is hardwired to V_{CC}, depending on the application. V_{PP} is treated as an input pin to enable erasing, programming, and block locking. When V_{PP} is lower than the write lockout voltage, V_{LKO}, all program functions are disabled.

Each block of the device can be independently erased 100,000 times. In addition, program suspend mode allows system software to suspend programming to read data from other flash memory locations.

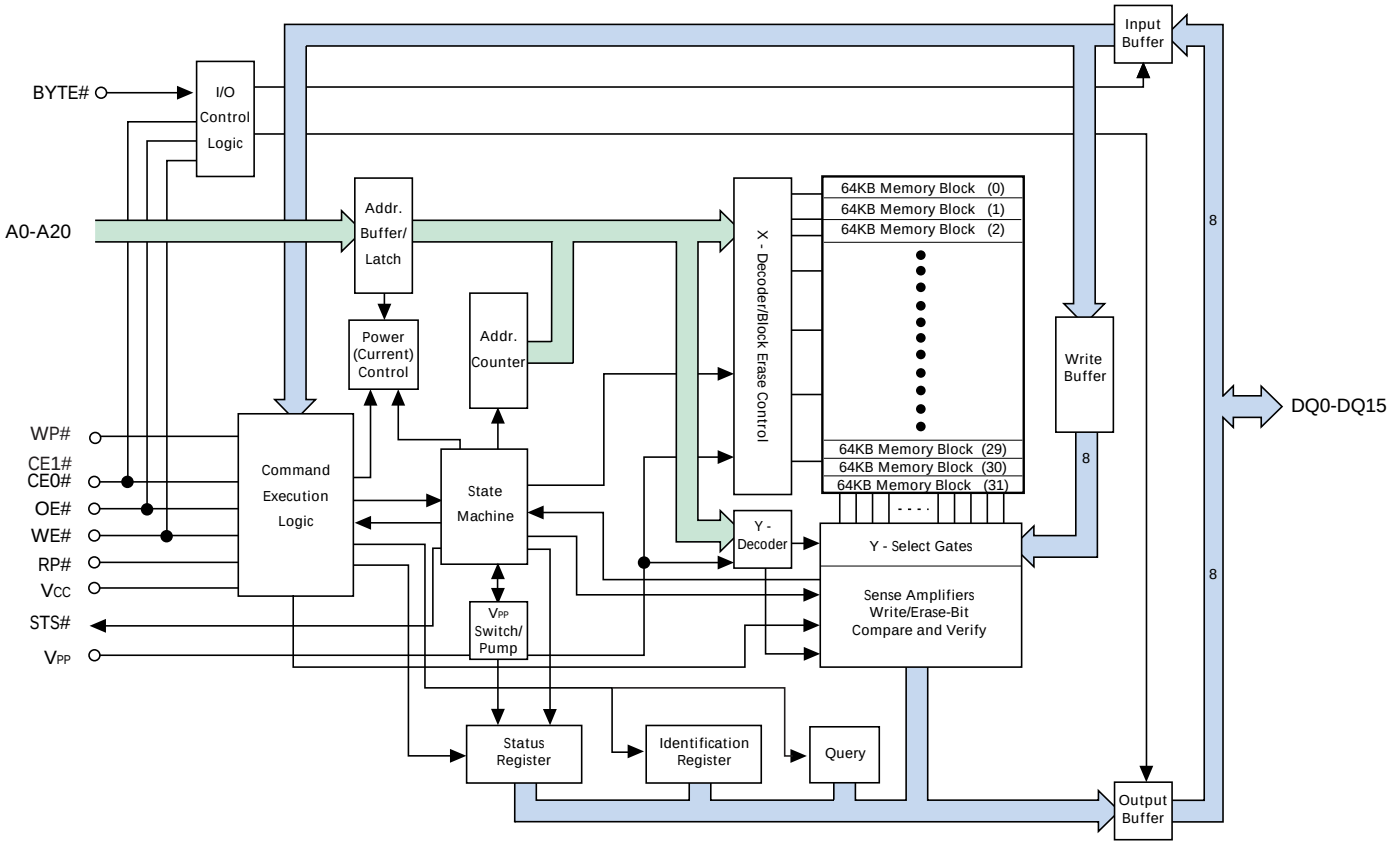
Additionally, the device offers individual block locking, which is controlled through a combination of block lock bits. Block erase suspend allows the reading of data from or the programming of data to any other block.

The status pin (STS) provides a logic signal output that acts as an additional indicator of internal state machine (ISM) activity. This status indicator minimizes both CPU overhead and system power consumption. In the default mode, it acts as a RY/BY# pin. When LOW, STS indicates that the ISM is performing a BLOCK ERASE, PROGRAM, or LOCK BIT CONFIGURATION. When HIGH, STS indicates that the ISM is ready for a new command.

Two chip enable pins (CE#) are used for enabling and disabling the device to activate the control logic, input buffer, decoders, and sense amplifiers.

The BYTE# pin allows x8 or x16 READs/WRITEs to be selected. BYTE# at logic LOW selects an 8-bit mode using address A0 to select between the low byte and the high byte. BYTE# at logic HIGH enables 16-bit operation.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

56-PIN TSOP NUMBERS	SYMBOL	TYPE	DESCRIPTION
55	WE#	Input	Write Enable: Determines if a given cycle is a WRITE cycle. If WE# is LOW, the cycle is either a WRITE to the command execution logic (CEL) or to the memory array.
14, 2	CE0#, CE1#	Input	Chip Enable: With CE0# or CE1# HIGH, the device is deselected and power consumption is reduced to standby levels. Both CE0# and CE1# must be LOW to select the device. All timing specifications are the same for these two signals.
16	RP#	Input	Reset/Power-Down: When LOW, RP# clears the status register, sets the ISM to the array read mode, and places the device in deep power-down mode. All inputs, including CE0#/CE1#, are "Don't Care," and all outputs are High-Z. RP# must be held at V_{IH} during all other modes of operation.
54	OE#	Input	Output Enable: Enables data ouput buffers when LOW. When OE# is HIGH, the output buffers are disabled.
56	WP#	Input	Write Protect: Controls the lock down function of the flexible locking feature. When LOW, locked blocks cannot be erased or programmed, and block lock bits may not be altered.
32, 28, 27, 26, 25, 24, 23, 22, 20, 19, 18, 17, 13, 12, 11, 10, 8, 7, 6, 5, 4	A0-A20	Input	Address inputs during READ and WRITE operations. A0 is only used in the x8 mode.
31	BYTE#	Input	Byte Enable: When LOW, BYTE# places the device in the x8 mode. When HIGH, BYTE# places the device in the x16 mode and ignores the A0 input buffer. Address A1 then becomes the lowest order address.
15	V_{PP}	Input	Programming Voltage: Necessary voltage for erasing blocks, programming data, or configuring lock bits. Typically, V_{PP} is connected to V_{CC}.
33, 35, 38, 40, 44, 46, 49, 51, 34, 36, 39, 41, 45, 47, 50, 52	DQ0-DQ15	Input/ Output	Data I/O: Data output pins during any READ operation or data input pins during a WRITE.
53	STS	Output	Status: Indicates the status of the ISM. When configured in its pulse mode, it can pulse to indicate program and/or erase completion. When configured in level mode (default), it acts as a RY/BY# pin.
9, 37, 43	V_{CC}	Supply	Supply Power: 2.7V–3.6V.
21, 42, 48	V_{SS}	Supply	Ground.
1, 3, 29, 30	NC	–	No Connect: These pins may be driven or left unconnected.

OPERATION OVERVIEW

The MT28F10S3 device has an on-chip internal state machine (ISM) for block erase and programming management, and lock bit configuration. The device defaults to read array mode upon initial device power-up or return from deep power-down mode. The external memory control pins allows array read, standby, and output disable operations. Read array, status register, query, and identifier codes can be accessed through the command execution logic (CEL), which is independent of the V_{PP} voltage. Proper programming voltage on V_{PP} enables successful block erasure, program, and lock bit configuration. All block erase, program, and lock bit configuration functions are accessed via the CEL and verified through the status register.

Commands are written with standard microprocessor write timings. The CEL contents become an input to the ISM that controls the block erase, programming, and lock bit configuration. The ISM regulates the internal algorithms, including pulse repetition, internal verification, and data margining. During WRITE cycles, addresses and data are internally latched. Writing the appropriate command outputs array data, identifier codes, or status register data. Interface software that initiates block erase, programming, and lock bit configuration can be stored in any block. During memory update, this code is transferred to and executed from the system RAM. Upon successful completion of an update, READs are again possible via the READ ARRAY command. Block erase suspend allows system software to suspend a block erase to read data from, or program data to, any other block. Program suspend allows system software to suspend a program to read data from any other flash memory location.

DATA PROTECTION

The system designer may choose to make the V_{PP} power supply switchable or hardwired to $V_{PPH1/2/3}$, depending on the application. Using either configuration will enable designers to optimize the processor-memory interface.

When V_{PP} is lower than V_{PPLK}, memory contents are fixed. When V_{PP} is HIGH, the two-step block erase, program, or lock bit configuration command sequences provide data protection. When V_{CC} voltage is below the write lockout voltage V_{LKO}, or when RP# is at V_{IL}, all WRITE functions are disabled. The device can lock blocks to provide additional protection from unwanted code or data changes.

BUS OPERATION

All bus cycles to or from the flash memory conform to standard microprocessor bus cycles.

READ

Reading the device is independent of the applied V_{PP} voltage and users can obtain block information, query information, identifier codes, and status register settings. To read, the device must be first placed into the desired read mode. This can be done by writing the appropriate read mode command (read array, query, read identifier codes, or read status register) to the CEL. The device will automatically reset to read array mode upon initial device power-up or after exit from deep power-down mode. Control pins manage the data flow in and out of the component. CE0#, CE1#, and OE# must be driven active to obtain data at the outputs. CE0# and CE1# are the device selection controls, and when both are active, they enable the selected memory device. OE# is the data output (DQ0–DQ15) control. When active, it drives the selected memory data onto the I/O bus. Both WE# and RP# must be at V_{IH}. The READ Operations timing diagram illustrates a READ cycle.

OUTPUT DISABLE

When OE# is at a logic HIGH level (V_{IH}), the device outputs are disabled.

STANDBY

When the device is in standby mode and CE0# or CE1# are at a logic HIGH level (V_{IH}), the device power consumption is substantially reduced. DQ0-DQ15 (or DQ0-DQ7 in x8 mode) outputs are High-Z, independent of OE#. When deselected during block erase, programming, or lock bit configuration, the device continues its operation and consumes active power until operation completion.

DEEP POWER-DOWN

The deep power-down mode occurs when RP# is at V_{IL}. RP# LOW deselects the memory, places output drivers in High-Z, and turns off all internal circuits. RP# must be held LOW for time $^{t}PLPH$. A period of $^{t}PHQV$ is required after power-down before initial memory access outputs are valid. After this wake-up interval, normal operation is resumed. The CEL resets to read array mode, and the status register is set to 80h.

RP# LOW will abort the operation during block erase, programming, or lock bit configuration modes. STS in RY/BY# mode remains LOW until the RESET operation is complete. The previously altered memory contents are no longer valid since the data may be partially corrupted after programming or partially altered after an erase or lock bit configuration. A period of $^{t}PHWL$ is required after RP# goes to logic HIGH (V_{IH}) before another command can be written. RP# must be

asserted during system reset. When the system is out of reset mode, it expects to read from the flash memory. Automated flash memories provide status information when accessed during block erase, programming, or lock bit configuration modes. If a CPU reset occurs with no flash memory reset, the proper CPU initialization may not occur because the flash memory may be providing status information instead of array data. Micron's flash memories allow proper CPU initialization following a system reset through the use of the RP# input. In this application, RP# is controlled by the same system CPU RESET# signal.

READ QUERY OPERATION

READ QUERY operation provides block status, CFI ID string, system interface, device geometry, and extended query information.

READ IDENTIFIER CODES OPERATION

This operation outputs the manufacturer code, device code, and block lock configuration codes for each block configuration (see Figure 2). The system software can automatically match the device with its proper algorithms using the manufacturer and device codes.

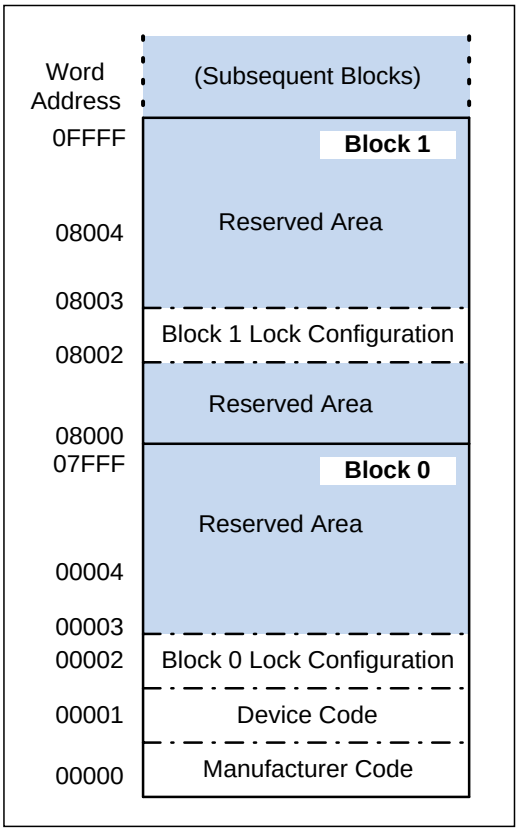
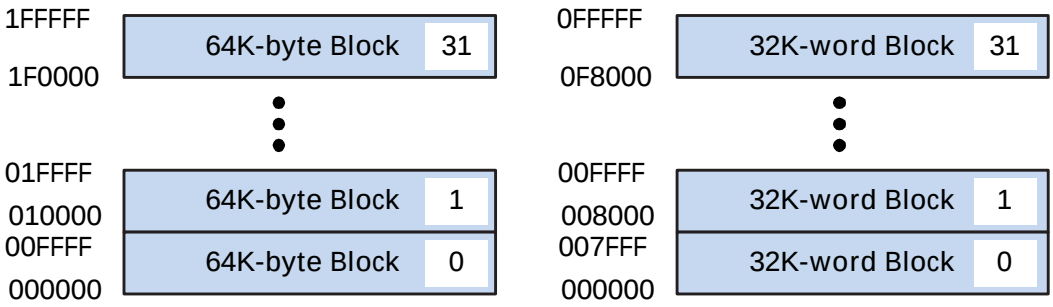


Figure 2
Device Identifier for Code Memory Map



Byte-Wide (x8) Mode **Word-Wide (x16) Mode**

Figure 1
Memory Map

WRITE

WRITE commands to the CEL enables reading the device data, query, identifier codes, and inspection and clearing of the status register. In addition, when $V_{PP} = V_{PPH1/2/3}$, block erasure, programming, and lock bit configuration can also be performed. The BLOCK ERASE command requires the command and address within the block to be erased. The BYTE/WORD WRITE command requires writing the command and address of the desired location. The CLEAR BLOCK LOCK BITS command requires the command and an address within the whole device. SET BLOCK LOCK BITS commands require the command and address within the block to be locked.

The CEL is written when CE0#, CE1# (CEx#), and WE# are active and OE# = V_{IH}. The address and data for a command execution are latched on the rising edge of WE# or CEx#, whichever goes HIGH first. Standard microprocessor write timings are used. The WRITE Operations timing diagram illustrates a WRITE operation.

COMMAND DEFINITIONS

V_{PP} voltage ≤ V_{PPLK} allows READ operations from the status register, identifier codes, or memory blocks. Placing $V_{PPH1/2/3}$ on V_{PP} enables successful BLOCK ERASE, PROGRAMMING, and LOCK BIT CONFIGURATION operations. To select device operations, one must write specific commands into the CEL. Table 2 defines these commands.

Table 1
Bus Operation

MODE	RP#	CE0#	CE1#	OE#[1]	WE[1]	ADDRESS	V_{PP}	DQs[2]	STS[3]	NOTES
Read	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	X	X	D_{OUT}	X	5, 6
Output Disable	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	X	High-Z	X	
Standby	V_{IH}	V_{IL} V_{IH} V_{IH}	V_{IH} V_{IL} V_{IH}	X	X	X	X	High-Z	X	
Reset/Power-Down Mode	V_{IL}	X	X	X	X	X	X	High-Z	High-Z[4]	7
Read Identifier Codes	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	See Figure 1	X	D_{OUT}	High-Z[4]	8
Read Query	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	See Table 5	X	D_{OUT}	High-Z[4]	9
Write	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	X	V_{PPH1} V_{PPH2} V_{PPH3}	D_{IN}	X	3, 10, 11

NOTE:
1. OE# = V_{IL} and WE# = V_{IL} concurrently is an undefined state and should not be attempted.
2. DQ refers to DQ0–DQ7 if BYTE# is LOW and DQ0–DQ15 if BYTE# is HIGH.
3. STS in level RY/BY# mode (default) is V_{OL} when the ISM is executing internal block erase, programming, or lock bit configuration algorithms. It is V_{OH} when the ISM is not busy, in block erase suspend mode (with programming inactive), program suspend mode, or deep power-down mode.
4. High-Z will be V_{OH} with an external pull-up resistor.
5. Refer to DC Characteristics table. When $V_{PP} \le V_{PPLK}$, memory contents can be read, but not altered.
6. "X" can be V_{IL} or V_{IH} for control and address input pins and V_{PPLK} or $V_{PPH1/2/3}$ for V_{PP}. See the DC Characteristics table for V_{PPLK} and $V_{PPH1/2/3}$ voltages.
7. RP# at GND ± 0.2V ensures the lowest deep power-down current.
8. See Read Identifier Codes Command section for read identifier code data.
9. See Read Query Mode section for read query data.
10. Command writes involving block erase, write, or lock bit configuration are reliably executed when $V_{PP} = V_{PPH1/2/3}$ and $V_{CC} = V_{CC1/2}$ (see Write/Erase Current Drain table).
11. Refer to Table 2 for valid D_{IN} during a WRITE operation.

Table 2
Command Set Definitions[1]

COMMAND	SCALABLE OR BASIC COMMAND SET[2]	BUS CYCLES REQ'D	FIRST BUS CYCLE			SECOND BUS CYCLE			NOTES
			OPER[3]	ADDR[4]	DATA[5,6]	OPER[3]	ADDR[4]	DATA[5,6]	
READ ARRAY	SCS/BCS	1	WRITE	X	FFh				
READ IDENTIFIER	SCS/BCS	≥2	WRITE	X	90h	READ	IA	ID	7
READ QUERY	SCS	≥2	WRITE	X	98h	READ	QA	QD	
READ STATUS REGISTER	SCS/BCS	2	WRITE	X	70h	READ	X	SRD	
CLEAR STATUS REGISTER	SCS/BCS	1	WRITE	X	50h				
WRITE-TO-BUFFER	SCS	>2	WRITE	BA	E8h	WRITE	BA	N	8, 9, 10
WORD/BYTE PROGRAM	SCS/BCS	2	WRITE	X	10h/40h	WRITE	PA	PD	11, 12
BLOCK ERASE	SCS/BCS	2	WRITE	X	20h	WRITE	BA	D0h	10, 11
BLOCK ERASE, WORD/ BYTE PROGRAM SUSPEND	SCS/BCS	1	WRITE	X	B0h				11
BLOCK ERASE, WORD/ BYTE PROGRAM RESUME	SCS/BCS	1	WRITE	X	D0h				11
STS PIN CONFIGURATION	SCS	2	WRITE	X	B8h	WRITE	X	CC	
SET BLOCK LOCK BIT	SCS	2	WRITE	X	60h	WRITE	BA	01h	13
CLEAR BLOCK LOCK BITS	SCS	2	WRITE	X	60h	WRITE	X	D0h	14
FULL CHIP ERASE	SCS	2	WRITE	X	30h	WRITE	X	D0h	10

NOTE:
1. Commands other than those shown above are reserved for future use and should not be used.
2. The SCS is compatible with the Intel® Extended Command Set.
3. Bus operations are defined in Table 1.
4. X = Any valid address within the device
   BA = Address within the block being erased or locked
   IA = Identifier code address; see Table 11
   QA = Query database address
   PA = Address of memory location to be programmed
5. ID = Data read from query database
   SRD = Data read from status register; see Table 14 for a description of the status register bits
   PD = Data to be programmed at location PA; data is latched on the rising edge of WE#
   CC = Configuration code; see Table 13
6. The upper byte of the data bus (DQ8–DQ15) during command writes is a "Don't Care" in x16 operation.
7. Following the READ IDENTIFIER CODES command, READ operations access manufacturer, device, and block lock codes. See Read Identifier Codes Command section for read identifier code data.
8. After the WRITE-to-BUFFER command is issued, check the XSR to make sure a write buffer is available.
9. N = byte/word count argument such that the number of bytes/words to be written to the input buffer = N + 1. (N = 0 is one byte/word length, and so on.) WRITE-to-BUFFER is a multicycle operation, where a byte/word count of N + 1 is written to the correct memory address (WA) with the proper data (WD). The CONFIRM command (D0h) is expected after exactly N + 1 WRITE cycles; any other command at that point in the sequence aborts the buffered WRITE. Writing a byte/word count outside the buffer boundary causes unexpected results and should be avoided.
10. The WRITE-to-BUFFER , BLOCK ERASE, or FULL CHIP ERASE operation does not begin until a CONFIRM command (D0h) is issued. Confirm also reactivates suspended operations.
11. If a block is locked (i.e., the block's lock bit is set to "0"), WP# must be at V_{IH} in order to perform BLOCK ERASE, PROGRAM, and SUSPEND operations. Attempts to issue a BLOCK ERASE, PROGRAM, or SUSPEND operation to a locked block while WP# is V_{IL} will fail.
12. Either 40h or 10h are recognized by the ISM as the byte/word program setup.
13. A block lock bit can be set only while WP# is V_{IH}.
14. WP# must be at V_{IH} to clear block lock bits. The clear BLOCK LOCK BITS operation simultaneously clears all block lock bits.

READ ARRAY COMMAND

Upon initial device power-up and exiting the deep power-down mode, the default state is the read array mode. This mode is also initiated by writing the READ ARRAY command to the device. The device remains available for READs until another command is written. Once the ISM has started block erase, program, or lock bit configuration, the device will not recognize the READ ARRAY command until the ISM completes its operation, unless the ISM is suspended via an ERASE SUSPEND or PROGRAM SUSPEND command. The READ ARRAY command functions independently of the V_{PP} voltage.

READ QUERY MODE COMMAND

This section is related to the definition of the data structure returned by the CFI QUERY command. System software can access this structure to gain critical information such as block size, density, x8/x16 configuration, and electrical specifications. Once this information has been obtained, the software will know which command sets can be used to enable flash writes, block erases, and otherwise control the flash component. The query belongs to an overall specification for multiple command set and control interface descriptions called common flash interface (CFI).

QUERY STRUCTURE OUTPUT

The query data structure allows system software to gain critical information for controlling the flash device. The device's CFI-compliant interface allows the host system to access query data.

Query data is always located on the lowest-order data outputs (DQ0-DQ7) only. The numerical offset value is the address relative to the maximum bus width supported by the device. Since the maximum bus width is x16, the query table device starting address is a 10h word address. (See Tables 3 and 4.)

For x16 organization, the first two bytes of the query structure, "Q" and "R" in ASCII, appear on the low byte at word addresses 10h and 11h. This CFI-compliant device outputs 00h data on upper bytes, thus making the device output ASCII "Q" on the low byte (DQ0-DQ7) and 00h on the high byte (DQ8-DQ15).

Because the device is either x8 or x16 capable, the x8 data is still presented in word-relative (16-bit) addresses. However, the "fill data" (00h) will be driven by the upper bytes in the x16 mode. As in x16 mode, the byte address (A0) is ignored for query output so that the "odd byte address" (A0 HIGH) repeats the "even byte address" data (A0 LOW). Therefore, in x8 mode, using byte addressing, the device will output the sequence "Q, Q, R, R, Y, Y," and so on, beginning at byte-relative address 20h. Note that the least significant data byte is presented at the lower address, and the most significant data byte is presented at the higher address.

Table 3
Summary of Query Structure Output

DEVICE TYPE/ MODE	WORD ADDRESSING			BYTE ADDRESSING		
	LOCATION	QUERY DATA		LOCATION	QUERY DATA	
		HEX	ASCII		HEX	ASCII
x16 device/ x16 mode	10h 11h 12h	0051h 0052h 0059h	"Q" "R" "Y"	20h 21h 22h	51h 00h 52h	"Q" null "R"
x16 device/ x8 mode	N/A[1]	N/A		20h 21h 22h	51h 51h 52h	"Q" "Q" "R"

NOTE: 1. The system must drive the lowest order addresses to access all the device's array data when the device is configured in x8 mode. Therefore, word addressing where lower addresses are not toggled by the system is "Not Applicable" for x8-configured devices.

Table 4
Example of Query Structure Output

DEVICE ADDRESS	WORD ADDRESSING: QUERY DATA		BYTE	BYTE ADDRESSING: QUERY DATA	
A16–A1	DQ15–DQ0		A7–A0	DQ7–DQ0	
0010h	0051h	"Q"	20h	51h	"Q"
0011h	0052h	"R"	21h	51h	"Q"
0012h	0059h	"Y"	22h	52h	"R"
0013h	P_IDLO	PrVendor	23h	52h	"R"
0014h	P_IDHI	ID #	24h	59h	"Y"
0015h	PLO	PrVendor	25h	59h	"Y"
0016h	PHI	TblAdr	26h	P_IDLO	PrVendor
0017h	A_IDLO	AltVendor	27h	P_IDLO	ID #
0018h	A_IDHI	ID #	28h	P_IDHI	"
...	...		...	...	ID #

QUERY STRUCTURE OVERVIEW

The QUERY command allows the flash component to display the CFI query structure. Table 5 summarizes the structure subsections and address locations.

Table 5
Query Structure[1]

OFFSET	SUBSECTION NAME	DESCRIPTION
00h		Manufacturer code
01h		Device code
(BA+2)h[2]	Block Status Register	Block-specific information
04-0Fh	Reserved	Reserved for vendor-specific information
10h	CFI Query Identification String	Command set ID and vendor data offset
1Bh	System Interface Information	Device timing and voltage information
27h	Device Geometry Definition	Flash device layout
P[3]	Primary Micron-Specific Extended Query Table	Vendor-defined additional information specific to the primary vendor algorithm

NOTE:
1. Refer to the Query Structure Output section and Table 3 for the detailed definition of offset address as a function of device word width and mode.
2. BA = The beginning location of a block address (i.e., 008000h) is the beginning location of block 1 when the block size is 32K-word.
3. Offset 15 defines "P," which points to the Primary Extended Query Table.

BLOCK STATUS REGISTER

The block status register indicates the completion of an ERASE operation, or whether a given block is either locked or can be accessed for PROGRAM or ERASE operations. Block erase status (BSR1) allows system software to recognize the success of the last BLOCK ERASE operation. After power-up, BSR1 can be used to verify that the V_{CC} supply was not accidentally removed during an ERASE operation. By issuing another ERASE operation to the block, this bit can be reset. Within each block, the block status register is accessed from word address 02h.

CFI QUERY IDENTIFICATION STRING

The identification string verifies whether the device supports the CFI specification. Additionally, it indicates the specification version and vendor-specified command set(s) to be supported.

Table 6
Block Status Register

OFFSET	LENGTH (BYTES)	DESCRIPTION	x16 MODE
(BA + 2)h[1]	01h	Block Status Register	BA + 2: 0000h or 0001h
		BSR0 = Block Lock Status 1 = Locked 0 = Unlocked	BA + 2 (bit 0): 0 or 1
		BSR1 = Block Erase Status 1 = Last ERASE operation did not complete successfully 0 = Last ERASE operation completed successfully	BA + 2 (bit 1): 0 or 1
		BSR2–BSR7 = Reserved for future use	BA + 2 (bits 2-7): 0

NOTE: 1. BA = The beginning location of a block address (i.e., 008000h is the beginning location of block 1 in word mode.)

Table 7
CFI Identification

OFFSET	LENGTH (BYTES)	DESCRIPTION	VALUE
10h	03h	Query-unique ASCII string "QRY"	10: 0051h 11: 0052h 12: 0059h
13h	02h	Primary vendor command set and control interface ID code 16-bit ID code for vendor-specified algorithms	13: 0001h 14: 0000h
15h	02h	Address for primary algorithm extended query table Offset value = P = 31h	15: 0031h 16: 0000h
17h	02h	Alternate vendor command set and control interface ID code Second vendor-specified algorithm supported Note: 0000h means none exist	17: 0000h 18: 0000h
19h	02h	Address for secondary algorithm extended query table Note: 0000h means none exist	19: 0000h 1A: 0000h

SYSTEM INTERFACE INFORMATION

Table 8 provides useful information to optimize the system interface software.

Table 8
System Interface Information

OFFSET	LENGTH (BYTES)	DESCRIPTION	VALUE
1Bh	01h	V_{CC} Logic Supply Minimum Program/Erase Voltage Bits 7–4 BCD volts Bits 3–0 BCD 100mV	1B: 0027h
1Ch	01h	V_{CC} Logic Supply Maximum Program/Erase Voltage Bits 7–4 BCD volts Bits 3–0 BCD 100mV	1C: 0055h
1Dh	01h	V_{PP} [Programming] Supply Minimum Program/Erase Voltage Bits 7–4 HEX volts Bits 3–0 BCD 100mV	1D: 0027h
1Eh	01h	V_{PP} [Programming] Supply Maximum Program/EraseVoltage Bits 7–4 HEX volts Bits 3–0 BCD 100mV	1E: 0055h
1Fh	01h	Typical Timeout per Single Byte/ Word Program, 2^n µsec	1F: 0003h (2^3 = 8)
20h	01h	Typical Timeout for Max. Buffer Write, 2^n µsec	20: 0006h (2^6 = 64)
21h	01h	Typical Timeout per Individual Block Erase, 2^n msec	21: 000Ah (0Ah = 10d, 2^{10} = 1,024)
22h	01h	Typical Timeout for Full Chip Erase, 2^n msec	22: 000Fh (0Fh = 15d, 2^{15} = 32,768)
23h	01h	Maximum Timeout for Byte/Word Program, 2^n Times Typical	23: 0004h (2^4 = 16, 16 x Typical)
24h	01h	Maximum Timeout for Buffer Write, 2^n Times Typical	24: 0004h (2^4 = 16, 16 x Typical)
25h	01h	Maximum Timeout per Individual Block Erase, 2^n Times Typical	25: 0004h (2^4 = 16, 16 x Typical)
26h	01h	Maximum Timeout for Full Chip Erase, 2^n Times Typical	26: 0004h (2^4 = 16, 16 x Typical)

DEVICE GEOMETRY DEFINITION

This table provides critical details of the device geometry.

Table 9
Device Geometry Definition

OFFSET	LENGTH (BYTES)	DESCRIPTION	VALUE
27h	01h	Device Size = 2^n in number of bytes	(15h = 21d, 2^{21} = 2,097,152 bytes = 2MB = 16Mb)
28h	02h	Flash Device Interface Description: Value Meaning 0002h x8/x16 asynchronous	28: 0002h 29: 0000h
2Ah	02h	Maximum Number of Bytes in Write Buffer = 2^n	2A: 0005h 2B: 0000h (2^5 = 32)
2Ch	01h	Number of Erase Block Regions Within Device: Bits 7–0 = x = number of regions within the device containing one or more contiguous erase blocks of the same size	2C: 0001h
2Dh	04h	Erase Block Region Information: Bits 15–0 = y, where y + 1 = number of erase blocks of identical size within region. Bits 31–16 = z, where the erase block(s) within this region are z × 256 bytes and z is the number of 256-byte clusters in an erase block.	y: 2D: 001Fh 2E: 0000h (1Fh + 1 = 32 blocks) z: 2F: 0000h 30: 0001h (100h = 256, 256 x 256 = 64KB)

MICRON-SPECIFIC EXTENDED QUERY TABLE

Table 10 specifies Micron-Specific Extended Query. Some flash features and commands are optional.

Table 10
Primary Vendor-Specific Extended Query

OFFSET	LENGTH (BYTES)	DESCRIPTION	DATA
(P)h	03h	Primary Extended Query Table Unique ASCII String "PRI"	31: 0050h 32: 0052h 33: 0049h
(P+3)h	01h	Major Version Number, ASCII	34: 0031h
(P+4)h	01h	Minor Version Number, ASCII	35: 0030h
(P+5)h	04h	Optional Feature and Command Support Bit 0 Chip Erase Supported = yes = 1 Bit 1 Suspend Erase Supported = yes = 1 Bit 2 Suspend Program Supported = yes = 1 Bit 3 Lock/Unlock Supported = yes = 1 Bit 4 Queued Erase Supported = no = 0 Bits 5-31 Reserved for Future Use; undefined bits are "0"	36: 000Fh 37: 0000h 38: 0000h 39: 0000h
(P+9)h	01h	Functions Supported After Suspend Read array, status, and query are always supported during suspended erase or program operation. This field defines other operations supported. Bit 0 Program Supported After Erase Suspend = yes = 1 Bits 1-7 Reserved for Future Use; undefined bits are "0"	3A: 0001h
(P+A)	02h	Block Status Register Mask Defines which bits in the block status register section of query are implemented. Bit 0 Block Status Register Lock Bit [BSR0] Active = yes = 1 Bit 1 Block Erase Status Bit [BSR1] Active = yes = 1 Bits 2-15 Reserved for Future Use; undefined bits are "0"	3B: 0003h 3C: 0000h
(P+C)h	01h	V_{CC} Logic Supply Optimum Program/Erase Voltage (highest performance) Bits 7–4 BCD value in volts Bits 3–0 BCD value in 100mV	3D: 0050h
(P+D)h	01h	V_{PP} [Programming] Supply Optimum Program/Erase Voltage Bits 7–4 HEX value in volts Bits 3–0 BCD value in 100mV	3E: 0050h
(P+E)h	Reserved	Reserved for Future Use	

NOTE: 1. The variable "P" is a pointer which is defined at offset 15h in Table 7.

READ IDENTIFIER CODES COMMAND

By writing the READ IDENTIFIER CODES command, the IDENTIFIER CODE operation is initiated. Following the command write, READ cycles from addresses shown in Figure 2 (p. 5) retrieve information on the manufacturer, device, block lock configuration, and block erase status codes (see Table 11 for identifier code values). To terminate the operation, write another valid command. Like the READ ARRAY command, the READ IDENTIFIER CODES command functions independently of the V_{PP} voltage. Following the READ IDENTIFIER CODES command, the information in Table 11 can be read.

READ STATUS REGISTER COMMAND

The READ STATUS REGISTER command functions independently of the V_{PP} voltage. It is used to determine the successful completion of programming, block erasure, or lock bit configuration. The status register may be read by writing the READ STATUS REGISTER command. Once the command is written, all subsequent READ operations output data from the status register, with this data being latched on the falling edge of OE# or CEx#, whichever occurs last. To update the status register latch, OE# or CEx# must be toggled to V_{IH}.

Table 11
Identifier Codes

CODE	ADDRESS[1]	DATA
Manufacturer Compatibility Code	000000	B0
Device Code	000001	D0
Block Lock Configuration • Block is unlocked • Block is locked • Reserved for future use	X0002[2]	 DQ0 = 0 DQ0 = 1 DQ2-DQ7
Block Erase Status • Last erase completed successfully • Last erase did not complete successfully • Reserved for future use	X0002[2]	 DQ1 = 0 DQ1 = 1 DQ2-DQ7

NOTE: 1. A0 should be ignored in this address. The lowest-order address line is A1 in both word and byte mode.
2. "X" selects the specific block lock configuration code. See Figure 2 for the device identifier code memory map.

From time ^{t}WB after a program, block erase, set block lock bit, or clear block lock bits command sequence, only SR7 is valid until the ISM completes or suspends the operation. Device I/O pins DQ0-DQ6 and DQ8-DQ15 are invalid. Once the operation completes or suspends (SR7 = 1), all contents of the status register are valid when read. The extended status register (XSR) may be read to determine write buffer availability (see Table 15). By writing the WRITE-to-BUFFER command, the XSR may be read at any time. After writing this command, all subsequent READ operations output data from the XSR until another valid command is written. The contents of the XSR are latched on the falling edge of OE# or CEx#, whichever occurs last in the READ cycle. To update the XSR latch, the WRITE-to-BUFFER command must be re-issued.

CLEAR STATUS REGISTER COMMAND

Status register bits SR5, SR4, SR3, and SR1 are set to "1s" by the ISM and can only be reset by the CLEAR STATUS REGISTER command. These bits indicate various failure conditions (see Table 14). By allowing system software to reset these bits, several operations may be performed. The status register may be polled to determine if an error occurred during the sequence. To clear the status register, the CLEAR STATUS REGISTER command is written. It functions independently of the applied V_{PP} voltage. Note that this command is not functional during block erase or program suspend modes.

BLOCK ERASE COMMAND

A BLOCK ERASE is initiated by a two-cycle command and is executed one block at a time. A BLOCK ERASE SETUP command is written, followed by a CONFIRM command. This command sequence requires appropriate sequencing and that an address within the block be erased. Block preconditioning, erase, and verify are handled internally by the ISM (invisible to the system). After the two-cycle block erase sequence is written, the device automatically outputs status register data when read (see Figure 6). The CPU can detect block erase completion by analyzing STS in RY/BY# level mode or status register bit SR7. Toggle OE#, CE0#, or CE1# to update the status register.

Upon completion of BLOCK ERASE, status register bit SR5 should be checked. If a block erase error is detected, the status register should be cleared before system software attempts corrective actions. The CEL remains in read status register mode until a new command is issued.

This two-step command sequence of setup followed by execution ensures that block contents are not accidentally erased. An invalid block erase command sequence will result in both status register bits SR4 and SR5 being set to "1." Also, reliable block erasure can only occur when $V_{CC} = V_{CC1/2}$ and $V_{PP} = V_{PPH1/2/3}$. In the absence of these voltages, block contents are protected against erasure. If BLOCK ERASE is attempted while $V_{PP} \leq V_{PPLK}$, SR3 and SR5 will be set to "1." Successful BLOCK ERASE requires that the corresponding block lock bit be cleared or that WP# $\geq V_{IH}$. If BLOCK ERASE is attempted when the corresponding block lock bit is set and WP# = V_{IL}, the BLOCK ERASE will fail, and SR1 and SR5 will be set to "1."

FULL CHIP ERASE COMMAND

The FULL CHIP ERASE command erases all unlocked blocks. After the CONFIRM command is written, the device erases all unlocked blocks from block 0 to block 31 sequentially. Block preconditioning, erase, and verify are handled internally by the ISM. After the full chip erase command sequence is written to the CEL, the device automatically outputs the status register data when read. The CPU can detect full chip erase completion by polling the STS pin in RY/BY# level mode or status register bit SR7.

Once the FULL CHIP ERASE is complete, status register bit SR5 should be checked to see if the operation completed successfully. If an erase error occurred, the status register should be cleared before issuing the next command. The CEL remains in read status register mode until a new command is issued. In the absence of these voltages, the block contents can be protected against erasure. Issuing the READ IDENTIFIER CODES command or QUERY command can inform the user of which block(s) failed to erase. This two-step command sequence of setup followed by execution ensures that block contents are not accidentally erased. An invalid full chip erase command sequence will set both status register bits SR4 and SR5 to "1." Also, reliable full chip erasure can only occur when $V_{CC} = V_{CC1/2}$ and $V_{PP} = V_{PPH1/2/3}$. Block contents can be protected against erasure in the absence of these voltages. If FULL CHIP ERASE is attempted while $V_{PP} \leq V_{PPLK}$, SR3 and SR5 will be set to "1." FULL CHIP ERASE cannot be suspended.

WRITE-TO-BUFFER COMMAND

A WRITE-to-BUFFER command sequence is initiated to program the flash device via the write buffer. A variable number of bytes or words can be written into the buffer and be programmed to the flash device. First, the WRITE-to-BUFFER SETUP command is issued, along with the block address. At this point, the XSR information is loaded and XSR7 indicates that another WRITE-to-BUFFER command is possible. If XSR7 = 0, the write buffer is not available. To retry, continue monitoring XSR7 by issuing the WRITE-to-BUFFER SETUP command with the block address until XSR7 = 1. When XSR7 = 1, the buffer is ready for loading. Next, a word or byte count is issued at a valid address within the block. On the next write, a device start address is given along with the write buffer data. To optimize the performance and lower power, align the start address at the beginning of a write buffer boundary. Depending on the count, subsequent writes must supply additional device addresses and data.

Once the final buffer data is given, a WRITE CONFIRM command is issued. This allows the ISM to begin copying the buffer data to the flash memory. If a command other than WRITE CONFIRM is written to the device, an invalid command/sequence error will be generated and status register bits SR5 and SR4 will be set to "1." Additional BUFFER WRITEs can be issued with another WRITE-to-BUFFER SETUP command and check XSR7. Refer to Figure 3 for the WRITE-to-BUFFER Flowchart.

If an error occurs during writing, the device will stop programming, and status register bit SR4 will be set to a "1" to indicate a program failure. Any time a media failure occurs during a program or erase (SR4 or SR5 is set), the device will not accept any more WRITE-to-BUFFER commands. Additionally, if the user attempts to write past an erase block boundary with a WRITE-to-BUFFER command, the device will abort programming and generate an invalid command/sequence error, and status register bits SR5 and SR4 will be set to "1." To clear SR4 and/or SR5, issue a CLEAR STATUS REGISTER command. Buffered programming can only occur when $V_{CC} = V_{CC1/2}$ and $V_{PP} = V_{PPH1/2/3}$. If programming is attempted while $V_{PP} \leq V_{PPLK}$, status register bits SR4 and SR5 will be set to "1." Programming attempts with invalid V_{CC} and V_{PP} voltages produce spurious results and should not be attempted. Finally, successful programming requires that the corresponding block lock bit be cleared, or WP# = V_{IH}. If a BUFFER WRITE command is issued when the corresponding block lock bit is set and WP# = V_{IL}, SR1 and SR4 will be set to "1."

BYTE/WORD PROGRAM COMMANDS

The byte/word programming is executed by a two-cycle command sequence. After the byte/word program setup, a second write is needed to specify the address and data (latched on the rising edge of WE#). Next, the ISM takes over to control the program and verify algorithms internally. Once the write sequence is written, the device automatically outputs status register data when read. The CPU can detect the completion of the program event by analyzing the STS in RY/BY# level

mode or status register bit SR7. Upon programming completion, status register bit SR4 should be checked. If a programming error is detected, the status register should be cleared. The ISM verify only detects errors for "1s" that do not successfully program to "0s." The CEL remains in read status register mode until it receives another command. Refer to Figure 4 for the SINGLE WORD/BYTE PROGRAM Flowchart. Also, reliable byte/word programming can only occur when $V_{CC} = V_{CC1/2}$ and $V_{PP} = V_{PPH1/2/3}$. In the absence of this high voltage, contents are protected against programming. If a byte/word program is tried while $V_{PP} \leq V_{PPLK}$, status register bits SR4 and SR3 will be set to "1." Successful byte/word programming requires that the corresponding block lock bit be cleared. If a byte/word program is attempted when the corresponding block lock bit is set and WP# = V_{IL}, SR1 and SR4 will be set to "1."

STS CONFIGURATION COMMAND

Using the STS CONFIGURATION command, the STS pin can be configured to different states. Once configured, it remains in that configuration until another CONFIGURATION command is issued or RP# is LOW. Initially, the STS pin defaults to RY/BY# level operation. STS LOW indicates that the state machine is busy, while STS HIGH indicates that the state machine is ready for a new operation or is suspended.

To change the STS pin to other modes, the STS CONFIGURATION command must be issued followed by the desired configuration code. The three alternate pulse-mode configurations may be used as a system interrupt as described in Table 13. With these configurations, bit 0 controls erase complete interrupt pulse, and bit 1 controls write complete interrupt pulse. Once the device is configured in one of the pulse modes, the STS pin pulses LOW with a typical pulse width of 250ns. Issuing the 00h configuration code with the CONFIGURATION command resets the STS pin to the default RY/BY# level mode. Table 13 explains configuration coding definitions. The CONFIGURATION command may only be given when the device is not busy or suspended. Check SR7 for device status. An invalid configuration code will result in status register bits SR4 and SR5 being set to "1."

BLOCK ERASE SUSPEND COMMAND

This command allows block erase interruption to read or program data in another block of memory. Right after starting the block erase process, writing the BLOCK ERASE SUSPEND command requests that the ISM suspend the block erase sequence at a predetermined point in the algorithm. When read after the BLOCK ERASE SUSPEND command is written, the device outputs the status register. Polling status register bit SR7 can determine when the BLOCK ERASE operation has been suspended. When SR7 = 1, SR6 should also be set to "1," indicating that the device is in the erase suspend mode. STS in RY/BY# level mode will also transition to V_{OH}. Specification ^{t}LES defines the block erase suspend latency. At this point, a READ ARRAY command can be written to read data from blocks other than that which is suspended. A program command sequence can also be issued during erase suspend to program data in other blocks. Using the PROGRAM SUSPEND command (see Program Suspend Command section), a PROGRAM operation can also be suspended. During a PROGRAM operation with block erase suspended, status register bit SR7 will return to "0," and STS in RY/BY# mode will transition to V_{OL}. However, SR6 will remain "1" to indicate block erase suspend status.

READ STATUS REGISTER and BLOCK ERASE RESUME are the only other valid commands while block erase is suspended. Once a BLOCK ERASE RESUME command is written to the flash memory, the ISM will continue the block erase process. Status register bits SR6 and SR7 will automatically clear, and STS in RY/BY# mode will return to V_{OL}. Once the ERASE RESUME command is written, the device automatically outputs status register data when read (see Figure 8). V_{PP} must remain at $V_{PPH1/2/3}$ and V_{CC} must remain at $V_{CC1/2}$ (the same V_{PP} and V_{CC} levels used for BLOCK ERASE) while block erase is suspended. RP# ≥ V_{IH}. BLOCK ERASE cannot resume until program operations initiated during BLOCK ERASE SUSPEND have completed.

PROGRAM SUSPEND COMMAND

The PROGRAM SUSPEND command enables program interruption to read data in other flash memory locations. After starting the programming process, writing the PROGRAM SUSPEND command requests that the ISM suspend the program sequence at a predetermined point in the algorithm. Once the PROGRAM SUSPEND command is written, the device continues to output status register data when read. Polling status register bit SR7 can determine when the programming operation has been suspended. When SR7 = 1, SR2 should also be set to "1" to indicate that the device is in the program suspend mode. STS in RY/BY# level mode will also transition to V_{OH}. Note that ^{t}LPS defines the program suspend latency. A READ ARRAY command can be written to read data from locations other than that which is suspended. While programming is suspended, the only other valid commands are READ STATUS REGISTER and PROGRAM RESUME. Once a PROGRAM RESUME command is written, the ISM will continue the programming process. Then status register bits SR2 and SR7 will automatically clear and STS in

RY/BY# mode will return to VOL. Once a PROGRAM RESUME command is written, the device automatically outputs status register data when read. VPP must remain at VPPH1/2/3 and VCC must remain at VCC1/2 while in program suspend mode. RP# must also remain at VIH (the same RP# level used for programming). Refer to Figure 5 for the PROGRAM SUSPEND/RESUME Flowchart.

SET BLOCK LOCK BITS COMMAND

A flexible block locking and unlocking scheme is enabled via a combination of block lock bits. The block lock bits gate PROGRAM and ERASE operations. With WP# = VIH, individual block lock bits can be set using the SET BLOCK LOCK BITS command.

SET BLOCK LOCK BITS is started using a two-cycle command sequence. The SET BLOCK LOCK BITS setup along with appropriate block address is written, followed by the SET BLOCK LOCK BITS CONFIRM and an address within the block to be locked. The ISM then controls the set lock bit algorithm. Once the sequence is written, the device automatically outputs status register data when read. The CPU then can detect the completion of the set lock bit event by analyzing STS in RY/BY# level mode or status register bit SR7.

Upon completion of the SET BLOCK LOCK BITS operation, status register bit SR4 should be checked. If an error is detected, the status register should be cleared. The CEL will remain in the read status register mode until a new command is issued.

This two-step sequence of setup followed by execution ensures that lock bits are not accidentally set. An invalid SET BLOCK LOCK BITS command will result in status register bits SR4 and SR5 being set to "1." Also, reliable operations occur only when VCC = VCC1/2 and VPP = VPPH1/2/3. If these voltages are absent, lock bit contents are protected against alteration. A successful SET BLOCK LOCK BITS operation requires that WP# = VIH. If it is attempted with WP# = VIL, the operation will fail, and SR1 and SR4 will be set to "1." See Table 12 for write protection alternatives and refer to Figure 8 for the SET BLOCK LOCK BITS Flowchart.

CLEAR BLOCK LOCK BITS COMMAND

The CLEAR BLOCK LOCK BITS command can clear all set block lock bits in parallel. This command is valid only when WP# = VIH. The CLEAR BLOCK LOCK BITS operation is started using a two-cycle command sequence. A CLEAR BLOCK LOCK BITS SETUP command is written, followed by a CONFIRM command. Then, the device automatically outputs status register data when read (see Figure 10). Once completed, the CPU can detect the completion of the clear block lock bits event by analyzing STS in RY/BY# level mode or status register bit SR7.

This two-step sequence of setup followed by execution ensures that block lock bits are not accidentally cleared. An invalid clear block lock bits command sequence will result in status register bits SR4 and SR5 being set to "1." Also, a reliable CLEAR BLOCK LOCK BITS operation can only occur when VCC = VCC1/2 and VPP = VPPH1/2/3. If a CLEAR BLOCK LOCK BITS operation is attempted while VPP ≤ VPPLK, SR3 and SR5 will be set to "1." If these voltages are absent, the block lock bits contents are protected against alteration.

When a CLEAR BLOCK LOCK BITS operation is aborted due to VPP or VCC transitioning out of valid range and RP# or WP# active transition, block lock bit values become undetermined. Then, a repeat of CLEAR BLOCK LOCK BITS is required to initialize block lock bit contents to known values.

Once the operation is complete, status register bit SR5 should be checked. Also, if a clear block lock bits error is detected, the status register should be cleared. The CEL will remain in read status register mode until another command is issued.

Table 12
Write Protection Alternatives

OPERATION	BLOCK LOCK BIT	WP#	EFFECT
PROGRAM AND BLOCK ERASE	0	V_{IL} or V_{IH}	Block erase and programming enabled
	1	V_{IL}	Block is locked; block erase and programming disabled
		V_{IH}	Block lock bit override; block erase and programming enabled
FULL CHIP ERASE	0,1	V_{IL}	All unlocked blocks are erased
	X	V_{IH}	Block lock bit override; all blocks are erased
SET OR CLEAR BLOCK LOCK BITS	X	V_{IL}	Set or clear block lock bits disabled
		V_{IH}	Set or clear block lock bits enabled

Table 13
Configuration Coding Definitions

RESERVED	PULSE ON WRITE COMPLETE	PULSE ON ERASE COMPLETE
BITS 7–2	**BIT 1**	**BIT 0**
DQ7–DQ2 = Reserved DQ1/DQ0 = STS Pin Configuration Codes 00 = Default, RY/BY# level mode (device ready) indication 01 = Pulse on Erase Complete 10 = Pulse on Flash Program Complete 11 = Pulse on Erase or Program Complete Configuration codes 01b, 10b, and 11b are all pulse modes such that the STS pin pulses low then high when the operation indicated by the given configuration is completed. Configuration command sequences for STS pin configuration (masking bits DQ7–DQ2 to 00h) are as follows: Default RY/BY# level mode: B8h, 00h ER INT (Erase Interrupt): B8h, 01h Pulse on Erase Complete PR INT (Program Interrupt): B8h, 02h Pulse on Flash Program Complete ER/PR INT (Erase or Program Interrupt): B8h, 03h Pulse on Erase or Program Complete	DQ7–DQ2 are reserved for future use. Default RY/BY# level mode (DQ1/DQ0 = 00) Used to control HOLD to a memory controller to prevent accessing a flash memory subsystem while any flash device's ISM is busy. Configuration 01 ER INT, pulse mode[1] Used to generate a system interrupt pulse when any flash device in an array has completed a BLOCK ERASE or sequence of queued BLOCK ERASEs; Helpful for reformatting blocks after file system free space reclamation or "cleanup." Configuration 10 PR INT, pulse mode[1] Used to generate a system interrupt pulse when any flash device in an array has completed a PROGRAM operation. Provides highest performance for servicing continuous BUFFER WRITE operations. Configuration ER/PR INT, pulse mode[1] Used to generate system interrupts to trigger the servicing of flash arrays when either ERASE or flash PROGRAM operations are completed when a common interrupt service routine is desired.	

NOTE: 1. When the device is configured in one of the pulse modes, the STS pin pulses low with a typical pulse width of 250ns.

Table 14
Status Register Definition

ISMS	ESS	ECLBS	PSLBS	VPPS	PSS	DPS	R
7	6	5	4	3	2	1	0

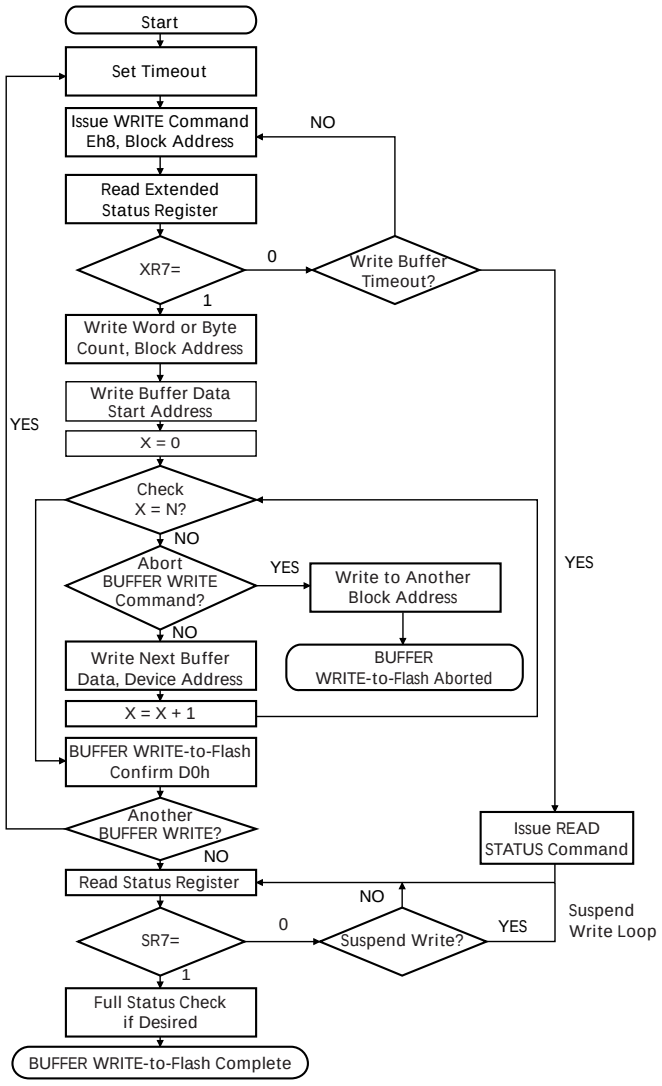
STATUS REGISTER BIT (SR)	DESCRIPTION
SR7 = INTERNAL STATE MACHINE STATUS (ISMS) 1 = Ready 0 = Busy	Check STS in RY/BY# mode or SR7 to determine block erase, programming, or lock bit configuration completion. SR6-SR0 are invalid when SR7 = 0.
SR6 = ERASE SUSPEND STATUS (ESS) 1 = BLOCK ERASE suspended 0 = BLOCK ERASE in progress/completed	
SR5 = ERASE AND CLEAR LOCK BITS STATUS (ECLBS) 1 = Error in block erasure or clear lock bits 0 = Successful block erase or clear lock bits	If both SR5 and SR4 are "1s" after a block erase or lock bit configuration attempt, an improper command sequence was entered.
SR4 = PROGRAM AND SET LOCK BITS STATUS (PSLBS) 1 = Error in program or block lock bits 0 = Successful program or set block lock bits	
SR3 = VPP STATUS (VPPS) 1 = VPP low detect, operation abort 0 = VPP OK	SR3 does not provide a continuous indication of VPP level. The ISM interrogates and indicates the VPP level only after a BLOCK ERASE, PROGRAM, or LOCK BIT CONFIGURATION operation. SR3 reports accurate feedback only when VPP = VPPH1/2/3.
SR2 = PROGRAM SUSPEND STATUS (PSS) 1 = PROGRAM suspended 0 = PROGRAM in progress/completed	
SR1 = DEVICE PROTECT STATUS (DPS) 1 = Block lock bit and/or WP# lock detected, operation abort 0 = Unlock	SR1 does not provide a continuous indication of block lock bit values. The ISM interrogates the block lock bit and WP# only after a BLOCK ERASE, PROGRAM, or LOCK BIT CONFIGURATION operation. It informs the system, depending on the attempted operation, if the block lock bit is set.
SR0 = Reserved for future enhancements	SR0 is reserved for future use and should be masked when polling the status register.

Table 15
Extended Status Register Definition (XSR)

WBS	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0

STATUS REGISTER BIT (XSR)	DESCRIPTION
XSR7 = WRITE BUFFER STATUS (WBS) 1 = WRITE-to-BUFFER available 0 = WRITE-to-BUFFER not available	After a WRITE-to-BUFFER command, XSR7 indicates that a WRITE-to-BUFFER command is possible.
XSR6-0 = Reserved for future enhancements	SR6–SR0 are reserved for future use and should be masked when polling the status register.

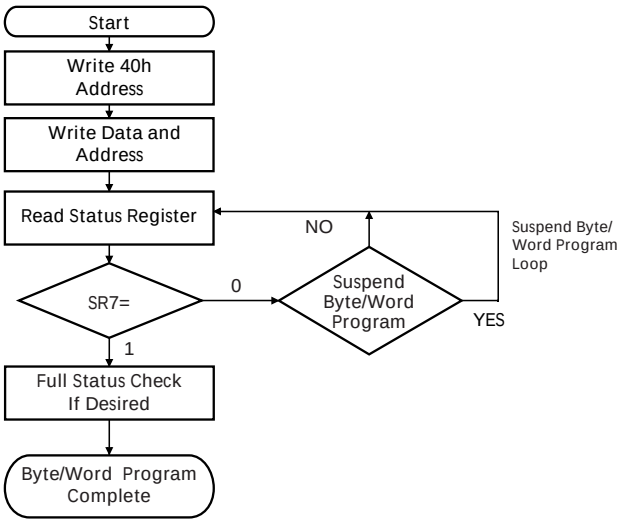
Figure 3
WRITE-to-BUFFER Flowchart



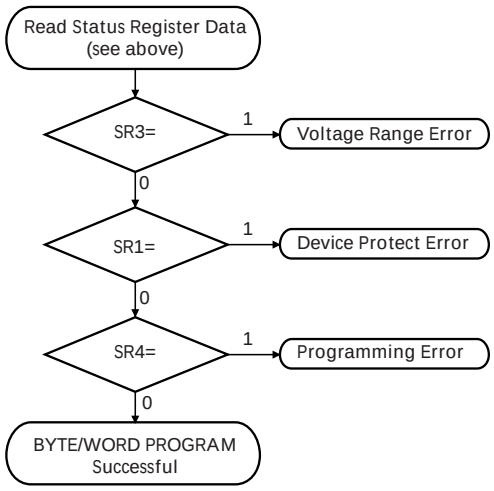
BUS OPERATION	COMMAND	COMMENTS
WRITE	WRITE-to-BUFFER	Data = E8h Block Address
READ		XSR 7 = Valid Addr = X
STANDBY		Check XSR 7 1 = Write Buffer Available 0 = Write Buffer Not Available
WRITE[1,2]		Data = N = Word/Byte Count N = 0 Corresponds to Count = 1 Addr = Block Address
WRITE[3,4]		Data = Write Buffer Data Addr = Device Start Address
WRITE[5,6]		Data = Write Buffer Data Addr = Device Address
WRITE	BUFFER WRITE-to-FLASH CONFIRM	Data = D0h Addr = X
READ		Status register data with the device enabled, OE# LOW Updates SR Addr = X
STANDBY		Check SR7 1 = ISM Ready 0 = ISM Busy
Full status check can be done after all erase and write sequences complete. Write FFh after the last operation to reset the device to read array mode.		

NOTE:
1. Byte or word count values on DQ0-DQ7 are loaded into the count register. Count ranges on this device for byte mode are N = 00h to 1Fh and for word mode are N = 0000h to 000Fh.
2. The device now outputs the status register when read (XSR is no longer available).
3. Write buffer contents will be programmed at the device start address or destination flash address.
4. Align the start address on a write buffer boundary for maximum programming performance (i.e., A4-A0 of the start address = 0).
5. The device aborts the WRITE-to-BUFFER command if the current address is outside of the original block address.
6. The status register indicates an "improper command sequence" if the WRITE-to-BUFFER command is aborted. Follow this with a CLEAR STATUS REGISTER command.

Figure 4
SINGLE BYTE/WORD PROGRAM Flowchart



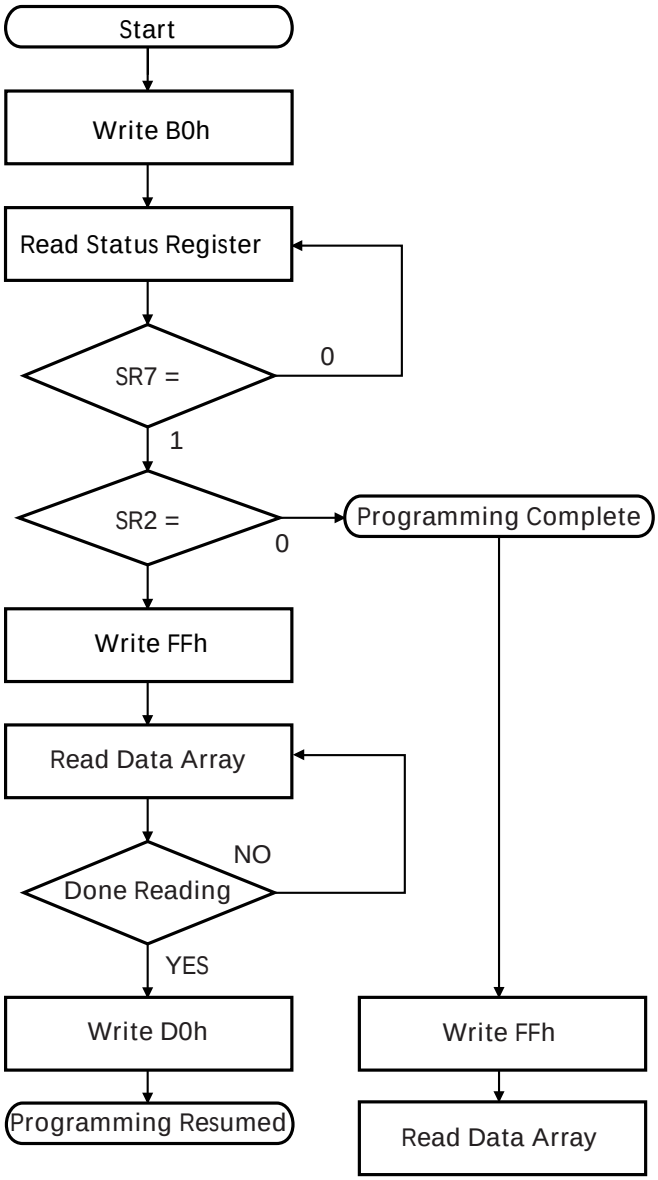
FULL STATUS CHECK PROCEDURE



BUS OPERATION	COMMAND	COMMENTS
WRITE	SETUP BYTE/ WORD PROGRAM	Data = 40h Addr = Location to Be Programmed
WRITE	BYTE/WORD PROGRAM	Data = Data to Be Programmed Addr = Location to Be Programmed
READ		Status Register Data
STANDBY		Check SR7 1 = ISM Ready 0 = ISM Busy
Repeat for subsequent programming operations. SR full status check can be done after each PROGRAM operation or after a sequence of programming operations. Write FFh after the last program operation to place device in read.		

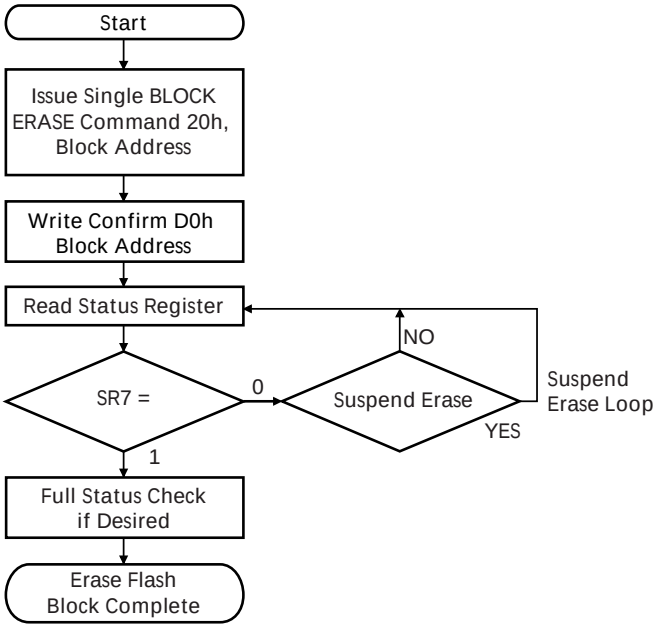
BUS OPERATION	COMMAND	COMMENTS
STANDBY		Check SR3 1 = Programming Voltage Error Detect
STANDBY		Check SR1 1 = Device Protect Detect RP# = V_{IH} , block lock bit is set. Only required for systems implementing lock bit configuration
STANDBY		Check SR4 1 = Programming Error
SR4, SR3, and SR1 are only cleared by the CLEAR STATUS REGISTER command in cases where multiple locations are programmed before full status is checked. If an error is detected, clear the status register before attempting retry or other error recovery.		

Figure 5
PROGRAM SUSPEND/RESUME Flowchart



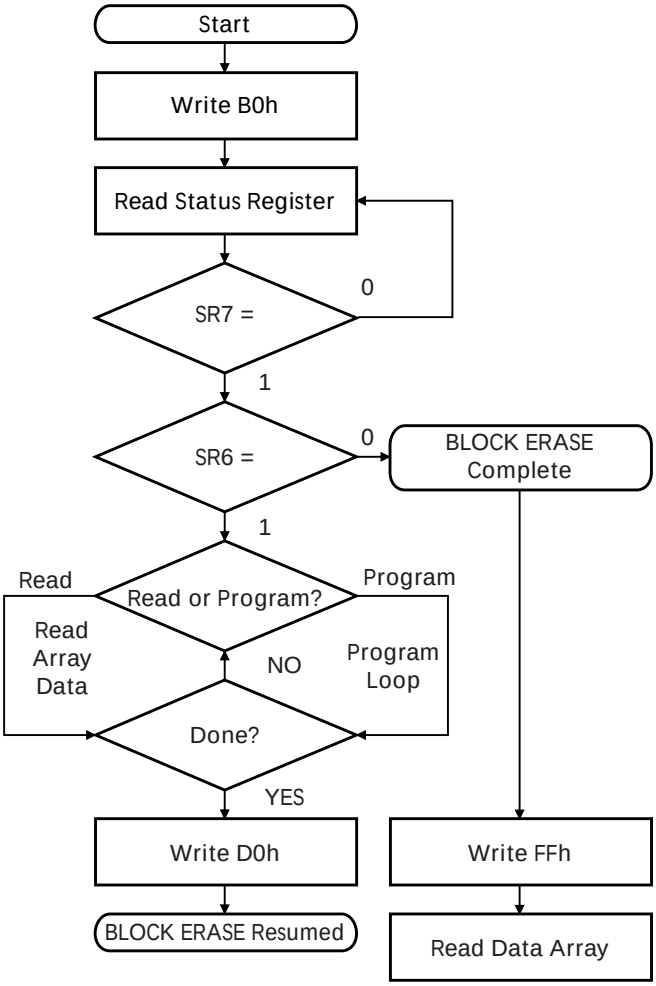
BUS OPERATION	COMMAND	COMMENTS
WRITE	PROGRAM SUSPEND	Data = B0h Addr = X
READ		Status Register Data Addr = X
STANDBY		Check SR7 1 - ISM Ready 0 = ISM Busy
STANDBY		Check SR6 1 = Programming Suspended 0 = Programming Completed
WRITE	READ ARRAY	Data = FFh Addr = X
READ		Read array location other than that being programmed
WRITE	PROGRAM RESUME	Data = D0h Addr = X

Figure 6
BLOCK ERASE Flowchart



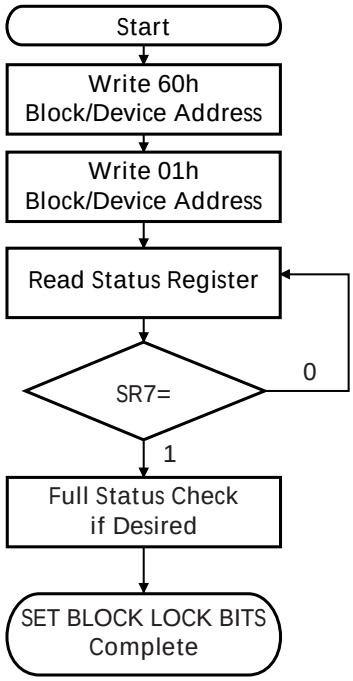
BUS OPERATION	COMMAND	COMMENTS
WRITE	ERASE BLOCK	Data = 28h or 20h Addr = Block Address
READ		XSR7 = Valid Addr = X
WRITE	ERASE CONFIRM	Data = D0h Addr = X
READ		Status register data With the device enabled, OE# LOW updates SR Addr = X
STANDBY		Check SR7 1 = ISM Ready 0 = ISM Busy
Full status check can be done after all erase and write sequences complete. Write FFh after the last operation to reset the device to read array mode.		

Figure 7
BLOCK ERASE SUSPEND/RESUME Flowchart



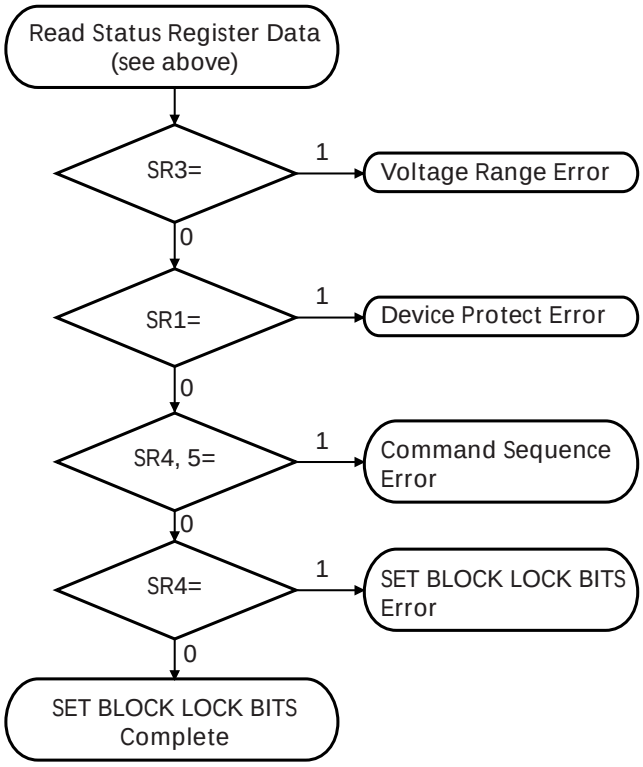
BUS OPERATION	COMMAND	COMMENTS
WRITE	ERASE SUSPEND	Data = B0h Addr = X
READ		Status Register Data Addr = X
STANDBY		Check SR7 1 - ISM Ready 0 = ISM Busy
STANDBY		Check SR6 1 = Block Erase Suspended 0 = Block Erase Completed
WRITE	ERASE RESUME	Data = D0h Addr = X

Figure 8
SET BLOCK LOCK BITS Flowchart



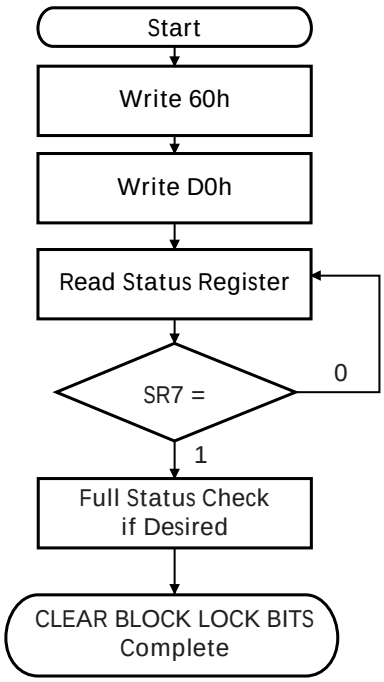
BUS OPERATION	COMMAND	COMMENTS
WRITE	CLEAR BLOCK LOCK BITS SETUP	Data = 60h Addr = X
WRITE	SET BLOCK LOCK BITS CONFIRM	Data = 01h Addr = X
READ		Status Register Data
STANDBY		Check SR7 1 = ISM Ready 0 = ISM Busy
Full status check can be done after each SET BLOCK LOCK BITS operation or a sequence of block lock bits set. Write FFh after the last SET BLOCK LOCK BITS operation to place the device in array mode.		

FULL STATUS CHECK PROCEDURE



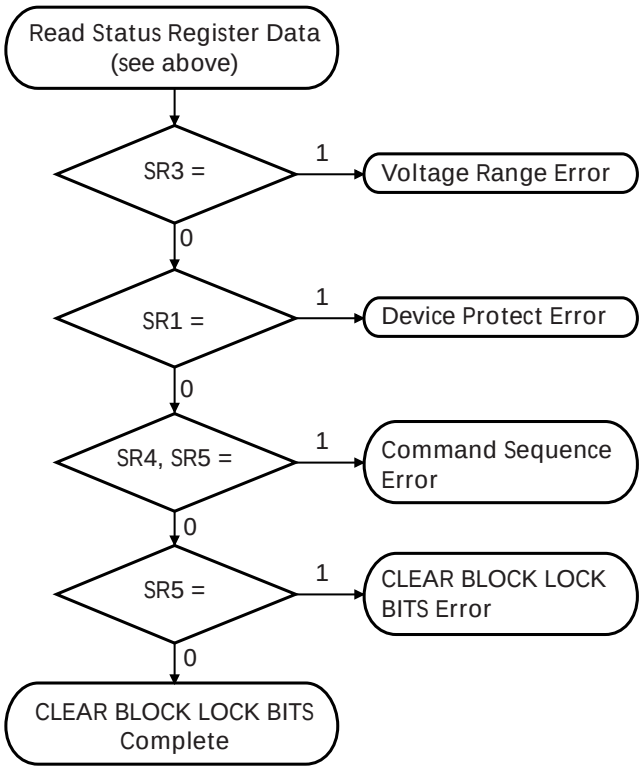
BUS OPERATION	COMMAND	COMMENTS
STANDBY		Check SR3 1 = Programming Voltage Error Detect
STANDBY		Check SR1 1 = Device Protect Detect WP# = V_{IL}
STANDBY		Check SR4, SR5 Both 1 = Command Sequence Error
STANDBY		Check SR5 1 = Set Block Lock Bits
SR5, SR4, SR3, and SR1 are only cleared by the CLEAR REGISTER command in cases where multiple lock bits are set full status. If an error is detected, clear the status register before attempting retry or other error recovery.		

Figure 9
CLEAR BLOCK LOCK BITS Flowchart



BUS OPERATION	COMMAND	COMMENTS
WRITE	CLEAR BLOCK LOCK BITS SETUP	Data = 60h Addr = X
WRITE	CLEAR BLOCK LOCK BITS CONFIRM	Data = D0h Addr = X
READ		Status Register Data
STANDBY		Check SR7 1 = ISM Ready 0 = ISM Busy
Write FFh after the CLEAR BLOCK LOCK BITS operation to place device in read array mode.		

FULL STATUS CHECK PROCEDURE



BUS OPERATION	COMMAND	COMMENTS
STANDBY		Check SR3 1 = Programming Voltage Error Detect
STANDBY		Check SR1 1 = Device Protect Detect WP# = V_{IL}
STANDBY		Check SR4, SR5 Both 1 = Command Sequence Error
STANDBY		Check SR5 1 = Clear Block Lock Bits Error
SR5, SR4, SR3, and SR1 are only cleared by the CLEAR STATUS REGISTER command. If an error is detected, clear the status register before attempting retry or other error recovery.		

DESIGN CONSIDERATIONS

THREE-LINE OUTPUT CONTROL

This device has three control inputs to provide multiple memory connections: CE0#, CE1#, and OE#. Three-line control affords (1) lowest possible memory power dissipation; and (2) data bus contention avoidance.

To use these control inputs optimally, an address decoder should enable CEx#, while OE# should be connected to all memory devices and the system's READ# control line. This ensures that only selected memory devices have active outputs, while deselected memory devices are in standby mode. RP# should be connected to the system POWERGOOD signal to prevent unintended WRITEs during system power transitions. POWERGOOD should also toggle during system reset.

STS AND ISM POLLING

The open drain output pin STS should be connected to V_{CC} by a pull-up resistor to provide a hardware form of detecting block erase, program, and lock bit configuration completion. In default mode, it transitions LOW during execution of these commands and returns to V_{OH} when the ISM has finished executing the internal algorithm. See STS Configuration Command section for alternate STS configurations. STS can be connected to an interrupt input of the system CPU or controller. STS is active at all times. In the default mode, STS is also V_{OH} during block erase suspend or reset/power-down.

POWER SUPPLY DECOUPLING

Flash memory power switching characteristics require careful device decoupling. Active current levels, standby current levels, and transient peaks produced by falling and rising edges of CEx# and OE# are areas of consideration. Two-line control and proper decoupling capacitor selection can suppress transient voltage peaks. Each device should have a 0.1µF ceramic capacitor connected between its V_{CC} and GND and V_{PP} and GND. These high-frequency, low-inductance capacitors should be placed as close as possible to package leads. In addition, for every eight devices, a 4.7µF electrolytic capacitor should be placed at the array's power supply connection between V_{CC} and GND. The bulk capacitor will overcome voltage slumps caused by PC board trace inductance.

V_{CC}, V_{PP}, RP# TRANSITIONS

If RP# ≤ V_{IH}, or if V_{PP} or V_{CC} fall outside of a valid voltage range ($V_{CC1/2}$ and $V_{PPH1/2/3}$), block erase, program, and lock bit configuration are not guaranteed. If V_{PP} error is detected, status register bits SR3 and SR4 or SR5 are set to "1." If RP# transitions to V_{IL} during block erase, program, or lock bit configuration, STS in RY/BY# level mode will remain LOW until the RESET operation is complete. Then, the operation will abort and the device will enter deep power-down. Because the aborted operation may leave data partially altered, the command sequence must be repeated after normal operation is restored.

POWER-UP/DOWN PROTECTION

This device provides protection against accidental block erase, programming, or lock bit configuration during power transitions.

System designers must guard against spurious writes for V_{CC} voltages above V_{LKO} when V_{PP} is active. Since both WE# and CEx# must be LOW for a command write, driving either input signal to V_{IH} will inhibit WRITEs. The CEL's two-step command sequence architecture provides an added level of protection against data alteration. In-system block lock and unlock provides additional protection during power-up by prohibiting BLOCK ERASE and PROGRAM operations. RP# = V_{IL} disables the device, regardless of its control inputs states.

ABSOLUTE MAXIMUM RATINGS

Voltage on V_{CC} Supply
Relative to Vss ..... -0.2V to V_{CC}+ 0.5V*
Voltage on V_{PP} Voltage
Relative to Vss during Block Erase, Flash Write, and Lock Bit Configuration ..... -0.2V to +7.0V**
Output Short Circuit Current ..... 100 mA†
Voltage on Any Pin (except V_{CC} and V_{PP})
Relative to Vss ..... -0.5V to V_{CC} + 0.5V*
Temperature Under Bias:
Commercial ..... 0ºC to +70ºC
Extended ..... -40ºC to +85ºC
Storage Temperature ..... -65ºC to +125ºC

*All specified voltages are with respect to Vss (GND). Minimum DC voltage is -0.5V on input/output pins and -0.2V on V_{CC} and V_{PP} pins. During transitions, this level may undershoot to -2.0V for periods < 20ns. Maximum DC voltage on input/output pins and V_{CC} is V_{CC} + 0.5V which, during transitions, may overshoot to V_{CC} + 2.0V for periods < 20ns.

**Maximum DC voltage on V_{PP} may overshoot to +7.0V for periods < 20ns.

†Output shorted for no more than one second. No more than one output shorted at a time.

TEMPERATURE AND RECOMMENDED DC OPERATING CONDITIONS

Note: 1

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Operating Temperature Commercial Ambient Temperature	T_A	0	+70	ºC	
Extended Ambient Temperature		-40	+85	ºC	
V_{CC} Supply Voltage (2.7V to 3.6V)	V_{CC1}	2.7	3.6	V	
V_{CC} Supply Voltage (3.3V ±0.3V)	V_{CC2}	3.0	3.6	V	
INPUT LEAKAGE CURRENT V_{CC} = $V_{CC1/2}$ (MAX) V_{IN} = $V_{CC1/2}$ or GND	I_L		±0.5	µA	2
OUTPUT LEAKAGE CURRENT V_{CC} = $V_{CC1/2}$ (MAX) V_{OUT} = $V_{CC1/2}$ or GND	I_{OZ}		±0.5	µA	2
OUTPUT VOLTAGE LEVELS (TTL) V_{CC} = $V_{CC1/2}$ (MIN) Output High Voltage (I_{OL} = 5.8mA)	V_{OH1}	2.4		V	3, 4
Output Low Voltage (I_{OH} = –2.5mA)	V_{OL}		0.4	V	
OUTPUT HIGH VOLTAGE (CMOS) V_{CC} = $V_{CC1/2}$ (MIN) I_{OH} = –2.5mA	V_{OH2}	0.85 × V_{CC}		V	3, 4
V_{CC} = $V_{CC1/2}$ (MIN) I_{OH} = –100µA		V_{CC} - 0.4		V	
Input High Voltage	V_{IH}	3.3	V_{CC} + 0.5	V	5
Input Low Voltage	V_{IL}	-0.5	0.8	V	4

NOTE:
1. Device operations in the V_{CC} voltage ranges not covered in the table produce spurious results and should not be attempted.
2. All currents are in RMS unless otherwise noted. Typical values at nominal V_{CC} voltage and T_A = +25ºC. These currents are valid for all product versions (packages and speeds).
3. Includes STS in RY/BY# level mode.
4. Sampled, not 100% tested.
5. CMOS inputs are either V_{CC} ±0.2V or GND ±0.2V. TTL inputs are either V_{IL} or V_{IH}.

CAPACITANCE

T_A = +25ºC, f = 1 MHz

PARAMETER	SYMBOL	TYP	MAX	UNITS	NOTES
Input Capacitance: V_{IN} = 0.0V	C_{IN}	6	8	pF	
Output Capacitance: V_{OUT} = 0.0V	C_{IO}	8	12	pF	

DC ELECTRICAL CHARACTERISTICS

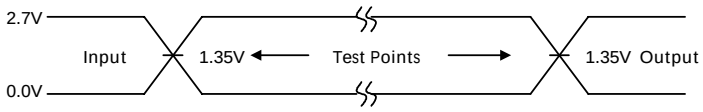
Commercial Temperature (0ºC ≤ T_A ≤ +70ºC) and Extended Temperature (-40ºC ≤ T_A ≤ +85ºC)

PARAMETER/CONDITION	SYMBOL	TYP	MAX	UNITS	NOTES
READ CURRENT: TTL INPUT LEVELS V_{CC} = $V_{CC1/2}$ (MAX) CEx# = V_{IL}; f = 5 MHz; I_{OUT} = 0mA	I_{CC1}		30	mA	
READ CURRENT: CMOS INPUT LEVELS V_{CC} = $V_{CC1/2}$ (MAX) CEx# = GND; f = 5 MHz; I_{OUT} = 0mA	I_{CC2}		25	mA	1, 3, 4
STANDBY CURRENT: TTL INPUT LEVELS V_{CC} = $V_{CC1/2}$ (MAX) CEx# = RP# = V_{IH}	I_{CC3}	1	4	mA	
STANDBY CURRENT: CMOS INPUT LEVELS V_{CC} = $V_{CC1/2}$ (MAX) CEx# = RP# = V_{CC} ±0.2V	I_{CC4}	20	100	µA	1, 2, 3
DEEP POWER-DOWN CURRENT: V_{CC} SUPPLY RP# = GND ±0.2V; OUT (RY/BY#) = 0mA	I_{CC5}	1	15	µA	1
STANDBY READ CURRENT: V_{PP} SUPPLY	I_{PP1}	±2	±15	µA	1
DEEP POWER-DOWN CURRENT: V_{PP} SUPPLY RP# = GND ±0.2V	I_{PP2}	0.1	5	µA	1
V_{PP} Lockout Voltage	V_{PPLK}		1.5	V	5, 6
V_{PP} Voltage	V_{PPH1}	2.7	3.6	V	6, 7
V_{PP} Voltage	V_{PPH2}	3.0	3.6	V	6, 7
V_{PP} Voltage	V_{PPH3}	4.5	5.5	V	6, 7
V_{CC} Lockout Voltage	V_{CCLK}	2.0		V	8

NOTE:
1. All currents are in RMS unless otherwise noted. Typical values at nominal V_{CC} voltage and T_A = +25ºC. These currents are valid for all product versions (packages and speeds).
2. Includes STS in RY/BY# level mode.
3. CMOS inputs are either V_{CC} ± 0.2V or GND ± 0.2V. TTL inputs are either V_{IL} or V_{IH}.
4. Automatic power savings (APS) reduces typical I_{CCR} to 3mA at 2.7V and 3.3V V_{CC} static operation.
5. Sampled, not 100% tested.
6. Refer to READ Operations timing diagram.
7. Refer to AC Characteristics – READ-Only Operations. If V_{CC} is in the range of 2.7V to 3.6V (V_{CC1}), then V_{PP} must be in the range of 2.7V to 3.6V (V_{PPH1}) or 4.5V to 5.5V (V_{PPH3}). If V_{CC} is in the range of 3.0V to 3.6V (V_{CC2}), then V_{PP} must be in the range of 3.0V to 3.6V (V_{PPH2}) or 4.5V to 5.5V (V_{PPH3}).
8. With V_{CC} ≤ V_{LKO}, flash memory WRITEs are inhibited.

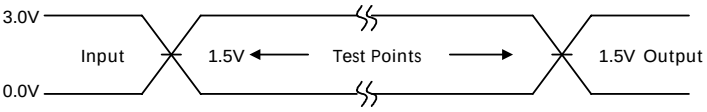
Table 16
Valid V_{PP}/V_{CC} Voltage

V_{CC} Voltage	V_{PP} Voltage
V_{CC1} = 2.7V to 3.6V	V_{PPH1} = 2.7V to 3.6V, V_{PPH2} = 3.0V to 3.6V, or V_{PPH3} = 4.5V to 5.5V
V_{CC2} = 3.0V to 3.6V	V_{PPH2} = 3.0V to 3.6V or V_{PPH3} = 4.5V to 5.5V



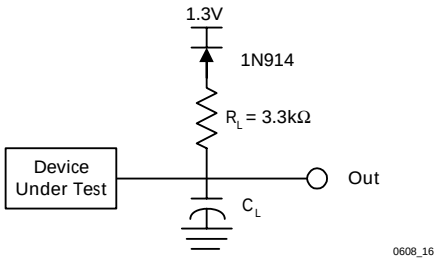
AC test inputs are driven at 2.7V for a logic 1 and 0.0V for a logic 0. Input timing begins and output timing ends at 1.35V. Input rise and fall times (10% to 90%) < 10ns.

Transient Input/Output Reference Waveform for V_{CC} = 2.7V–3.6V



AC test inputs are driven at 3.0V for a logic 1 and 0.0V for a logic 0. Input timing begins and output timing ends at 1.5V. Input rise and fall times (10% to 90%) < 10ns.

Transient Input/Output Reference Waveform for V_{CC} = 3.3V ±0.3V (High-Speed Testing Configuration)



NOTE: C_L includes jig capacitance.

Transient Equivalent Testing Load Circuit

Test Configuration Capacitance Loading Value

Test Configuration	C_L (pF)
V_{CC} = 3.3V ±0.3V, 2.7V to 3.6V	50

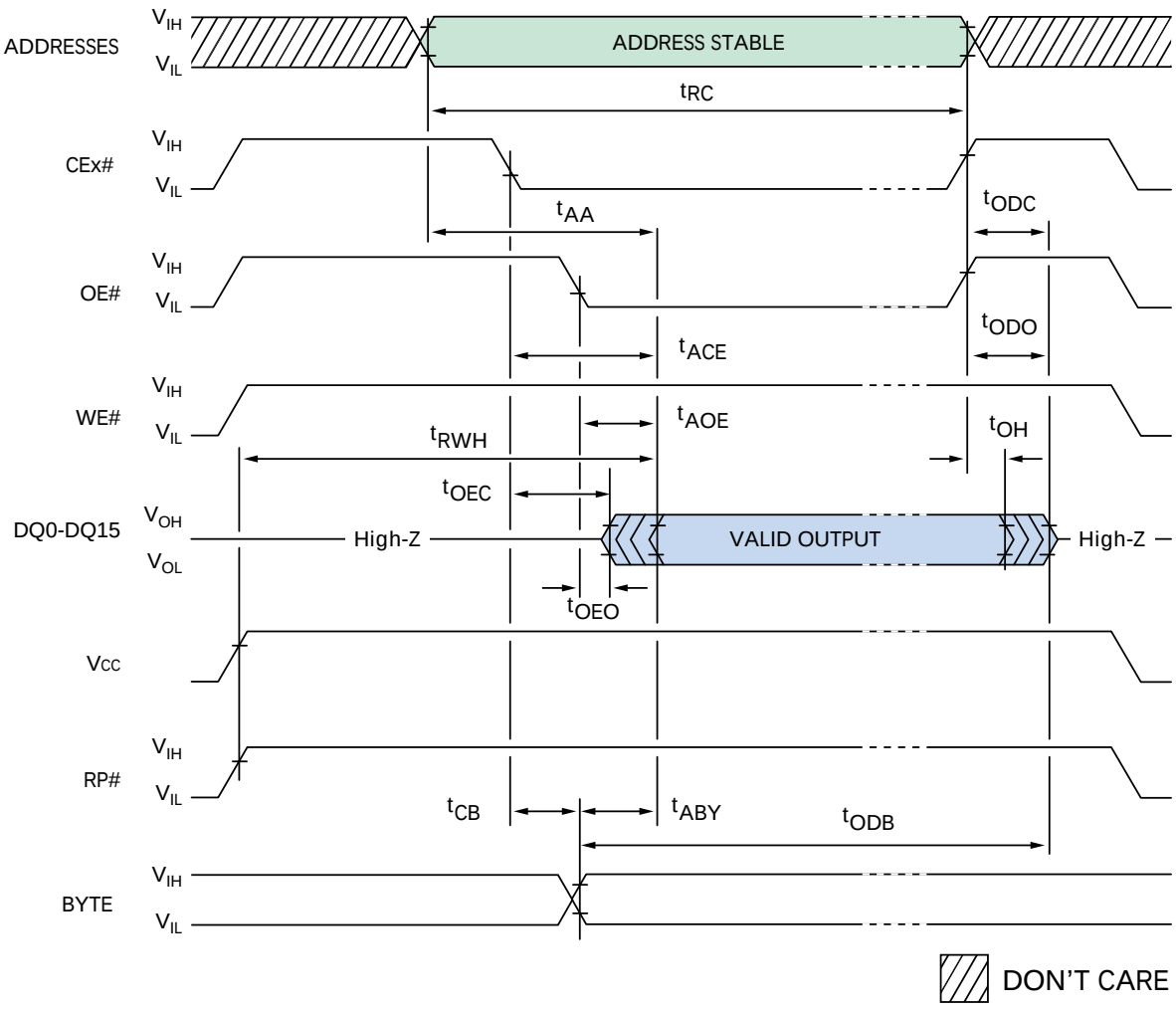
AC CHARACTERISTICS – READ-ONLY OPERATIONS[1]

Note 1; Commercial Temperature ($0^oC \le T_A \le +70^oC$) and Extended Temperature ($-40^oC \le T_A \le +85^oC$)

PARAMETER	SYMBOL	3.3V ±0.3V Vcc -75		2.7V–3.6V Vcc -10		UNITS	NOTES
		MIN	MAX	MIN	MAX		
READ/WRITE Cycle Time 1	^tRC	75		100		ns	
Address to Output Delay	^tAA		75		100	ns	2
CEx# to Output Delay	^tACE		75		100	ns	3
OE# to Output Delay	^tAOE		45		50	ns	3
RP# HIGH to Output Delay	^tRWH		600		600	ns	
CEx# to Output in Low-Z	^tOEC	0		0		ns	4
OE# to Output in Low-Z	^tOEO	0		0		ns	4
CEx# HIGH to Output in High-Z	^tODC		50		50	ns	4
OE# HIGH to Output in High-Z	^tODO		20		20	ns	4
Output Hold from Address, CEx#, or OE# change, whichever occurs first	^tOH	0		0		ns	4
CEx# LOW to BYTE# HIGH or LOW	^tCB		5		5	ns	4
BYTE# to Output Delay	^tABY		100		120	ns	4
BYTE# to Output in High-Z	^tODB		30		30	ns	4

NOTE:
1. See READ, WRITE, and RESET Timing Diagrams for testing characteristics.
2. See AC Input/Output Reference Waveform for maximum allowable input slew rate.
3. OE# may be delayed up to ^tACE - ^tAOE after the falling edge of CEx# without impact on ^tACE.
4. Sampled, not 100% tested.

READ OPERATIONS



TIMING PARAMETERS

SYMBOL	-75 MIN	-75 MAX	-10 MIN	-10 MAX	UNITS
tRC	75		100		ns
tAA		75		100	ns
tACE		75		100	ns
tAOE		45		50	ns
tRWH		600		600	ns
tOEC	0		0		ns
tOEO	0		0		ns

SYMBOL	-75 MIN	-75 MAX	-10 MIN	-10 MAX	UNITS
tODC		50		50	ns
tODO		20		20	ns
tOH	0		0		
tCB		5		5	ns
tABY		100		120	ns
tODB		30		30	ns

WRITE/ERASE CURRENT DRAIN

Commercial Temperature ($0^{\circ}C \le T_A \le +70^{\circ}C$) and Extended Temperature ($-40^{\circ}C \le T_A \le +85^{\circ}C$)

PARAMETER/CONDITION	SYMBOL	TYP	MAX	UNITS	NOTES
PROGRAM OR SET LOCK BIT CURRENT: V_{PP} SUPPLY $V_{PP} = V_{PPH1/2/3}$	I_{PP3}		15	µA	1, 2
BLOCK ERASE OR CLEAR BLOCK LOCK BITS CURRENT: V_{PP} SUPPLY $V_{PP} = V_{PPH1/2/3}$	I_{PP4}		15	µA	1, 2
PROGRAM SUSPEND OR BLOCK ERASE SUSPEND CURRENT: V_{PP} SUPPLY $V_{PP} = V_{PPH1/2/3}$	I_{PP5}	10	±15	µA	1
PROGRAMMING AND SET LOCK BIT CURRENT: V_{CC} SUPPLY $V_{PP} = V_{PPH1/2/3}$	I_{CC6}		95	mA	1, 2
BLOCK ERASE OR CLEAR BLOCK LOCK BITS CURRENT: V_{CC} SUPPLY $V_{PP} = V_{PPH1/2/3}$	I_{CC7}		55	mA	1, 2
PROGRAM SUSPEND OR BLOCK ERASE SUSPEND CURRENT: V_{CC} SUPPLY CEx# = V_{IH}	I_{CC8}	1	6	mA	1, 3

NOTE:
1. All currents are in RMS unless otherwise noted. Typical values at nominal V_{CC} voltage and $T_A = +25^{\circ}C$. These currents are valid for all product versions (packages and speeds).
2. Sampled, not 100% tested.
3. I_{CC8} is specified with the device deselected. If read or programmed while in erase suspend mode, the device's current is the sum of I_{CC8} and I_{CC2} or I_{CC6}.

AC CHARACTERISTICS – WRITE OPERATIONS

Notes: 1, 2; Commercial Temperature ($0^oC \le T_A \le +70^oC$) and Extended Temperature ($-40^oC \le T_A \le +85^oC$)

PARAMETER	SYMBOL	3.3V ±0.3V Vcc -75		2.7V–3.6V Vcc -10		UNITS	NOTES
		MIN	MAX	MIN	MAX		
RP# HIGH Recovery to WE# (CEx#) Going LOW	^tRS	1		1		µs	3
CEx# Setup to WE# Going LOW	^tCS	10		10		ns	
WE# Setup to CEx# Going LOW	^tWS	0		0		ns	
WE# Pulse Width	^tWP	50		50		ns	
CEx# Pulse Width	^tCP	70		70		ns	
Data Setup to WE# (CEx#) Going HIGH	^tDS	50		50		ns	4
Address Setup to WE# (CEx#) Going HIGH	^tAS	50		50		ns	4
CEx# Hold from WE# HIGH	^tCH	10		10		ns	
WE# Hold from CEx# HIGH	^tWH	0		0		ns	
Data Hold from WE# (CEx#) HIGH	^tDH	5		5		ns	
Address Hold from WE# (CEx#) HIGH	^tAH	5		5		ns	
Pulse Width HIGH	^tWPH	30		25		ns	
CEx# Pulse Width HIGH	^tCPH	25		25		ns	
WP# V_{IH} Setup to WE# (CEx#) Going HIGH	^tWPS	100		100		ns	
V_{PP} Setup to WE# (CEx#) Going HIGH	^tVPS	100		100		ns	3
Write Recovery before READ	^tWR	0		0		ns	
WE# HIGH to STS in RY/BY# LOW	^tSTS		100		100	ns	
WE# (CEx#) HIGH to Busy Status (SR7 = 0)	^tWB		100		100	ns	3, 5
WP# V_{IH} Hold from Valid SRD	^tQVSL	0		0		ns	3, 5
V_{PP} Hold from Valid SRD, STS in RY#/BY# HIGH	^tVPH	0		0		ns	3, 5

NOTE:
1. READ timing characteristics during BLOCK ERASE, PROGRAM, and LOCK BIT CONFIGURATION operations are the same as during READ-only operations. Refer to AC Characteristics – READ-Only Operations.
2. See READ, WRITE, and RESET timing diagrams for testing characteristics.
3. Sampled, not 100% tested.
4. Refer to Table 2 for valid A_{IN} and D_{IN} for block erase, program, or lock bit configuration.
5. V_{PP} should be at $V_{PPH1/2/3}$ until determination of block erase, program, or lock bit configuration success (SR1/3/4/5 = 0).

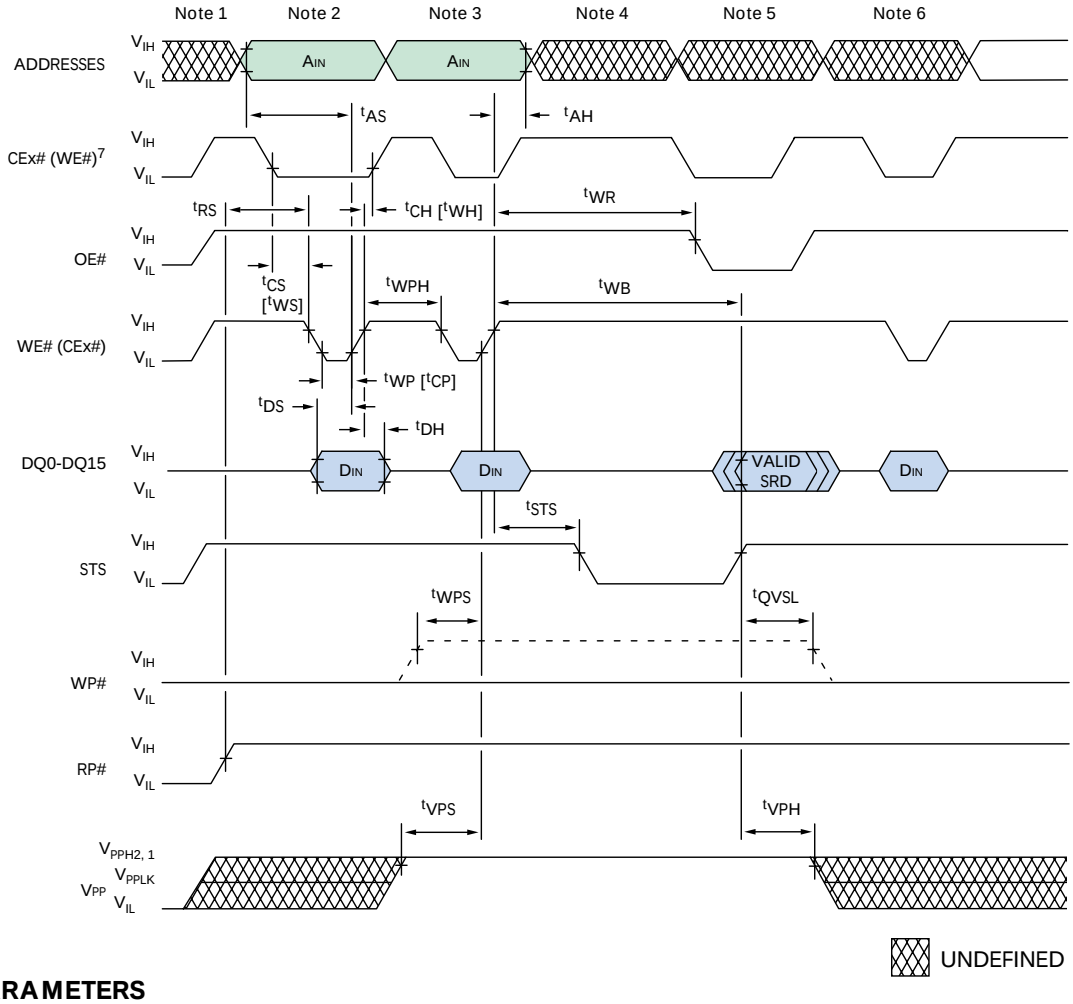
ERASE, WRITE, AND LOCK BIT CONFIGURATION PERFORMANCE

Notes: 1, 2

PARAMETER	SYMBOL	3.3V ±0.3V Vcc		2.7V–3.6V Vcc		UNITS	NOTES
		TYP[3]	MAX[4]	TYP[3]	MAX[4]		
Byte/word program time (using write buffer)	^{t}WED1	5.66	250	5.8	250	µs	5
Per byte program time (without write buffer)	^{t}WED2	19.51	250	18.0	160	µs	6
Per word program time (without write buffer)	^{t}WED3	21.75	250	20.0	190	µs	6
Block program time (byte mode)	^{t}WED4	1.6	16.5	1.2	2.0	sec	6
Block program time (word mode)	^{t}WED5	0.89	8.2	0.7	1.0	sec	6
Block program time (using write buffer)	^{t}WED6	0.36	4.1	0.37	4.0	sec	6
Block erase time	^{t}WED7	0.55	20	0.56	6.0	sec	6
Full chip erase time	^{t}WED8	17.6	320	17.9	190	sec	
Set lock bit time	^{t}WED9	22.75	250	20.0	190	µs	6
Clear block lock bits time	^{t}WED10	0.55	10	0.56	6.0	sec	6
Program suspend latency time to read	^{t}LPS	7.1	10	7.2	10	µs	
Erase suspend latency time to read	^{t}LES	15.2	21.1	15.5	21.5	µs	

NOTE:
1. These performance numbers are valid for all speed versions.
2. Sampled, but not 100% tested.
3. Typical values measured at T_A = +25ºC and nominal voltages. Assumes corresponding lock bits are not set. Subject to change based on device characterization.
4. Maximum values represent less than 1% of units exposed to greater than 100,000 cycles.
5. Uses whole buffer.
6. Excludes system-level overhead.

WRITE OPERATIONS



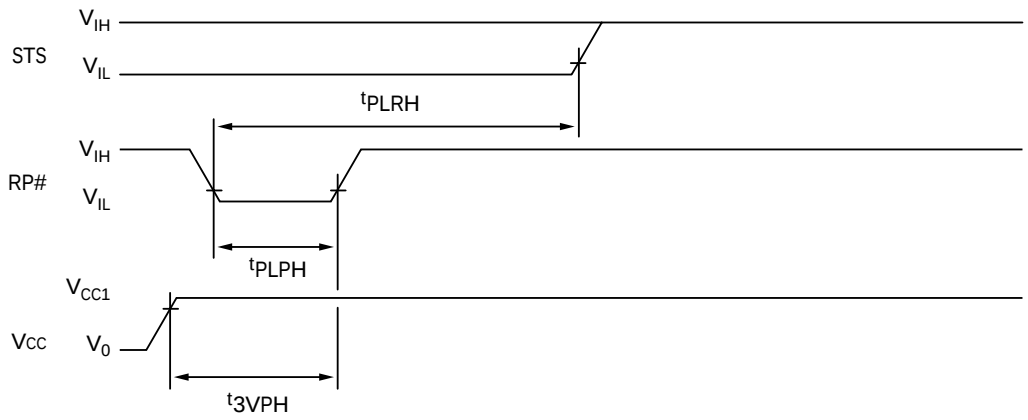
TIMING PARAMETERS

SYMBOL	-75 MIN	-75 MAX	-10 MIN	-10 MAX	UNITS
tRS	1		1		µs
tCS	10		10		ns
tWS	0		0		ns
tWP	50		50		ns
tCP	70		70		ns
tDS	50		50		ns
tAS	50		50		ns
tCH	10		10		ns
tWH	0		0		ns
tDH	5		5		ns

SYMBOL	-75 MIN	-75 MAX	-10 MIN	-10 MAX	UNITS
tAH	5		5		ns
tWPH	30		30		ns
tWPS	100		100		ns
tVPS	100		100		ns
tWR	0		0		ns
tSTS		100		100	ns
tWB		100		100	ns
tQVSL	0		0		ns
tVPH	0		0		ns

NOTE:
1. Vcc power-up and standby.
2. Write block erase or program setup.
3. Write block erase confirm or valid address and data.
4. Automated erase and program delay.
5. Read status register data.
6. WRITE READ ARRAY command.
7. CEx# is the latter of CE0# and CE1# LOW or the first of CE0# or CE1# HIGH.

RESET OPERATION



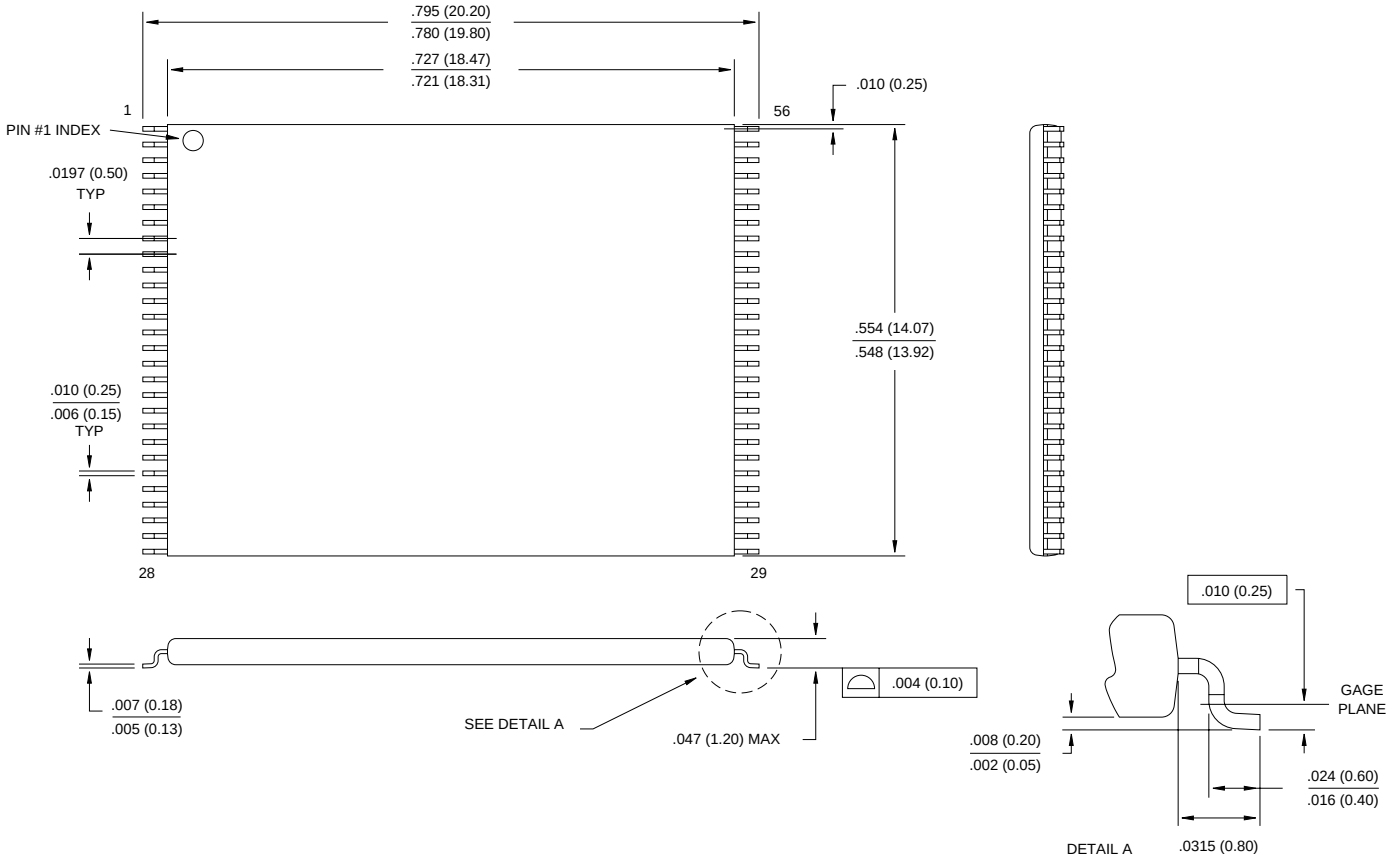
RESET AC SPECIFICATIONS

Note: 1

PARAMETER	SYMBOL	2.7V–3.6V Vcc		3.3V ±0.3V Vcc		UNITS	NOTES
		MIN	MAX	MIN	MAX		
RP# Pulse LOW Time (If RP# is tied to Vcc, this specification is not applicable)	tPLPH	100		100		ns	
RP# LOW to Reset during block erase, program, or lock bit configuration	tPLRH		20		20	µs	2, 3
Vcc at 2.7V to RP# HIGH Vcc at 3.0V to RP# HIGH	t3VPH		50		50	µs	

NOTE:
1. These specifications are valid for all product versions (packages and speeds).
2. If RP# is asserted while a BLOCK ERASE, PROGRAM, or LOCK BIT CONFIGURATION operation is not executing, the reset will complete within tPLPH.
3. A reset time, tPHQV, is required from the latter of STS in RY/BY# mode or RP# going HIGH until outputs are valid.

56-PIN PLASTIC TSOP I



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

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